MOTOROLA

CMOS DATA MANUAL
VOLUME 1
STANDARD LOGIC

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Introduction
Or how to find the information you need

The European CMOS Data Manuals Volumes 1, 2 and 3 contain all the relevant data required to design and use Motorola CMOS Functions. The first two volumes replace the European CMOS Selection Data Book which was published in 1979.

Volume 1 contains data on Standard Logic which is defined as the following functions:

- NAND / NOR / AND / OR / Complex Gates
- Inverters / Buffers / Level Translators
- Schmitt Triggers
- Flip Flops / Latches
- Shift Registers
- Counters
- Adders / Comparators
- Parity Generators / Checkers
- ALU's / Rate Multipliers
- Encoders / Decoders
- Multiplexers / Demultiplexers / Bilateral Switches
- Multivibrators / Oscillators / Timers

Volume 2 contains data on Special Functions which are defined as the following functions:

- PLL Frequency Synthesizers
- Display Decoders / Drivers
- A/D, D/A Converters / Logic Functions
- Operational Amplifiers / Comparators
- Remote Control Functions
- Radio / TV Functions
- Miscellaneous Functions

Volume 3 contains data on High Speed CMOS.

Telecommunications functions are listed in the Selection Guide but data is to be found in the Telecommunications Data Manual.

Microprocessors and peripherals are listed in the Selection Guide, but data is to be found in the Microprocessors Data Manuals (8 and 16-Bit).

Memories are also listed in the Selection Guide. Volume 2, Special Functions, contains data on the smaller memories. The data for larger memories is to be found in the Memory Data Manual. See the selector guides for details.

Selection Guides 1

B-Series Family Data 2

Data Sheets 3

Mechanical Data 4

Handling Precautions 5

Reliability and Quality Assurance 6

Publications and Applications 7

The contents of each section of this book are:

1. SELECTION GUIDES

Ordering Information (page 1-2) — defines the numbering system and suffixes and gives details of processing options.

Selection Guide by Part Number (page 1-6) — contains a human alphanumeric listing of all functions with details of suffixes and pins, and where to find detailed technical data. This section can also be used as a cross reference to find equivalents for other suppliers' functions.

Selection Guide by Function (page 1-13) — lists all devices which are capable of performing broadly defined functions, and where to find detailed technical data.

Counter Selector Table (page 1-18) — gives comparative data for key characteristics of counters.

HSCMOS Selector Guide (page 1-19) — gives key family characteristics and ordering information. Lists devices by function and shows equivalent LSTTL and CMOS functions.

Gate Arrays (page 1-26) — a brief outline of the MOS Gate Arrays and the design system.

2. B-SERIES FAMILY DATA

EIA/JEDEC and Motorola formats for CMOS Industry B and UB series specifications.

3. DATA SHEETS

Technical data for all special functions. Where parts are still at the design and development stage, then the data consists of either Product Previews or Advance Information.

4. MECHANICAL DATA

Package dimensions for all devices in this book.

5. HANDLING PRECAUTIONS

The static and latch-up problems associated with MOS are now well understood. This section lists the precautions to be taken during shipment, assembly and test to avoid these problems. It is recommended that this section be read thoroughly.

6. RELIABILITY AND QUALITY ASSURANCE

This section describes the key elements of Motorola's reliability and quality assurance activities, and gives the results of the 1982 tests.

7. PUBLICATIONS / APPLICATIONS

Lists the publications available from Motorola Semiconductors.

On the back cover, there is a list of Motorola Sales Offices and Distributors.

Selection Guides

1

1

Ordering Information

STANDARD PRODUCTS

MC14001BAL

- BAL — denotes — Operating Voltage Range
  - — Operating Temperature Range
  - — Package Material
- MC14001 — denotes Function

SUFFIXES

AL	3 to 18 V, −55 to +125°C, Ceramic Package
CL	3 to 18 V, −40 to +85°C, Ceramic Package
CP	3 to 18 V, −40 to +85°C, Plastic Package
L	Limited Voltage Range, Limited Temperature Range, Ceramic Package
P	Limited Voltage Range, Limited Temperature Range, Plastic Package
EFL	3 to 18 V, −55 to +125°C, Ceramic Package
FL	3 to 18 V, −40 to +85°C, Ceramic Package
FP	3 to 18 V, −40 to +85°C, Plastic Package
EVL	3 to 6 V, −55 to +125°C, Ceramic Package
VL	3 to 6 V, −40 to +85°C, Ceramic Package
VP	3 to 6 V, −40 to +85°C, Plastic Package
Z	Limited Voltage Range, Limited Temperature Range, Leadless Chip Carrier

OPTIONS

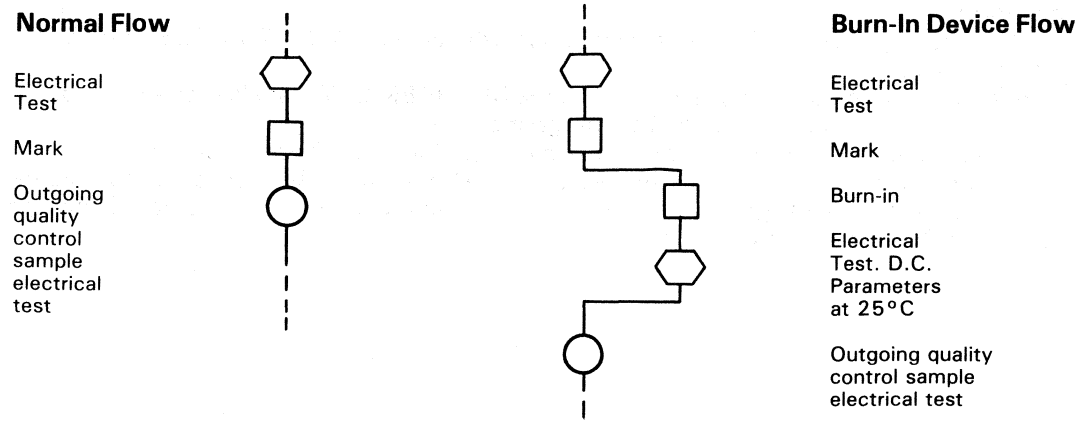
1. Burn-in

Motorola CMOS integrated circuits are manufactured under strict quality control. In-process screens and tight out-going inspection result in a high order of quality and reliability.

In addition, Burn-in is an option available on all CMOS packaged products. The benefits of this option are:

- reduced infant mortality (typically 0.2% of the product is screened out);
- reduced board and system rework;
- reduced equipment downtime;
- reduced field failures.

Additional processing of these burnt-in circuits is as follows:



Motorola Burn-in is performed under the following conditions:

V_{DD}	15 V
Temperature	125°C ambient
Time	168 hours
Bias	Dynamic for Memories and Analog Circuits, Static for all others

Ordering Information:

The Burn-in option is selected by adding the suffix D to the part number, for example:

MC14001BALD

2. Chips and Wafers

Chips and wafers are available for all CMOS types. For further information, consult your Motorola Sales Office or authorized Motorola Distributor.

3. HI-REL

The HI-REL Operation in East Kilbride supplies components which have been qualified and/or processed to European standards or military specifications. The factory approvals are: Def. Stan. 05-21, BS9000, CECC.

The Def. Stan. 05-21 approval, which is equivalent to N.A.T.O. AQAP 1, is monitored by the British Ministry of Defence.

The BS9000 and CECC approvals are monitored by the NSI (National Supervisory Inspectorate).

Additionally, parts can be processed in accordance with MIL-STD-883B, per JEDEC Publication 101.

For comparative purposes, table 1 gives the MIL-HDBK-217D quality levels and quality factors (π_Q) for the various HI-REL programs.

Table 2 gives a cross-reference of test methods for various specifications.

For specific details of availability, see the latest edition of the "European Semiconductor Hi-Reliability Programs" brochure, or contact your Motorola Sales Office or authorised Motorola distributor.

Table 1 — Comparison of HI-REL programs

Program	Description	MIL-HDBK-217D Level	MIL-HDBK-217D Factor
BS9000/CECC90000 Level B	Full Qualification, Full Processing	B	1.0
BS9000/CECC90000 Level B	Interim Qualification, Full Processing	B-0	2.0
BS9000/CECC90000 Level B	No Qualification, Full Processing	B-2	6.5
MIL-STD-883B Level B	No Qualification, JEDEC 101 Processing	B-2	6.5
BS9000/CECC90000 Level C	Full Qualification Full Processing	C	8.0
BS9000/CECC90000 Level C	No Qualification Full Processing	C1	13.0
MIL-STD-883B Level C	No Qualification Full Processing	C1	13.0
Commercial Ceramic	168 Hour Burn-in at 15 V, 125° C, with 100° C Electrical Test	D	17.5

TABLE 2 — TEST METHOD CROSS-REFERENCE

Test	CECC 90000	IEC68	BS9400	Method BS2011	MIL STD833
Precap Visual				—	2010A or B
Low Temperature Storage	4.6.1.2	2-1	1.2.10A or B	Aa	
High Temperature Storage	4.6.1.1	2-2	As BS2011	Ba	1008
Rapid Change in Temp. (air)	4.6.8.1	2-14-Na	1.2.6.13	Na	1010c
Rapid Change in Temp. (liquid)	4.6.8.3	2-14-Nc	As BS2011	Nc	1011a
Humidity (Cycled)	4.6.3.1	2-4	As BS2011	Da	—
Humidity (Cycled)	4.6.3.2	2-30	—	Db	—
Humidity (Cycled)			—	—	1004
Humidity (Constant)	4.6.2 Cond.1	2-3	As BS2011	Ca	
Acceleration	4.6.7	2-7	As BS2011	Ca	2001
Hermeticity (fine)	4.6.9.1	2-17QK	As BS2011	Qk	1014A
Hermeticity (gross)	4.6.9.2		1.2.6.14.3	Qc	1014C
Solderability	4.6.10	2-20	As BS2011	Ta	2003
Termination Robustness (DIL)	4.6.12.2	2-21	As BS2011 or 1.2.6.16.3	Ub	2004
Mechanical Shock	4.6.4	2.27	As BS2011	Ea	2002
Vibration (Swept frequency)	4.6.5	2-6	As BS2011	Fc/B4	2007
Salt Mist	4.6.14	2-11	—	Ka	—
Salt Mist	—	—	—	—	1009
Operating Life Test	4.8	—	1.2.7.2	—	1005
Electrical Burn-In	D.S.	—	1.2.9.2	—	1015

1 Selection Guide by Part Number

Device	Function	Suffix	Pins	Page
MC54HCXXX	High Speed CMOS Series	J		□
MC68HC04P2	8-Bit Single Chip Microcomputer	L,P,Z	28	×
MC68HC04P3	8-Bit CMOS Microcomputer EPROM	L,P,Z	28	×
MC68HC05C4	8-Bit Single Chip Microcomputer	L,P,Z	40	×
MC68HC09E	8-Bit Microprocessor	L,P,Z	40	×
MC74HCXXX	High Speed CMOS Series	J,N		□
MC6172	2400 Baud DPSK Modulator	L,P	24	●
MC6173	2400 Baud DPSK Demodulator	L,P	24	●
MC6220	4-Bit Microcomputer with PLL Frequency Synthesizer (NMOS Device)	P	28	§
MC6860	Low Speed Modem	L,P	24	●
MC6862	Part Number changed to MC6172			
MC14000UB	Dual 3-Input NOR Gate Plus Inverter	AL,CL,CP	14	3-2
MC14001B	Quad 2-Input NOR Gate	AL,CL,CP	14	3-5
MC14001UB	Quad 2-Input NOR Gate	AL,CL,CP	14	3-14
MC14002B	Dual 4-Input NOR Gate	AL,CL,CP	14	3-5
MC14002UB	Dual 4-Input NOR Gate	AL,CL,CP	14	3-14
MC14006B	18-Bit Static Shift Register	AL,CL,CP	14	3-20
MC14007UB	Dual Complimentary Pair Plus Inverter	AL,CL,CP	14	3-24
MC14008B	4-Bit Full Adder	AL,CL,CP	16	3-28
4009	See MC14049UB - Pin for Pin Equivalent			
4010	See MC14050B - Pin for Pin Equivalent			
MC14011B	Quad 2-Input NAND Gate	AL,CL,CP	14	3-5
MC14011UB	Quad 2-Input NAND Gate	AL,CL,CP	14	3-14
MC14012B	Dual 4-Input NAND Gate	AL,CL,CP	14	3-5
MC14012UB	Dual 4-Input NAND Gate	AL,CL,CP	14	3-14
MC14013B	Dual D Flip-Flop	AL,CL,CP	14	3-36
MC14014B	8-Bit Static Shift Register	AL,CL,CP	16	3-40
MC14015B	Dual 4-Bit Static Shift Register	AL,CL,CP	16	3-44
MC14016B	Quad Analog Switch/Multiplexer	AL,CL,CP	14	3-50
MC14017B	Decade Counter/Divider	AL,CL,CP	16	3-56
MC14018B	Presettable Divide-By-N Counter	AL,CL,CP	16	3-61
4019B	See MC14519B - Normally Pin for Pin Equivalent			
MC14020B	14-Bit Binary Counter	AL,CL,CP	16	3-65
MC14021B	8-Bit Static Shift Register	AL,CL,CP	16	3-40
MC14022B	Octal Counter/Divider	AL,CL,CP	16	3-70

× See the 8-Bit Microprocessors Data Manual.
§ See Data Sheet.
□ See the CMOS Data Manual, Volume 3, High Speed CMOS.
● See the Telecommunications Data Manual.

Device	Function	Suffix	Pins	Page
MC14023B	Triple 3-Input NAND Gate	AL,CL,CP	14	3-5
MC14023UB	Triple 3-Input NAND Gate	AL,CL,CP	14	3-14
MC14024B	7-Stage Ripple Counter	AL,CL,CP	14	3-76
MC14025B	Triple 3-Input NOR Gate	AL,CL,CP	14	3-5
MC14025UB	Triple 3-Input NOR Gate	AL,CL,CP	14	3-14
MC14027B	Dual J-K Flip-Flop	AL,CL,CP	16	3-82
MC14028B	BCD-to-Decimal/Binary-to-Octal Decoder	AL,CL,CP	16	3-86
MC14029B	Binary/Decade Up/Down Counter	AL,CL,CP	16	3-91
4030B	See MC14070B - Pin for Pin Equivalent			
4031B	See MC14557B - Functionally Equivalent			
MC14032B	Triple Serial Adder (Positive Logic)	AL,CL,CP	16	3-97
MC14034B	8-Bit Universal Bus Register	AL,CL,CP	24	3-102
MC14035B	4-Bit Shift Register	AL,CL,CP	16	3-109
MC14038B	Triple Serial Adder (Negative Logic)	AL,CL,CP	16	3-97
MC14040B	12-Bit Binary Counter	AL,CL,CP	16	3-114
MC14042B	Quad Transparent Latch	AL,CL,CP	16	3-118
MC14043B	Quad NOR R-S Latch	AL,CL,CP	16	3-122
MC14044B	Quad NAND R-S Latch	AL,CL,CP	16	3-122
MC14046B	Phase-Locked Loop	AL,CL,CP	16	3-126
4047B	See MC14528B - Functionally Equivalent			
MC14049UB	Hex Inverter/Buffer	AL,CL,CP	16	3-131
MC14050B	Hex Buffer	AL,CL,CP	16	3-131
MC14051B	8-Channel Analog Multiplexer/Demultiplexer	AL,CL,CP	16	3-135
MC14052B	Dual 4-Channel Analog Multiplexer/ Demultiplexer	AL,CL,CP	16	3-135
MC14053B	Triple 2-Channel Analog Multiplexer/ Demultiplexer	AL,CL,CP	16	3-135
4055B	See MC14543B - Functionally Equivalent			
4056B	See MC14543B - Normally Pin for Pin Equivalent			
4057B	See MC14581B - Functionally Equivalent			
MC14060B	14-Bit Binary Counter and Oscillator	AL,CL,CP	14	3-141
4061	See MCM14537 - Functionally Equivalent			
4063	See MC14585B - Functionally Equivalent			
MC14066B	Quad Analog Switch/Multiplexer	AL,CL,CP	14	3-145
MC14067B	16-Channel Analog Multiplexer/Demultiplexer	AL,CL,CP	24	3-150
MC14068B	8-Input NAND Gate	AL,CL,CP	14	3-5
MC14069UB	Hex Inverter	AL,CL,CP	14	3-157
MC14070B	Quad Exclusive OR Gate	AL,CL,CP	14	3-159
MC14071B	Quad 2-Input OR Gate	AL,CL,CP	14	3-5
MC14072B	Dual 4-Input OR Gate	AL,CL,CP	14	3-5
MC14073B	Triple 3-Input AND Gate	AL,CL,CP	14	3-5
MC14075B	Triple 3-Input OR Gate	AL,CL,CP	14	3-5
MC14076B	Quad D-Type Register	AL,CL,CP	16	3-165
MC14077B	Quad Exclusive NOR Gate	AL,CL,CP	14	3-159
MC14078B	8-Input NOR Gate	AL,CL,CP	14	3-5
MC14081B	Quad 2-Input AND Gate	AL,CL,CP	14	3-5
MC14082B	Dual 4-Input AND Gate	AL,CL,CP	14	3-5
4085B	See MC14506B - Functionally Equivalent			

Device	Function	Suffix	Pins	Page
MC14093B	Quad 2-Input NAND Schmitt Trigger	AL,CL,CP	14	3-173
MC14094B	8-Bit Bus Compatible Shift/Store Latch	AL,CL,CP	16	3-177
MC14097B	Dual 8-Channel Analog Multiplexer/ Demultiplexer	AL,CL,CP	24	3-150
4098B	See MC14528B - Normally Pin for Pin Equivalent			
MC14099B	8-Bit Addressable Latch	AL,CL,CP	16	3-182
MC14106B	Hex Schmitt Trigger	AL,CL,CP	14	3-189
MC14160B	Synchronous Programmable Decade Counter	AL,CL,CP	16	3-189
MC14161B	Synchronous Programmable 4-Bit Binary Counter	AL,CL,CP	16	3-189
MC14162B	Synchronous Programmable Decade Counter	AL,CL,CP	16	3-189
MC14163B	Synchronous Programmable 4-Bit Binary Counter	AL,CL,CP	16	3-189
MC14174B	Hex D Flip-Flop	AL,CL,CP	16	3-197
MC14175B	Quad D Flip-Flop	AL,CL,CP	16	3-201
MC14194B	4-Bit Universal Shift Register	AL,CL,CP	16	3-205
MC14400	PCM Monocircuit	L	16	●
MC14401	PCM Monocircuit	L	18	●
MC14402	PCM Monocircuit	L	22	●
		Z	28	
MC14403	PCM Monocircuit	L	16	●
MC14405	PCM Monocircuit	L	16	●
MC14408	Binary-to-Phone Pulse Converter	L,P	16	●
MC14409	Binary-to-Phone Pulse Converter	L,P	16	●
MC14410	2-of-8 Tone Encoder	L,P	16	●
MC14411	Bit-Rate Frequency Generator	L,P	24	● ○
MC14412	Universal Low Speed Modem	FL,FP,VL,VP	16	●
MC14413	PCM Sampled Data Filter, See Note A	L,P	16	●
		Z	18	
MC14414	PCM Sampled Data Filter, See Note A	L,P	16	●
		Z	18	
MC14415	Quad Precision Timer/Driver	EFL,FL,FP EVL, VL, VP	16	3-209
MC14416	PCM Time Slot Assigner Circuit	L,P	16	●
MC14417	PCM Time Slot Assigner Circuit	L,P	18	●
MC14418	PCM Time Slot Assigner Circuit	L,P	22	●
MC14419	2-of-8 Keypad-to-Binary Encoder	L,P	16	3-214
MC14426	8 × 14-Bit Static Tuning Memory	P	16	○
MC14429	Tuning Memory Control, See Note B	P	18	○
MC14430	Input Address Encoder	P	16	3-218
MC14433	3-1/2 Digit A/D Converter	L,P	24	○
MC14442	Microprocessor Compatible A/D Converter	L,P	28	○
MC14443	6-Channel A/D Converter Subsystem	L,P	16	○
MC14444	Microprocessor Compatible A/D Converter	L,P	40	○
MC14447	6-Channel A/D Converter Subsystem	L,P	16	○

○ See the CMOS Data Manual, Volume 2, Special Functions.
● See the Telecommunications Data Manual.

Note A: Add Suffix 1 or 2. Example MC14413L2.
Note B: Add Suffix B. Example MC14429PB.

Device	Function	Suffix	Pins	Page
4449UB	See MC14049UB, Pin for Pin Equivalent			
MC14457	Remote Control Transmitter	P	16	○
MC14458	Remote Control Receiver	P	24	○
MC14466	Low Cost Smoke Detector	P	16	○
MC14467	Low Cost Smoke Detector	P	16	○
MC14468	Interconnect Smoke Detector	P	16	○
MC14469	Addressable Asynchronous Receiver/Transmitter	L,P	40	○
MC14490	Hex Contact Bounce Eliminator	L,P	16	○
MC14493	Binary-to-7-Segment Latch Decoder/Driver	L,P	16	○
MC14494	Binary-to-7-Segment Latch Decoder/Driver	L,P	16	○
MC14495	Binary-to-7-Segment Hexadecimal Latch/	L,P	16	○
	Decoder/Driver, See Note C	L1,P1	16	○
MC14497	PCM Remote Control Transmitter	P	18	○
MC14499	4-Digit 7-Segment LED Display Decoder/Driver	P	18	○
MC14500B	Industrial Control Unit	AL,CL,CP	16	○
MC14501UB	Triple Gate	AL,CL,CP	16	3-222
MC14502B	Strobed Hex Inverter/Buffer	AL,CL,CP	16	3-226
MC14503B	Hex 3-State Buffer	AL,CL,CP	16	3-230
MC14504B	Hex TTL or CMOS to CMOS Level Shifter	AL,CL,CP	16	3-234
MC14506UB	Dual Expandable AOI Gate	AL,CL,CP	16	3-237
MC14508B	Dual 4-Bit Latch	AL,CL,CP	24	3-242
MC14510B	BCD Up/Down Counter	AL,CL,CP	16	3-247
MC14511B	BCD-to-7-Segment Latch/Decoder/Driver	AL,CL,CP	16	○
MC14512B	8-Channel Data Selector	AL,CL,CP	16	3-253
MC14513B	BCD-to-7-Segment Latch/Decoder/Driver			
	with Ripple Blanking	AL,CL,CP	18	○
MC14514B	4-Bit Transparent Latch/4-to-16 Line			
	Decoder (High)	AL,CL,CP	24	3-257
MC14515B	4-Bit Transparent Latch/4-to-16 Line			
	Decoder (Low)	AL,CL,CP	24	3-257
MC14516B	Binary Up/Down Counter	AL,CL,CP	16	3-263
MC14517B	Dual 64-Bit Static Shift Register	AL,CL,CP	16	3-269
MC14518B	Dual BCD Up Counter	AL,CL,CP	16	3-273
MC14519B	4-Bit And/Or Selector	AL,CL,CP	16	3-278
MC14520B	Dual Binary Up Counter	AL,CL,CP	16	3-273
MC14521B	24-Stage Frequency Divider	AL,CL,CP	16	3-283
MC14522B	Programmable BCD Divide-by-N Counter	AL,CL,CP	16	3-289
MC14526B	Programmable Binary Divide-by-N Counter	AL,CL,CP	16	3-289
MC14527B	BCD Rate Multiplier	AL,CL,CP	16	3-296
MC14528B	Dual Monostable Multivibrator	AL,CL,CP	16	3-302
MC14529B	Dual 4-Channel Analog Data Selector	AL,CL,CP	16	3-307
MC14530B	Dual 5-Input Majority Logic Gate	AL,CL,CP	16	3-313
MC14531B	12-Bit Parity Tree	AL,CL,CP	16	3-318
MC14532B	8-Bit Priority Encoder	AL,CL,CP	16	3-321
MC14534B	5-Decade Counter	AL,CL,CP	24	3-327
MC14536B	Programmable Timer	AL,CL,CP	16	3-333
MC14538B	Dual Precision Monostable Multivibrator	AL,CL,CP	16	3-340

○ See the CMOS Data Manual, Volume 2, Special Functions.

Note C: There are two versions of this device, with different electrical and switching characteristics. To order, one has suffix L or P and the other L1 or P1. See data sheets for details.

Device	Function	Suffix	Pins	Page
MC14539B	Dual 4-Channel Data Selector/Multiplexer	AL,CL,CP	16	3-348
MC14541B	Programmable Oscillator-Timer	AL,CL,CP	14	3-352
MC14543B	BCD-to-7-Segment Latch/Decoder/Driver	AL,CL,CP	16	○
MC14544B	BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking	AL,CL,CP	18	○
MC14547B	High Current BCD-to-7-Segment Decoder/Driver	AL,CL,CP	16	○
MC14548B	Dual Monostable Multivibrator (Retriggerable/Resettable)	L,P	16	3-358
MC14549B	Successive Approximation Register	AL,CL,CP	16	○
MC14551B	Quad 2-Channel Analog Multiplexer/ Demultiplexer	AL,CL,CP	16	3-365
MC14553B	3-Digit BCD Counter	AL,CL,CP	16	3-371
MC14554B	2 × 2-Bit Parallel Binary Multiplier	AL,CL,CP	16	3-377
MC14555B	Dual Binary to 1-of-4 Decoder	AL,CL,CP	16	3-381
MC14556B	Dual Binary to 1-of-4 Decoder (Inverting)	AL,CL,CP	16	3-381
MC14557B	1-to-64 Bit Variable Length Shift Register	AL,CL,CP	16	3-384
MC14558B	BCD-to-7-Segment Decoder	AL,CL,CP	16	○
MC14559B	Successive Approximation Register	AL,CL,CP	16	○
MC14560B	NBCD Adder	AL,CL,CP	16	3-388
MC14561B	9's Complementer	AL,CL,CP	14	3-392
MC14562B	128-Bit Static Shift Register	AL,CL,CP	14	3-398
MC14566B	Industrial Time-Base Generator	AL,CL,CP	16	3-402
MC14568B	Phase Comparator and Programmable Counters	AL,CL,CP	16	3-408
MC14569B	Dual Programmable BCD/Binary Counter	AL,CL,CP	16	3-418
MC14572UB	Hex Gate	AL,CL,CP	16	3-422
MC14573	Quad Programmable Op Amp	CL,CP	16	○
MC14574	Quad Programmable Comparator	CL,CP	16	○
MC14575	Programmable Dual Op Amp/Dual Comparator	CL,CP	16	○
MC14580B	4 × 4 Multiport Register	AL,CL,CP	24	3-425
MC14581B	4-Bit Arithmetic Logic Unit	AL,CL,CP	24	3-430
MC14582B	Look-Ahead Carry Block	AL,CL,CP	16	3-435
MC14583B	Dual Schmitt Trigger	AL,CL,CP	16	3-439
MC14584B	Hex Schmitt Trigger	AL,CL,CP	14	3-445
MC14585B	4-Bit Magnitude Comparator	AL,CL,CP	16	3-448
MC14597B	8-Bit Bus Compatible Counter Latch	AL,CL,CP	16	3-452
MC14598B	8-Bit Bus Compatible Addressable Latch	AL,CL,CP	18	3-452
MC14599B	8-Bit Addressable Latch	AL,CL,CP	18	3-182
4734B	See MC14513B - Normally Pin for Pin Equivalent			
40014B	See MC14584B - Normally Pin for Pin Equivalent			
40085B	See MC14585B - Normally Pin for Pin Equivalent			
40097B	See MC14503B - Normally Pin for Pin Equivalent			
40101B	See MC14531B - Functionally Equivalent			
40106B	See MC14106B - Pin for Pin Equivalent			

○ See the CMOS Data Manual, Volume 2, Special Functions.

Device	Function	Suffix	Pins	Page
40108B	See MC14580B - Normally Pin for Pin Equivalent			
40160B	See MC14160B - Pin for Pin Equivalent			
40161B	See MC14161B - Pin for Pin Equivalent			
40162B	See MC14162B - Pin for Pin Equivalent			
40163B	See MC14163B - Pin for Pin Equivalent			
40174B	See MC14174B - Pin for Pin Equivalent			
40175B	See MC14175B - Pin for Pin Equivalent			
40181B	See MC14581B - Pin for Pin Equivalent			
40182B	See MC14582B - Pin for Pin Equivalent			
40192B	See MC14510B - Functionally Equivalent			
40193B	See MC14516B - Functionally Equivalent			
40194B	See MC14194B - Normally Pin for Pin Equivalent			
40208B	See MC14580B - Normally Pin for Pin Equivalent			
MC142100	4 × 4 Cross Point Switch	AL,CL,CP	16	●
MC144100	Duplex Mode 32-Segment LED Driver	P	24	○
MC144104	High Performance Remote Control Transmitter	P	24	○
MC144105	Remote Control Transmitter	P	20	○
MC144110	Hex D/A Converter	P	18	○
MC144111	Quad D/A Converter	P	14	○
MC144115	16-Segment LCD Driver	P	24	○
MC144117	4-Digit Duplex Mode LCD Decoder/Driver	P	24	○
MC144122	Remote Control Receiver	P	16	○
MC144124	High Performance Remote Control Receiver	P	24	○
MC144130	TV Stereo Decoder	P	28	○
MC145000	48-Segment Multiplexed LCD Driver (Master)	L,P	24	○
MC145001	44-Segment Multiplexed LCD Driver (Slave)	L,P	18	○
MC145026	Remote Control Encoder	L,P	16	○
MC145027	Remote Control Decoder	L,P	16	○
MC145028	Remote Control Decoder	L,P	16	○
MC145029	Remote Control Decoder	L,P	16	○
MC145040	Serial A/D Converter	L,P	20	○
MC145041	Serial A/D Converter	L,P	20	○
MC145100	4 × 4 Cross Point Switch	L,P	16	●
MC145104	PLL Frequency Synthesizer	P	16	○
MC145106	PLL Frequency Synthesizer	P	18	○
MC145107	PLL Frequency Synthesizer	P	16	○
MC145109	PLL Frequency Synthesizer	P	16	○
MC145112	PLL Frequency Synthesizer	P	18	○
MC145143	PLL Frequency Synthesizer	P	16	○
MC145144	4-Bit Data Bus Input PLL Frequency Synthesizer	L,P	16	○
MC145145	4-Bit Data Bus Input PLL Frequency Synthesizer	L,P	18	○
MC145146	4-Bit Data Bus Input PLL Frequency Synthesizer	L,P	20	○
MC145151	Parallel Input PLL Frequency Synthesizer	L,P	28	○

● See the Telecommunications Data Manual.
○ See the CMOS Data Manual, Volume 2, Special Functions.

Device	Function	Suffix	Pins	Page
MC145152	Parallel Input PLL Frequency Synthesizer	L,P	28	○
MC145155	Serial Input PLL Frequency Synthesizer	L,P	18	○
MC145156	Serial Input PLL Frequency Synthesizer	L,P	20	○
MC145157	Serial Input PLL Frequency Synthesizer	L,P	16	○
MC145158	Serial Input PLL Frequency Synthesizer	L,P	16	○
MC145159	Serial Input PLL Frequency Synthesizer	L,P	20	○
MC145414	Dual Tuneable Lowpass Sampled Data Filters	L,P	16	○ ●
MC145415	Dual Tuneable Linear Phase Low Pass Sampled Data Filters	L,P	16	●
MC145420	MDPSK Universal Digital-Loop Transceiver (4-Wire Master)	L	24	●
MC145422	MDPSK Universal Digital-Loop Transceiver (2-Wire Master)	L	22	●
MC145423	MDPSK Universal Digital-Loop Transceiver (2-Wire Master)	L	20	●
MC145425	MDSPK Universal Digital-Loop Transceiver (4-Wire Slave)	L	22	●
MC145426	MDPSK Universal Digital-Loop Transceiver (2-Wire Slave)	L	22	●
MC145428	Data Set Interface	L,P	20	●
MC145429	Telset Audio Interface	L,P	18	●
MC145431	Tuneable Lowpass/Bandpass Filter	L,P	16	●
MC145432	2600 Hz Tone Signalling Filter	L,P	18	●
MC145433	Tuneable Notch/Bandpass Filter	L,P	16	●
MC145440	Low Speed Modem Filter	L,P	18	●
MC145441	Low Speed Modem Filter	L,P	18	●
MC145445	300 Baud FSK Modem	L,P	22	●
MC145450	1200 Baud FSK Modem	L,P	22	●
MC146805E2	8-Bit Microprocessor, Expandable	L,P,Z	40	×
MC146805F2	8-Bit Single Chip Microcomputer	L,P,Z	28	×
MC146805G2	8-Bit Single Chip Microcomputer	L,P,Z	40	×
MC146818	Real-Time Clock/RAM	L,P,Z	24	×
MC146823	Parallel Interface	L,P,Z	40	×
MC1468705G2	8-Bit Single Chip Microcomputer with EPROM	L,P	40	×
MCM5101	256 × 4-Bit Static RAM	C,P	22	+
MCM14505	64 × 1-Bit Static RAM	AL,CL,CP	14	○
MCM14524	256 × 4-Bit ROM, See Note D	AL,CL,CP	16	○
MCM14537	256 × 1-Bit Static RAM	AL,CL,CP	16	○
MCM14552	64 × 4-Bit Static RAM	AL,CL,CP	24	○
MCM65116	2048 × 8-Bit Static RAM	C,P	24	+
MCM65147	4096 × 1-Bit Static RAM	C,P	18	+
MCM65256	32768 × 8-Bit ROM	P	28	+
MCM65516	2048 × 8-Bit Multiplexed Bus ROM	L,P	18	+
MCM144102	16 × 16-Bit Static RAM	P	8	○

× See the 8-Bit Microprocessors Data Manual.
\+ See the Memory Data Manual.
● See the Telecommunications Data Manual.
○ See the CMOS Data Manual, Volume 2, Special Functions.
Note D: Available only by special order.

Selection Guide by Function

Microprocessors/Peripherals ..... ×

Memories ..... § +

Special Functions:

Display Decoders/Drivers ..... ○
A/D, D/A Converters/Logic Functions ..... ○
Operational Amplifiers/Comparators ..... ○
Telecommunications Functions ..... ●
Remote Control Functions ..... ○
Radio/TV Functions ..... ○
Miscellaneous ..... ○
Phase-Locked Loops ..... ○

Device	Function	Page
NAND Gates		
MC14011B	Quad 2-Input NAND Gate	3-5
MC14011UB	Quad 2-Input NAND Gate	3-14
MC14093B	Quad 2-Input Schmitt Trigger	3-173
MC14023B	Triple 3-Input NAND Gate	3-5
MC14023UB	Triple 3-Input NAND Gate	3-14
MC14012B	Dual 4-Input NAND Gate	3-5
MC14012UB	Dual 4-Input NAND Gate	3-14
MC14068B	8-Input NAND Gate	3-5
See also MC14501UB and MC14572UB		
NOR Gates		
MC14001B	Quad 2-Input NOR Gate	3-5
MC14001UB	Quad 2-Input NOR Gate	3-14
MC14025B	Triple 3-Input NOR Gate	3-5
MC14025UB	Triple 3-Input NOR Gate	3-14
MC14000UB	Dual 3-Input NOR Gate Plus Inverter	3-2
MC14002B	Dual 4-Input NOR Gate	3-5
MC14002UB	Dual 4-Input NOR Gate	3-14
MC14078B	8-Input NOR Gate	3-5
See also MC14501UB and MC14572UB		
AND Gates		
MC14081B	Quad 2-Input AND Gate	3-5
MC14073B	Triple 3-Input AND Gate	3-5
MC14082B	Dual 4-Input AND Gate	3-5
See also MC14501UB		

× See the 8-Bit Microprocessors Data Manual.
\+ For large CMOS Memories see the Memory Data Manual.
§ For small CMOS Memories see the CMOS Data Manual, Volume 2, Special Functions.
○ See the CMOS Data Manual, Volume 2, Special Functions.
● See the Telecommunications Data Manual.

Device	Function	Page
OR Gates		
MC14071B	Quad 2-Input OR Gate	3-5
MC14075B	Triple 3-Input OR Gate	3-5
MC14072B	Dual 4-Input OR Gate	3-5
See also MC14501UB		
Complex Gates		
MC14070B	Quad Exclusive OR Gate	3-159
MC14077B	Quad Exclusive NOR Gate	3-159
MC14501UB	Triple Gate	3-222
MC14506UB	Dual Expandable AOI Gate	3-237
MC14519B	4-Bit And/Or Selector	3-278
MC14530B	Dual 5-Input Majority Logic Gate	3-313
MC14572UB	Hex Gate	3-422
Inverters/Buffers/Level Translators		
MC14007UB	Dual Complementary Pair Plus Inverter	3-24
MC14049UB	Hex Inverter/Buffer	3-131
MC14050B	Hex Buffer	3-131
MC14069UB	Hex Inverter	3-157
MC14502B	Strobed Hex Inverter/Buffer	3-226
MC14503B	Hex 3-State Buffer	3-230
MC14504B	Hex TTL or CMOS to CMOS Level Shifter	3-234
MC14584B	Hex Schmitt Trigger	3-445
See also MC14000UB		
Schmitt Triggers		
MC14093B	Quad 2-Input NAND Schmitt Trigger	3-173
MC14583B	Dual Schmitt Trigger	3-439
MC14106B	Hex Schmitt Trigger	3-188
MC14584B	Hex Schmitt Trigger	3-445
Flip-Flops/Latches		
MC14013B	Dual D Flip-Flop	3-36
MC14027B	Dual J-K Flip-Flop	3-82
MC14042B	Quad Latch	3-118
MC14043B	Quad NOR R-S Latch	3-122
MC14044B	Quad NAND R-S Latch	3-122
MC14076B	Quad D-Type Register	3-165
MC14175B	Quad D Flip-Flop	3-201
MC14508B	Dual 4-Bit Latch	3-242
MC14174B	Hex D Flip-Flop	3-197
MC14099B	8-Bit Addressable Latch	3-182
MC14597B	8-Bit Bus Compatible Counter/Latch	3-452
MC14598B	8-Bit Bus Compatible Addressable Latch	3-452
MC14599B	8-Bit Addressable Latch	3-182

Device	Function	Page
Shift Registers		
MC14035B	4-Bit Shift Register	3-109
MC14194B	4-Bit Universal Shift register	3-205
MC14015B	Dual 4-Bit Static Shift Register	3-44
MC14580B	4 × 4 Multiport Register	3-425
MC14014B	8-Bit Static Shift Register	3-40
MC14021B	8-Bit Static Shift Register	3-40
MC14034B	8-Bit Universal Bus Register	3-102
MC14094B	8-Bit Bus Compatible Shift/Store Latch	3-177
MC14006B	18-Bit Static Shift Register	3-20
MC14557B	1-to-64 Bit Variable Length Shift Register	3-384
MC14517B	Dual 64-Bit Static Shift Register	3-269
MC14562B	128-Bit Static Shift Register	3-398
Counters		
MC14024B	7-Stage Ripple Counter	3-76
MC14022B	Octal Counter/Divider	3-70
MC14017B	Decade Counter/Divider	3-56
MC14018B	Presettable Divide-By-N Counter	3-61
MC14160B	Synchronous Programmable Decade Counter	3-189
MC14162B	Synchronous Programmable Decade Counter	3-189
MC14534B	Real Time 5-Decade Counter	3-327
MC14029B	Binary/Decade Up/Down Counter	3-91
MC14020B	14-Bit Binary Counter	3-65
MC14040B	12-Bit Binary Counter	3-114
MC14060B	14-Bit Binary Counter and Oscillator	3-141
MC14161B	Synchronous Programmable 4-Bit Binary Counter	3-189
MC14163B	Synchronous Programmable 4-Bit Binary Counter	3-189
MC14516B	Binary Up/Down Counter	3-263
MC14520B	Dual Binary Up Counter	3-273
MC14521B	24-Stage Frequency Divider	3-283
MC14526B	Programmable Binary Divide-By-N Counter	3-289
MC14568B	Phase Comparator and Programmable Counters	3-408
MC14569B	Dual Programmable BCD/Binary Counter	3-418
MC14510B	BCD Up/Down Counter	3-247
MC14522B	Programmable BCD Divide-By-N Counter	3-289
MC14518B	Dual BCD Up Counter	3-273
MC14553B	3-Digit BCD Counter	3-371
Adders/Comparators		
MC14008B	4-Bit Full Adder	3-28
MC14032B	Triple Serial Adder (Positive Logic)	3-97
MC14038B	Triple Serial Adder (Negative Logic)	3-97
MC14560B	NBCD Adder	3-388
MC14561B	9's Complementer	3-392
MC14582B	Look Ahead Carry Block	3-435
MC14585B	4-Bit Magnitude Comparator	3-448

Device	Function	Page
Parity Generator/Checker		
MC14531B	12-Bit Parity Tree	3-318
ALU's/Rate Multipliers		
MC14527B	BCD Rate Multiplier	3-296
MC14554B	2 × 2-Bit Parallel Binary Multiplier	3-377
MC14581B	4-Bit Arithmetic Logic Unit	3-430
Encoders/Decoders		
MC14028B	BCD-to-Decimal/Binary-to-Octal Decoder	3-86
MC14419	2-of-8 Keypad-to-Binary encoder	3-214
MC14430	Input Address Encoder	3-218
MC14514B	4-Bit Latch/4-to-16 Line Decoder (High)	3-257
MC14515B	4-Bit Latch/4-to-16 Line Decoder (Low)	3-257
MC14532B	8-Bit Priority Encoder	3-321
MC14555B	Dual Binary to 1-of-4 Decoder	3-381
MC14556B	Dual Binary to 1-of-4 Decoder (Inverting)	3-381
MC145026	Remote Control Encoder	○
MC145027	Remote Control Decoder	○
MC145028	Remote Control Decoder	○
MC145029	Remote Control Decoder	○
Multiplexers/Demultiplexers/Bilateral Switches		
MC14016B	Quad Analog Switch/Multiplexer	3-50
MC14066B	Quad Analog Switch/Multiplexer	3-145
MC14053B	Triple 2-Channel Analog Multiplexer	3-135
MC14551B	Quad 2-Channel Analog Multiplexer	3-365
MC14052B	Dual 4-Channel Analog Multiplexer	3-135
MC14529B	Dual 4-Channel Analog Data Selector	3-307
MC14539B	Dual 4-Channel Data Selector/Multiplexer	3-348
MC14051B	8-Channel Analog Multiplexer	3-135
MC14512B	8-Channel Data Selector	3-253
MC14097B	Differential 8-Channel Analog Multiplexer	3-150
MC14067B	16-Channel Analog Multiplexer	3-150
MC14519B	4-Bit And/Or Selector	3-278
MC14007UB	Dual Complementary Pair Plus Inverter	3-24
MC14555B	Dual Binary to 1-of-4 Decoder	3-381
MC14556B	Dual Binary to 1-of-4 Decoder (Inverting)	3-381
Multivibrators/Oscillators/Timers		
MC14060B	14-Bit Binary Counter and Oscillator	3-141
MC14415	Quad Precision Timer/Driver	3-209
MC14521B	24-Stage Frequency Divider	3-283

○ See the CMOS Data Manuel, Volume 2, Special Functions.

Device	Function	Page
MC14528B	Dual Monostable Multivibrator	3-302
MC14536B	Programmable Timer	3-333
MC14538B	Dual Precision Monostable Multivibrator	3-340
MC14541B	Programmable Oscillator-Timer	3-352
MC14548B	Dual Monostable Multivibrator	3-358
MC14566B	Industrial Time-Base Generator	3-402

PLL Frequency Synthesizer

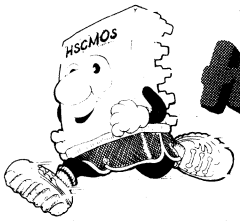
MC14046B	Phase-Locked Loop, See Note	3-126

Note: For other PLL Frequency Synthesizers, see CMOS Data Manual, Volume 2.

TABLE 3 — COUNTER SELECTOR

	Binary (Bits)	Octal	Decade	BCD	UP/ Down	Outputs	Carry Out/In	÷ Ratio	Preset/ Program	Reset/ Clear	On-chip Osc.
MC14017B	—	—	1	—	U	Q0-Q9	Out	—	—	Yes	—
MC14018B	5	—	—	—	U	$\overline{Q1}$-$\overline{Q5}$	—	2-10	Yes	Yes	—
MC14020B	14	—	—	—	U	Q1, Q4-Q14	—	—	—	Yes	—
MC14022B	—	1	—	—	U	Q0-Q7	Out	—	—	Yes	—
MC14024B	7	—	—	—	U	Q1-Q7	—	—	—	Yes	—
MC14029B	4#	—	—	1 #	U/D	Q0-Q3	Out/In	1-16 or 1-10	Yes	—	—
MC14040B	12	—	—	—	U	Q1-Q12	—	—	—	Yes	—
MC14060B	14	—	—	—	U	Q4-Q10 Q12-Q14	—	—	—	Yes	Yes
MC14160B	—	—	—	1	U	Q1-Q4	Out	1-10	Yes	Yes	—
MC14161B	4	—	—	—	U	Q1-Q4	Out	1-16	Yes	Yes	—
MC14162B	—	—	—	1	U	Q1-Q4	Out	1-10	Yes	Yes	—
MC14163B	4	—	—	—	U	Q1-Q4	Out	1-16	Yes	Yes	—
MC14510B	—	—	—	1	U/D	Q1-Q4	Out/In	1-10	Yes	Yes	—
MC14516B	4	—	—	—	U/D	Q0-Q3	Out/In	1-16	Yes	Yes	—
MC14518B	—	—	—	2×1	U	Q0-Q3	—	—	—	Yes	—
MC14520B	2×4	—	—	—	U	Q0-Q3	—	—	—	Yes	—
MC14521B	24	—	—	—	U	Q18-Q24	—	—	—	Yes	Yes
MC14522B	—	—	—	1	D	Q0-Q3	Out/In	1-10	Yes	Yes	—
MC14526B	4	—	—	—	D	Q0-Q3	Out/In	1-16	Yes	Yes	—
MC14534B	—	—	5	—	U	Q0-Q3*	Out	—	—	Yes	—
MC14553B	—	—	—	3	U	Q0-Q3*	Out	—	—	Yes	Yes
MC14568B	7	—	—	—	U	Q1	—	4, 16, 64 or 100	—	—	—
	4	—	—	—	U	—	Out	1-16	Yes	—	—
MC14569B	1#	—	—	1 #	U	—	In	1-10 or 1-16	Yes	—	—
	1#	—	—	1 #	U	Q	In	1-10 or 1-16	Yes	—	—

Selectable.
* Multiplexed Output.



HIGH SPEED CMOS

Introducing a new dimension in CMOS[1]

Motorola's new family of standard-logic High-Speed CMOS integrated circuits provides the designer with a complete series of functions which approaches the ideal in performance.

All of the present CMOS logic family features, including low power dissipation and high noise immunity, combine with LSTTL speeds, pinouts and drives to offer the marketplace a new dimension in CMOS standard logic.

- Guaranteed Propagation Delay — 15 ns for 74HC00
- Wide Operating Range — 2-6 V Recommended
- High Noise Immunity — Typically 45% of Supply Voltage
- Low Quiescent Power Dissipation
- Diode Protection — All Inputs
- High Fanout — 10 LSTTL Loads (4 mA Drive)
- Direct Pin Compatibility with LSTTL Parts (HCXXX or HCTXXX) and CMOS Parts (HC4XXX)
- Input Logic Compatible with CMOS Parts (HCXXX or HC4XXX) and/or LSTTL Parts (HCTXXX)
- Proven Reliability and Process

BASIC NUMBERING PARAMETERS

MC VV WWW XXXX Y

Example:

Motorola Circuit Identifier

Temperature Range
- 74 for Commercial Range (– 40°C to 85°C)
- 54 for Extended Range (–55°C to 125°C)

High-Speed CMOS Specification Identifier
- HC for Buffered High-Speed CMOS
- HCU for Unbuffered High-Speed CMOS*
- HCT for TTL Input Compatible CMOS*

Basic Device Type

Package Type
- N for Plastic (74 Series Only)
- J for Ceramic

*Not Available On All Devices

[1] For full information, see the CMOS Data Manual, Volume 3, High Speed CMOS

HIGH SPEED CMOS FUNCTION SELECTOR GUIDE

- Parts shown are functional equivalent *except* when preceded by an asterisk (*), indicating a suggested alternative
- Device numbers preceded by a "★" are new proprietary designs

High-Speed Device Number MC74/MC54	Function	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
GATES					
HC00	Quad 2-Input NAND Gate	LS00	4011	LS	14
HC02	Quad 2-Input NOR Gate	LS02	4001	LS	14
HC03	Quad 2-Input NAND with Open Drain Outputs	LS03	*4011	LS	14
HC08	Quad 2-Input AND Gate	LS08	4081	LS	14
HC10	Triple 3-Input NAND Gate	LS10	4023	LS	14
HC11	Triple 3-Input AND Gate	LS11	4073	LS	14
HC20	Dual 4-Input NAND Gate	LS20	4012	LS	14
HC27	Triple 3-Input NOR Gate	LS27	4025	LS	14
HC30	8-Input NAND Gate	LS30	4068	LS	14
HC32	Quad 2-Input OR Gate	LS32	4071	LS	14
HC51	2-Wide, 2-Input/2-Wide, 3-Input AND-OR-INVERT Gates	LS51	*4506	LS	14
★HC58	2-Wide, 2-Input/2-Wide, 3-Input AND-OR Gates	*LS51	*4506		14
HC86	Quad 2-Input Exclusive OR Gate	LS86	4070	LS	14
HC132	Quad 2-Input Schmitt-Trigger NAND Gate	LS132	4093	LS	14
HC133	13-Input NAND Gate	LS133		LS	16
HC266	Quad 2-Input Exclusive NOR Gate (Non Open Drain)	LS266	4077	LS/CMOS	14
HC4002	Dual 4-Input NOR Gate	*LS25	4002	CMOS	14
HC4075	Triple 3-Input OR Gate		4075	CMOS	14
HC4078	8-Input NOR Gate		4078	CMOS	14
BUFFERS / INVERTERS					
HC04	Hex Inverter	LS04	*4069	LS/CMOS	14
HCU04	Hex Unbuffered Inverter	LS04	4069	LS/CMOS	14
HC14	Hex Schmitt-Trigger Inverter	LS14	4584	LS/CMOS	14
HC240/ HCT240	Octal Buffer/Line Driver/Line Receiver, 3-State, Inverting Output	LS240		LS	20
HC241/ HCT241	Octal Buffer/Line Driver/Line Receiver, 3-State	LS241		LS	20
HC244/ HCT244	Octal Buffer/Line Driver/Line Receiver, 3-State	LS244		LS	20
HC365	Hex 3-State Bus Driver with Common 2-Input NOR Enable	LS365A		LS	16
HC366	Hex 3-State Bus Driver with Common 2-Input NOR Enable, Inverting Output	LS366A		LS	16
HC367	Hex 3-State Bus Driver with Separate 2-Bit and 4-Bit Sections	LS367A	4503	LS/CMOS	16
HC368	Hex 3-State Bus Driver with Separate 2-Bit and 4-Bit Sections, Inverting Output	LS368A		LS	16
HC540	Octal Buffer/Line Driver/Line Receiver, 3-State Inverting Outputs	LS540		LS	20
HC541	Octal Buffer/Line Driver/Line Receiver, 3-State	LS541		LS	20
HC4049	Hex Inverting Buffer		4049	CMOS	16
HC4050	Hex Buffer		4050	CMOS	16

High-Speed Device Number MC74/MC54	Function	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
SCHMITT TRIGGERS					
HC14	Hex Schmitt-Trigger Inverter	LS14	4584	LS/CMOS	14
HC132	Quad 2-Input Schmitt-Trigger NAND Gate	LS132	4093	LS	14
BUS TRANSCEIVERS					
HC242	Quad Bus Transceiver, 3-State, Inverting Output	LS242		LS	14
HC243	Quad Bus Transceiver, 3-State	LS243		LS	14
HC245/ HCT245	Octal Bus Transceiver, 3-State	LS245		LS	20
HC640	Octal Bus Transceiver, 3-State	LS640		LS	20
HC643	Octal Bus Transceiver, 3-State	LS643		LS	20
HC646	Octal Bus Transceiver and Register, 3-State	LS646		LS	24
HC648	Octal Bus Transceiver and Register, 3-State, Inverting Output	LS648		LS	24
ARITHMETIC CIRCUITS					
HC85	4-Bit Magnitude Comparator	LS85	*4585	LS	16
HC181	4-Bit Arithmetic Logic Unit	LS181	4581	LS/CMOS	24
HC182	Carry Lookahead Generator	LS182	4582	LS/CMOS	16
HC280	9-Bit Odd/Even Parity Generator/Checker	LS280	*4531	LS	14
HC283	4-Bit Binary Full Adder with Fast Carry	LS283	4008	LS	16
HC888	8-Bit Equality Comparator				20
HC4560	NBCD Adder		4560	CMOS	16
MISCELLANEOUS					
HC292	Programmable Frequency Divider/ Digital Timer	LS292		LS	16
HC294	Programmable Frequency Divider/ Digital Timer	LS294		LS	16
HC4046	Phase-Locked Loop	*LS297	4046	CMOS	16
FLIP-FLOPS / LATCHES					
HC73	Dual J-K Flip-Flop with Reset	LS73A	*4027	LS	14
HC74	Dual D-Type Flip-Flop with Set and Reset, Positive-Edge Triggered	LS74A	4013	LS	14
HC75	4-Bit D-Type Latch	LS75	*4042	LS	16
HC76	Dual J-K Flip-Flop with Set and Reset	LS76A	*4027	LS	16
HC107	Dual J-K Flip-Flop with Reset	LS107A	4027	LS	14
HC109	Dual J-K Flip-Flop with Set and Reset, Positive-Edge Triggered	LS109A	*4027	LS	16
HC112	Dual J-K Flip-Flop with Set and Reset, Negative-Edge Triggered	LS112A	*4027	LS	16
HC113	Dual J-K Flip-Flop with Set, Negative-Edge Triggered	LS113	*4027	LS	14
HC174	Hex D-Type Flip-Flop with Common Clock and Reset	LS174	4174	LS/CMOS	16
HC175	Quad D-Type Flip-Flop	LS175	4175	LS/CMOS	16
HC259	8-Bit Addressable Latch	LS259	*4099	LS	16
HC273	Octal D-Type Flip-Flop with Common Clock/Reset	LS273	*4175	LS	20
HC373/ HCT373	Octal D-Type Transparent Latch, 3-State	LS373		LS	20
HC374/ HCT374	Octal D-Type Flip-Flop, 3-State	LS374		LS	20
HC533	Octal D-Type Transparent Latch, 3-State Inverting Output	LS533		LS	20

High-Speed Device Number MC74/MC54	Function	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
FLIP-FLOPS/LATCHES (continued)					
HC534	Octal D-Type Flip-Flop, 3-State, Inverting Output	LS534		LS	20
HC563	Octal Transparent Latch, 3-State, Inverting Output	LS576		LS	20
HC564	Octal D-Type Flip-Flop, 3-State, Inverting Output	LS580		LS	20
HC573	Octal Transparent Latch, 3-State	LS573		LS	20
HC574	Octal D-Type Flip-Flop, 3-State	LS574		LS	20
SHIFT REGISTERS					
HC164	8-Bit Serial Input/Parallel Output Shift Register	LS164	*4034	LS	14
HC165	8-Bit Serial or Parallel Input/Serial Output Shift Register	LS165	*4021	LS	16
HC173	4-Bit D-Type Register, 3-State	LS173	4076	LS/CMOS	16
HC194	4-Bit Bidirectional Universal Shift Register	LS194A	4194	LS/CMOS	16
HC195	4-Bit Universal Shift Register	LS195A	*4035	LS	16
HC299	8-Bit Universal Shift/Store Register, 3-State	LS299	*4094	LS	20
★HC589	8-Bit Parallel-to-Serial Shift Register with Input Latches, 3-State	*LS597	*4014 or *4021		16
HC595	8-Bit Serial-to-Parallel Shift Register, 3-State	LS595	*4034	LS	16
HC597	8-Bit Parallel-to-Serial Shift Register with Input Latches	LS597	*4014 or *4021	LS	16
COUNTERS					
HC160	Programmable Decade Counter, Asynchronous Clear	LS160A	4160	LS/CMOS	16
HC161	Programmable 4-Bit Binary Counter, Asynchronous Clear	LS161A	4161	LS/CMOS	16
HC162	Programmable Decade Counter, Synchronous Clear	LS162A	4162	LS/CMOS	16
HC163	Programmable 4-Bit Binary Counter, Synchronous Clear	LS163A	4163	LS/CMOS	16
HC192	Presettable BCD Decade Up/Down Counter	LS192	4510	LS	16
HC193	Presettable 4-Bit Binary Up/Down Counter	LS193	4516	LS	16
HC390	Dual Decade Counter	LS390	*4518	LS	16
HC393	Dual 4-Bit Binary Counter	LS393	*4520	LS	14
HC4017	Decade Counter/Divider		4017	CMOS	16
HC4020	14-Stage Binary Ripple Counter		4020	CMOS	16
HC4024	7-Stage Binary Ripple Counter		4024	CMOS	14
HC4040	12-Stage Binary Ripple Counter		4040	CMOS	16
HC4060	14-Stage Binary Ripple Counter with Oscillator		4060	CMOS	16
MONOSTABLE MULTIVIBRATORS					
HC123	Dual Retriggerable Monostable Multivibrator	LS123	*4538 or *4528	LS	16
HC221	Dual Monostable Multivibrator	LS221	*4538 or *4528	LS	16
HC423	Dual Monostable Multivibrator	LS423	*4538 or *4528	LS	16
HC4538	Dual Precision Retriggerable/Resettable Monostable Multivibrator	*LS221	4538	CMOS	16

High-Speed Device Number MC74/MC54	Function	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
DECODERS/ENCODERS/DISPLAY DRIVERS					
HC42	BCD to 1-of-10 Decoder	LS42	*4028	LS	16
HC137	1-of-8 Decoder/Demultiplexer with Latched Inputs, Inverting Output	LS137	*4028	LS	16
HC138/ HCT138	1-of-8 Decoder/Demultiplexer	LS138	*4028	LS	16
HC139	Dual 1-of-4 Decoder (Active-Low Outputs)	LS139	4555	LS/CMOS	16
HC147	10-to-4 Priority Encoder	LS147	*4532	LS	16
HC154	4-to-16 Decoder	LS154	*4514	LS	24
HC237	1-of-8 Decoder/Demultiplexer with Latched Inputs	*LS137	*4028		16
HC4511	BCD-to-7-Segment Latch/Decoder/Driver	*(LS46-LS49)	4511	LS/CMOS	16
HC4514	4-Bit Latch/4-to-16 Line Decoder		4514	CMOS	24
HC4543	BCD-to-7 Segment Latch/Decoder/Driver for Liquid-Crystal Displays	*(LS46-LA49)	4543	CMOS	16
BUS-COMPATIBLE DEVICES					
HC173	4-Bit D-Type Register, 3-State	LS173	4076	LS/CMOS	16
HC240/ HCT240	Octal Buffer/Line Driver/Line Receiver, 3-State, Inverting Output	LS240		LS	20
HC241/ HCT241	Octal Buffer/Line Driver/Line Receiver, 3-State	LS241		LS	20
HC242	Quad 3-State Bus Transceiver, Inverting Output	LS242		LS	14
HC243	Quad 3-State Bus Transceiver	LS243		LS	14
HC244/ HCT244	Octal Buffer/Line Driver/Line Receiver, 3-State	LS244		LS	20
HC245/ HCT245	Octal Bus Transceiver, 3-State	LS245		LS	20
HC251	8-Input Multiplexer, 3-State	LS251	*4512	LS	16
HC253	Dual 4-Input Multiplexer, 3-State	LS253	*4539	LS/CMOS	16
HC257	Quad 2-Input Data Selector/Multiplexer, 3-State	LS257	*4519	LS	16
HC299	8-Bit Universal Shift/Store Register, 3-State	LS299	*4094	LS	20
HC354	8-Input Multiplexer, 3-State	LS354	*4512	LS	20
HC356	8-Input Multiplexer, 3-State	LS356	*4512	LS	20
HC365	Hex 3-State Bus Driver with Common 2-Input NOR Enable	LS365A		LS	16
HC366	Hex 3-State Bus Driver with Common 2-Input NOR Enable, Inverting Output	LS366A		LS	16
HC367	Hex 3-State Bus Driver with Separate 2-Bit and 4-Bit Sections	LS367A	4503	LS/CMOS	16
HC368	Hex 3-State Bus Driver with Separate 2-Bit and 4-Bit Sections, Inverting Output	LS368A		LS	16
HC373/ HCT373	Octal Transparent Latch, 3-State	LS373		LS	20
HC374/ HCT374	Octal D-Type Flip-Flop, 3-State	LS374		LS	20
HC533	Octal D-Type Transparent Latch, 3-State, Inverting Output	LS533		LS	20

High-Speed Device Number MC74/MC54	Function	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
BUS-COMPATIBLE DEVICES (continued)					
HC534	Octal D-Type Flip-Flop, 3-State, Inverting Output	LS534		LS	20
HC540	Octal Buffer/Line Driver/Line Receiver, 3-State Inverting Outputs	LS540		LS	20
HC541	Octal Buffer/Line Driver/Line Receiver, 3-State	LS541		LS	20
HC563	Octal Transparent Latch, 3-State, Inverting Output	LS576		LS	20
HC564	Octal D-Type Flip-Flop, 3-State, Inverting Output	LS580		LS	20
HC573	Octal Transparent Latch, 3-State	LS573		LS	20
HC574	Octal D-Type Flip-Flop, 3-State	LS574		LS	20
★HC589	8-Bit Parallel-to-Serial Shift Register with Input Latches, 3-State	*LS597	*4014 or 4021		16
HC595	8-Bit Serial-to-Parallel Shift Register, 3-State	LS595	*4034	LS	16
HC640	Octal Bus Transceiver, 3-State	LS640		LS	20
HC643	Octal Bus Transceiver, 3-State	LS643		LS	20
HC646	Octal Bus Transceiver and Register, 3-State	LS646		LS	24
HC648	Octal Bus Transceiver and Register, 3-State	LS648		LS	24
TTL INPUT COMPATIBLE DEVICES					
HCT138	1-of-8 Decoder/Demultiplexer	LS138	*4028	LS	16
HCT240	Octal Buffer/Line Driver/Line Receiver, 3-State, Inverting Output	LS240		LS	20
HCT241	Octal Buffer/Line Driver/Line Receiver, 3-State	LS241		LS	20
HCT244	Octal Buffer/Line Driver/Line Receiver, 3-State	LS244		LS	20
HCT245	Octal Bus Transceiver, 3-State	LS245		LS	20
HCT373	Octal D-Type Transparent Latch, 3-State	LS373		LS	20
HCT374	Octal D-Type Flip-Flop, 3-State	LS374		LS	20
MULTIPLEXERS (ANALOG AND DIGITAL)					
HC151	8-Channel Digital Multiplexer	LS151	*4512	LS	16
HC153	Dual 4-Channel Digital Multiplexer	LS153	4539	LS/CMOS	16
HC157	Quad 2-Input Data Selector/Multiplexer	LS157	*4519	LS	16
HC158	Quad 2-Input Data Selector/Multiplexer, Inverting Output	LS158		LS	16
HC251	8-Input Multiplexer, 3-State	LS251	*4512	LS	16
HC253	Dual 4-Input Multiplexer, 3-State	LS253	*4539	LS/CMOS	16
HC257	Quad 2-Input Data Selector/Multiplexer, 3-State	LS257	*4519	LS	16
HC298	Quad 2-Input Multiplexer with Storage	LS298		LS	16
HC354	8-Input Multiplexer, 3-State	LS354	*4512	LS	20
HC356	8-Input Multiplexer, 3-State	LS356	*4512	LS	20
HC4016	Quad Analog Switch		4016	CMOS	14
HC4051	8-Channel Analog Multiplexer/Demultiplexer		4051	CMOS	16
HC4052	8-Channel Analog Multiplexer/Demultiplexer		4052	CMOS	16
HC4053	8-Channel Analog Multiplexer/Demultiplexer		4053	CMOS	16
HC4066	Quad Analog Switch		4066	CMOS	14

High-Speed Device Number MC74/MC54	Function	Functional Equivalent LSTTL Device 74/54	Functional Equivalent CMOS Device MC1XXXX or CDXXXX	Direct Pin Compatibility	Number of Pins
MULTIPLEXERS (ANALOG AND DIGITAL) (continued)					
★HC4316	Quad Analog Switch with Level Translator		*4016		16
★HC4351	Quad Analog Multiplexer/Demultiplexer with Latched Select Inputs		*4051		18
★HC4352	Dual 4-Channel Analog Multiplexer/Demultiplexer with Latched Select Inputs		*4052		18
★HC4353	Triple 2-Channel Analog Multiplexer/Demultiplexer with Latched Select Inputs		*4053		18

1 MOS GATE ARRAYS

Motorola is introducing a range of 3μ High-Density CMOS Gate Arrays, with gate counts from 600 to 6000 gates. 4 parts will be introduced in 1983 and 2 more in 1984.
Key features of the range are:

- System speed similar to LSTTL
- Low power consumption
- Option of CMOS or LSTTL compatible inputs
- Output drive capability of 10 LSTTL loads
- Simple design procedure

Design of the gate arrays is a very simple procedure, using the Motorola CAD system. This system has all of the design aids necessary for the designer to simulate his design, automatically place and route the circuit, complete an accurate timing analysis and prepare a test program for testing the finished product.

The CAD system is an improved version of the system which has been successfully used for several years for the design of Motorola ECL and TTL Macrocell Arrays. The same design system can be used for all three technologies. The designer needs no knowledge of I.C. design or computer programming to design a Motorola Gate Array.

The designer works in his own office using a simple printing terminal with Modem or acoustic coupler, and connects to the Motorola computer by dialling the nearest Motorola Sales Office. From here, connection to the Motorola computer in Phoenix, Arizona, is over the Motorola worldwide communications network.

Using a comprehensive library of SSI and MSI functions, the designer describes his circuit as a list of functions and interconnections which then becomes the input to the CAD system.

Future plans include the addition of analog and memory functions, and using a 2μ HCMOS process which will increase speed.

For further information on the Motorola range of CMOS, TTL and ECL Arrays, contact your nearest Motorola Sales Office.

B-Series Family Data

2

B AND UB SERIES CMOS FAMILY DATA

The CMOS Devices in this volume which have a B or UB suffix meet the minimum values for the industry-standardized* family specification. These standardized values are shown in the Maximum Ratings and Electrical Characteristics Tables. In addition to a standard minimum specification for characteristics the B/UB devices feature:

- **3–18 volt operational limits**
- **Capable of driving two low-power TTL loads, one low-power Schottky TTL load, or two HTL loads over the rated temperature range**
- **Maximum input current of ±1 μA at 15 volt power supply over the temperature range**
- **Parameters specified at 5.0, 10, and 15 volt supply**
- **Noise margins of 1.0 V min @ 5.0 V supply**
  2.0 V min @ 10 V supply
  2.5 V min @ 15 V supply

The industry-standardized maximum ratings and recommended operating range are shown at the bottom of this page. Limits for the static characteristics are shown in two formats: Table 1 is in the industry format and Table 2 is in the equivalent Motorola format. The Motorola format is used throughout this data book. Additional specification values are shown on the individual data sheets.

Switching characteristics for the B and UB series devices are specified under the following conditions:

Load Capacitance, C_L, of 50 pF
Load Resistance, R_L, of 200 K Ω
Input pulse voltage equal to $+V_{DD}$ supply voltage
Input pulse rise and fall times of 20 ns
Propagation Delay times measured from 50% point of input voltage to 50% point of output voltage
Three different supply voltages: 5, 10, and 15 V

Exceptions to the B and UB Series Family Specification

There are a number of devices which have a B or UB suffix whose input and/or outputs vary somewhat from the family specification because of functional requirements. Some categories of notable exceptions are:

Devices with specialized outputs on the chip, such as NPN emitter-follower drivers or transmission gates, do not meet output specifications.

Devices with specialized inputs, such as oscillator inputs, have unique input specifications.

Input Voltage

The input voltage specification is interpreted as the worst-case input voltage to produce an output level of "1" or "0". The "1" or"0" output level is defined as a deviation from the supply (V_{DD}) and ground (V_{SS}) levels. For a 5.0 V supply, this deviation is 0.5 V; for a 10 V supply, 1.0 V; and for 15 V, 1.5 V. As an example, in a device operating at a 5.0 V supply, the device with the input starting at ground is guaranteed to switch on or before 3.5 V and not to switch up to 1.5 V. Switching and not switching are defined as within 0.5 V of the ideal output level for the example with a 5.0 V supply. The actual switching level referred to the input is between 1.5 V and 3.5 V.

Noise Margin

The values for input voltage and the given defined output deviation lead to minimum noise margins of 1.0 V, 2.0 V, and 2.5 V for a 5.0 V, 10 V, and 15 V supply, respectively.

Output Drive Current

Devices in the B Series are capable of sinking a minimum of 0.36 mA over the temperature range with a 5.0 V supply. This value guarantees that these CMOS devices will drive one Schottky low-power TTL input.

B Series vs UB CMOS

The primary difference between B series and UB series devices is that UB series gates and inverters are constructed with a single inverting stage between input and output. The decreased gain caused by using a single stage results in less noise immunity and a transfer characteristic that is less ideal.

The decreased gain is quite useful when CMOS Gates and inverters are used in a "Linear" mode to form oscillators, monostables or amplifiers. The decreased gain results in increased stability and a "cleaner" output waveform. In addition to linear operation, the UB gates and inverters offer an increase in speed since only a single stage is involved.

The B series, UB CMOS, and devices with no suffix can be used interchangeably in digital circuits that interface to other CMOS devices.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING RANGE

DC Supply Voltage	V_{DD}	+3.0 to +15	Vdc

*Specifications coordinated by EIA/JEDEC Solid-State Products Council.

TABLE 1 – EIA/JEDEC FORMAT FOR CMOS INDUSTRY B AND UB SERIES SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

PARAMETER		TEMP RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS						UNITS
					T_{LOW}*		+ 25°C		T_{HIGH}*		
					Min	Max	Min	Max	Min	Max	
I_{DD}	Quiescent Device Current		5			0.25		0.25		7.5	
		Mil	10	$V_{in} = V_{SS}$ or V_{DD}		0.5		0.5		15	µAdc
	GATES		15			1.0		1.0		30	
			5			1.0		1.0		7.5	
		Comm	10	All valid input combinations		2.0		2.0		15	µAdc
			15			4.0		4.0		30	
			5			1.0		1.0		30	
		Mil	10	$V_{IN} = V_{SS}$ or V_{DD}		2.0		2.0		60	µAdc
			15			4.0		4.0		120	
	BUFFERS, FLIP-FLOPS		5			4		4.0		30	
		Comm	10	All valid input combinations		8		8.0		60	µAdc
			15			16		16.0		120	
			5			5		5		150	
		Mil	10	$V_{IN} = V_{SS}$ or V_{DD}		10		10		300	µAdc
			15			20		20		600	
	MSI		5			20		20		150	
		Comm	10	All valid input combinations		40		40		300	µAdc
			15			80		80		600	
V_{OL}	Low-Level Output Voltage		5			0.05		0.05		0.05	
		All	10	$V_{IN} = V_{SS}$ or V_{DD}		0.05		0.05		0.05	Vdc
			15	$\|I_O\| < 1\mu A$		0.05		0.05		0.05	
V_{OH}	High-Level Output Voltage		5		4.95		4.95		4.95		
		All	10	$V_{IN} = V_{SS}$ or V_{DD}	9.95		9.95		9.95		Vdc
			15	$\|I_O\| < 1\mu A$	14.95		14.95		14.95		
V_{IL}	Input Low Voltage # B Types	All	5	$V_O = 0.5V$ or 4.5V		1.5		1.5		1.5	
			10	$V_O = 1.0V$ or 9.0V		3.0		3.0		3.0	Vdc
			15	$V_O = 1.5V$ or 13.5V $\|I_O\| < 1\mu A$		4.0		4.0		4.0	
V_{IL}	Input Low Voltage # UB Types	All	5	$V_O = 0.5V$ or 4.5V		1.0		1.0		1.0	
			10	$V_O = 1.0V$ or 9.0V		2.0		2.0		2.0	Vdc
			15	$V_O = 1.5V$ or 13.5V $\|I_O\| < 1\mu A$		2.5		2.5		2.5	
V_{IH}	Input High Voltage # B Types	All	5	$V_O = 0.5V$ or 4.5V	3.5		3.5		3.5		
			10	$V_O = 1.0V$ or 9.0V	7.0		7.0		7.0		Vdc
			15	$V_O = 1.5V$ or 13.5V $\|I_O\| < 1\mu A$	11.0		11.0		11.0		
V_{IH}	Input High Voltage # UB Types	All	5	$V_O = 0.5V$ or 4.5V	4.0		4.0		4.0		
			10	$V_O = 1.0V$ or 9.0V	8.0		8.0		8.0		Vdc
			15	$V_O = 1.5V$ or 13.5V $\|I_O\| < 1\mu A$	12.5		12.5		12.5		
I_{OL}	Output Low (Sink) Current		5	$V_O = 0.4V$, $V_{IN} = 0$ or 5V	0.64		0.51		0.36		
		Mil	10	$V_O = 0.5V$, $V_{IN} = 0$ or 10V	1.6		1.3		0.9		mAdc
			15	$V_O = 1.5V$, $V_{IN} = 0$ or 15V	4.2		3.4		2.4		
			5	$V_O = 0.4V$, $V_{IN} = 0$ or 5V	0.52		0.44		0.36		
		Com	10	$V_O = 0.5V$, $V_{IN} = 0$ or 10V	1.3		1.1		0.9		mAdc
			15	$V_O = 1.5V$, $V_{IN} = 0$ or 15V	3.6		3.0		2.4		

TABLE 1 – Continued

ELECTRICAL CHARACTERISTICS

PARAMETER		TEMP RANGE	V_{DD} (Vdc)	CONDITIONS	LIMITS						UNITS
					T_{LOW}*		+ 25°C		T_{HIGH}*		
					Min	Max	Min	Max	Min	Max	
I_{OH}	Output High (Source) Current	Mil	5	V_O = 4.6V, V_{IN} = 0 or 5V	-0.25		-0.2		-0.14		mAdc
			10	V_O = 9.5V, V_{IN} = 0 or 10V	-0.62		-0.5		-0.35		
			15	V_O = 13.5V, V_{IN} = o or 15V	-1.8		-1.5		-1.1		
		Com	5	V_O = 4.6V, V_{IN} = 0 or 5V	-0.2		-0.16		-0.12		mAdc
			10	V_O = 9.5V, V_{IN} = 0 or 10V	-0.5		-0.4		-0.3		
			15	V_O = 13.5V V_{IN} = 0 or 15V	-1.4		-1.2		-1.0		
I_{IN}	Input Current	Mil	15	V_{IN} = 0 or 15V		±0.1		±0.1		±1.0	µAdc
		Comm	15	V_{IN} = 0 or 15V		±0.3		±0.3		±1.0	µAdc
I_{oz}	3-State Output Leakage Current	Mil	15	V_{IN} = 0 or 15V		±0.4		±0.4		±12	µAdc
		Comm	15	V_{IN} = 0 or 15V		±1.6		±1.6		±12	µAdc
C_{IN}	Input Capacitance per unit load	All	–	Any Input				7.5			pF

*T_{LOW} = -55°C for Military temperature range device, -40°C for Commercial temperature range device.
T_{HIGH} = +125°C for Military temperature range device, +85°C for Commercial temperature range device.
#Applies for Worst Case input combinations.

TABLE 2 – MOTOROLA FORMAT FOR CMOS INDUSTRY B AND UB SERIES SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}*		25°C		T_{high}*		Unit
				Min	Max	Min	Max	Min	Max	
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0			10	–	0.05	–	0.05	–	0.05	
			15	–	0.05	–	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}			10	9.95	–	9.95	–	9.95	–	
			15	14.95	–	14.95	–	14.95	–	
Input Voltage # B Types	"0" Level	V_{IL}								Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.5	–	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	–	3.0	–	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	4.0	–	4.0	–	4.0	
	"1" Level	V_{IH}								Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	3.5	–	3.5	–	3.5	–	
(V_O 1.0 or 9.0 Vdc)			10	7.0	–	7.0	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	11.0	–	11.0	–	11.0	–	
Input Voltage # UB Types	"0" Level	V_{IL}								Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.0	–	1.0	–	1.0	
(V_O = 9.0 or 1.0 Vdc)			10	–	2.0	–	2.0	–	2.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	2.5	–	2.5	–	2.5	
	"1" Level	V_{IH}								Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	4.0	–	4.0	–	4.0	–	
(V_O = 1.0 or 9.0 Vdc)			10	8.0	–	8.0	–	8.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	12.5	–	12.5	–	12.5	–	

TABLE 2 – Continued

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}*		25°C		T_{high}*		Unit
				Min	Max	Min	Max	Min	Max	
Output Drive Current (AL) B Gates		I_{OH}								mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-1.2	–	-1.0	–	-0.7	–	
(V_{OH} = 4.6 Vdc)			5.0	-0.25	–	-0.2	–	-0.14	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	–	-0.35	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	–	0.51	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	–	1.3	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	–	2.4	–	
Output Drive Current (CL/CP) B Gates		I_{OH}								mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-1.0	–	-0.8	–	-0.6	–	
(V_{OH} = 4.6 Vdc)			5.0	-0.2	–	-0.16	–	-0.12	–	
(V_{OH} = 9.5 Vdc)			10	-0.5	–	-0.4	–	-0.3	–	
(V_{OH} = 13.5 Vdc)			15	-1.4	–	-1.2	–	-1.0	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.52	–	0.44	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.3	–	1.1	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	3.6	–	3.0	–	2.4	–	
Output Drive Current (AL) UB Gates		I_{OH}								mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-1.2	–	-1.0	–	-0.7	–	
(V_{OH} = 4.6 Vdc)			5.0	-0.25	–	-0.2	–	-0.14	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	–	-0.35	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	–	0.51	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	–	1.3	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	–	2.4	–	
Output Drive Current (CL/CP) UB Gates		I_{OH}								mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-1.0	–	-0.8	–	-0.6	–	
(V_{OH} = 4.6 Vdc)			5.0	-0.2	–	-0.16	–	-0.12	–	
(V_{OH} = 9.5 Vdc)			10	-0.5	–	-0.4	–	-0.3	–	
(V_{OH} = 13.5 Vdc)			15	-1.4	–	-1.2	–	-1.0	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.52	–	0.44	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.3	–	1.1	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	3.6	–	3.0	–	2.4	–	
Output Drive Current (AL) Other Devices		I_{OH}								mAdc
(V_{OH} = 4.6 Vdc)	Source		5.0	-0.25	–	-0.2	–	-0.14	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	–	-0.35	–	
(V_{OH} = 13.5 Vdc)			15	-1.8	–	-1.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	–	0.51	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	–	1.3	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	–	2.4	–	
Output Drive Current (CL/CP) Other Devices		I_{OH}								mAdc
(V_{OH} = 4.6 Vdc)	Source		5.0	-0.2	–	-0.12	–	-0.12	–	
(V_{OH} = 9.5 Vdc)			10	-0.5	–	-0.4	–	-0.3	–	
(V_{OH} = 13.5 Vdc)			15	-1.4	–	-1.2	–	-1.0	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.52	–	0.44	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.3	–	1.1	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	3.6	–	3.0	–	2.4	–	
Input Current (AL Device)		I_{in}	15	–	±0.1	–	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)		I_{in}	15	–	±0.3	–	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	7.5	–	–	pF
Gate Quiescent Current (Per Package)	(AL Device)	I_{DD}	5.0	–	0.25	–	0.25	–	7.5	μAdc
			10	–	0.5	–	0.5	–	15	
			15	–	1.0	–	1.0	–	30	
	(CL/CP Device)	I_{DD}	5.0	–	1.0	–	1.0	–	7.5	μAdc
			10	–	2.0	–	2.0	–	15	
			15	–	4.0	–	4.0	–	30	

TABLE 2 – Continued

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}*		25°C		T_{high}*		Unit
				Min	Max	Min	Max	Min	Max	
Flip-Flop and Buffer Quiescent Current (Per Package)	(AL Device)	I_{DD}	5.0	–	1.0	–	1.0	–	30	μAdc
			10	–	2.0	–	2.0	–	60	
			15	–	4.0	–	4.0	–	120	
	(CL/CP Device)	I_{DD}	5.0	–	4.0	–	4.0	–	30	μAdc
			10	–	8.0	–	8.0	–	60	
			15	–	16	–	16	–	120	
MSI Quiescent Current (Per Package)	(AL Device)	I_{DD}	5.0	–	5.0	–	5.0	–	150	μAdc
			10	–	10	–	10	–	300	
			15	–	20	–	20	–	600	
	(CL/CP Device)	I_{DD}	5.0	–	20	–	20	–	150	μAdc
			10	–	40	–	40	–	300	
			15	–	80	–	80	–	600	
LSI Quiescent Current		I_{DD}		See Individual Data Sheets.						

* T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

Data Sheets

3

MOTOROLA

MC14000UB

DUAL 3-INPUT "NOR" GATE PLUS INVERTER

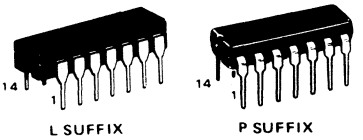
The MC14000UB dual 3-input NOR gate plus inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4000UB

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 3-INPUT "NOR" GATE PLUS INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

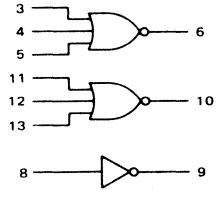
ORDERING INFORMATION

MC14XXXUB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

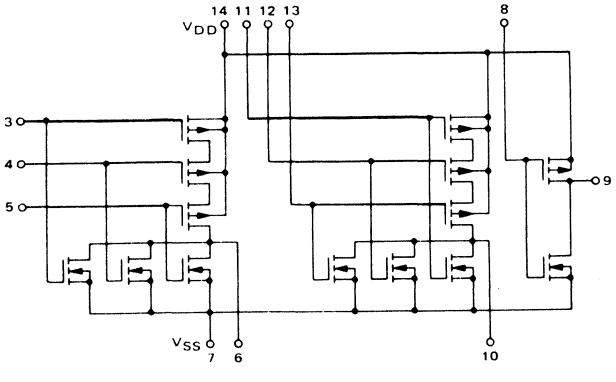
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM

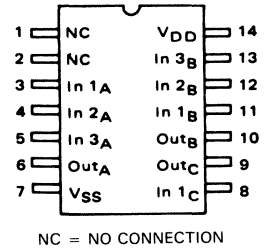


V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC



PIN ASSIGNMENT



NC = NO CONNECTION

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5 Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0 Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15		±0.1		±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15		±0.3		±0.00001	±0.3		±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–			5.0	7.5			pF
Quiescent Current (AL Device)	I_{DD}	5.0		0.25		0.0005	0.25		7.5	µAdc
(Per Package)		10		0.50		0.0010	0.50		15.0	
		15		1.00		0.0015	1.00		30.0	
Quiescent Current (CL/CP Device)	I_{DD}	5.0		1.0		0.0005	1.0		7.5	µAdc
(Per Package)		10		2.0		0.0010	2.0		15.0	
		15		4.0		0.0015	4.0		30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}/N							µAdc
		10	I_T = (0.6 µA/kHz) f + I_{DD}/N							
		15	I_T = (0.8 µA/kHz) f + I_{DD}/N							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst case input combination.
Noise Margin for both "1" and "0" level =
0.5 Vdc min @ V_{DD} = 5.0 Vdc
1.0 Vdc min @ V_{DD} = 10 Vdc
1.0 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + N \times 10^{-3}(C_L - 50)V_{DD}f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency and N is number of gates per package.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns		5.0	–	115	230	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	–	55	110	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 15 ns		15	–	40	80	

*The formulas given are for the typical characteristics only.

3

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

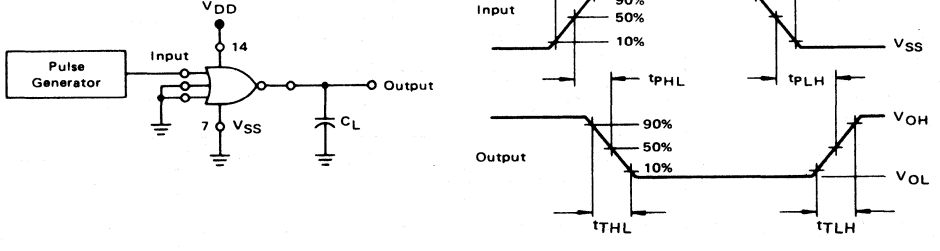


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

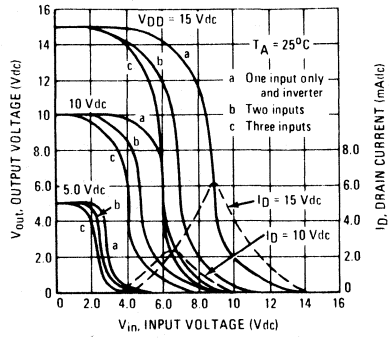
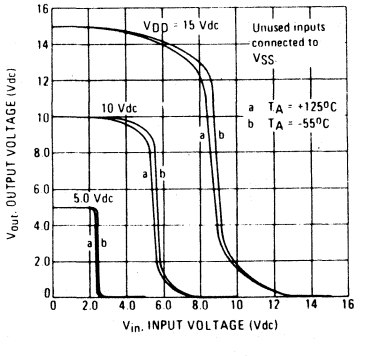


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE



MOTOROLA

MC14001B
Quad 2-Input NOR Gate

MC14002B
Dual 4-Input Nor Gate

MC14011B
Quad 2-Input NAND Gate

MC14012B
Dual 4-Input NAND Gate

MC14023B
Triple 3-Input NAND Gate

MC14025B
Triple 3-Input NOR Gate

MC14068B
8-Input NAND Gate

MC14071B
Quad 2-Input OR Gate

MC14072B
Dual 4-Input OR Gate

MC14073B
Triple 3-Input AND Gate

MC14075B
Triple 3-Input OR Gate

MC14078B
8-Input NOR Gate

MC14081B
Quad 2-Input AND Gate

MC14082B
Dual 4-Input AND Gate

3

B-SUFFIX SERIES CMOS GATES

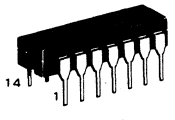
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices

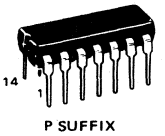
ORDERING INFORMATION

MC14XXXB — Suffix Denotes

- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}.

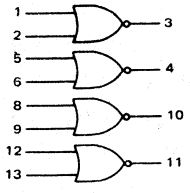
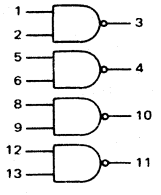
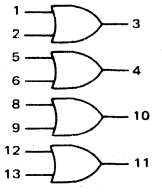
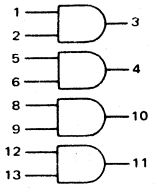
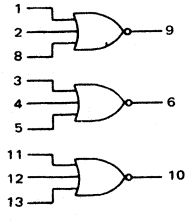
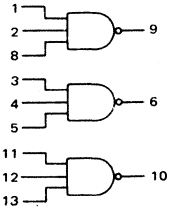
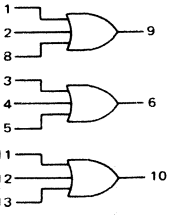
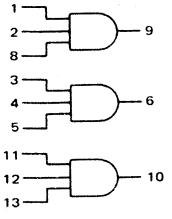
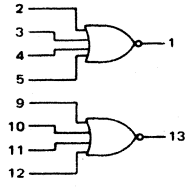
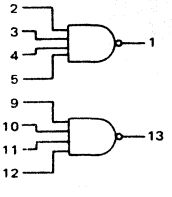
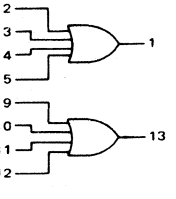
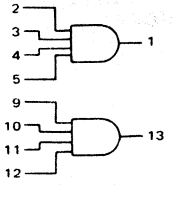
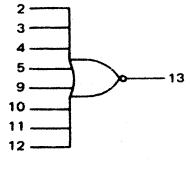
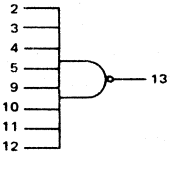
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

B-SERIES GATES

CMOS B-SERIES GATES

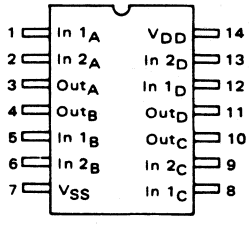
LOGIC DIAGRAMS

	NOR	NAND	OR	AND
2 INPUT	**MC14001B** Quad 2-Input NOR Gate	**MC14011B** Quad 2-Input NAND Gate	**MC14071B** Quad 2-Input OR Gate	**MC14081B** Quad 2-Input AND Gate
				
3 INPUT	**MC14025B** Triple 3-Input NOR Gate	**MC14023B** Triple 3-Input NAND Gate	**MC14075B** Triple 3-Input OR Gate	**MC14073B** Triple 3-Input AND Gate
				
4 INPUT	**MC14002B** Dual 4-Input NOR Gate	**MC14012B** Dual 4-Input NAND Gate	**MC14072B** Dual 4-Input OR Gate	**MC14082B** Dual 4-Input AND Gate
				
8 INPUT	**MC14078B** 8-Input NOR Gate	**MC14068B** 8-Input NAND Gate		
				

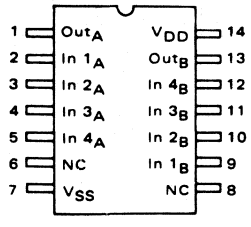
V_{DD} = Pin 14
V_{SS} = Pin 7
for All Devices

PIN ASSIGNMENTS

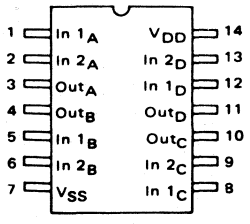
MC14001B
Quad 2-Input NOR Gate



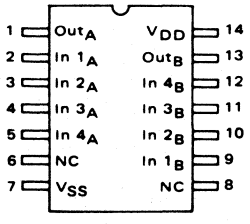
MC14002B
Dual 4-Input NOR Gate



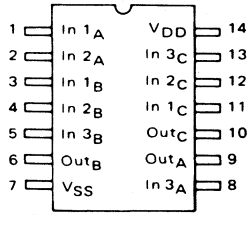
MC14011B
Quad 2-Input NAND Gate



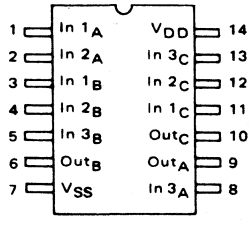
MC14012B
Dual 4-Input NAND Gate



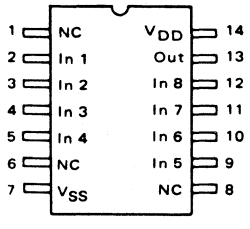
MC14023B
Triple 3-Input NAND Gate



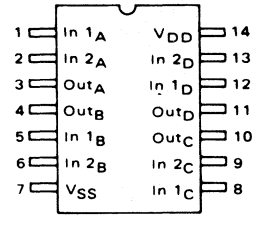
MC14025B
Triple 3-Input NOR Gate



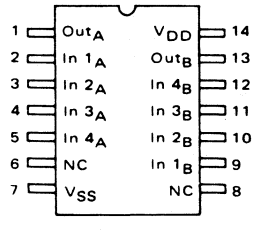
MC14068B
8-Input NAND Gate



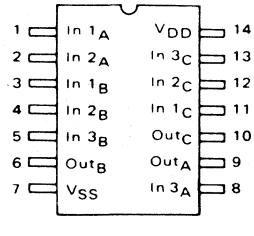
MC14071B
Quad 2-Input OR Gate



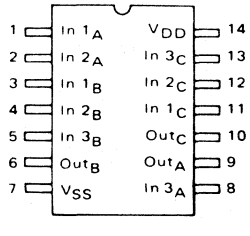
MC14072B
Dual 4-Input OR Gate



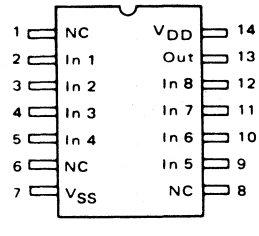
MC14073B
Triple 3-Input AND Gate



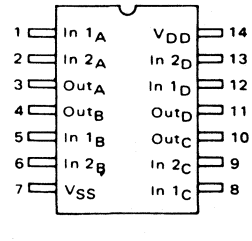
MC14075B
Triple 3-Input OR Gate



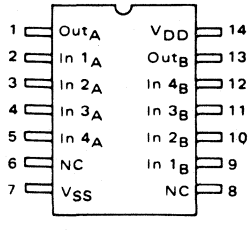
MC14078B
8-Input NOR Gate



MC14081B
Quad 2-Input AND Gate



MC14082B
Dual 4-Input AND Gate



NC = No Connection

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15		±0.1		±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15		±0.3		±0.00001	±0.3		±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–			5.0	7.5			pF
Quiescent Current (AL Device)	I_{DD}	5.0		0.25	–	0.0005	0.25	–	7.5	μAdc
(Per Package)		10		0.50		0.0010	0.50		15.0	
		15		1.00		0.0015	1.00		30.0	
Quiescent Current (CL/CP Device)	I_{DD}	5.0		1.0		0.0005	1.0		7.5	μAdc
(Per Package)		10		2.0		0.0010	2.0		15.0	
		15		4.0		0.0015	4.0		30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	$I_T = (0.3\ \mu A/kHz)\ f + I_{DD}/N$							μAdc
		10	$I_T = (0.6\ \mu A/kHz)\ f + I_{DD}/N$							
		15	$I_T = (0.9\ \mu A/kHz)\ f + I_{DD}/N$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF

$$I_T(C_L) = I_T(50\ pF) + N \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency and N is number of gates per package.
**The formulas given are for the typical characteristics only at 25°C.

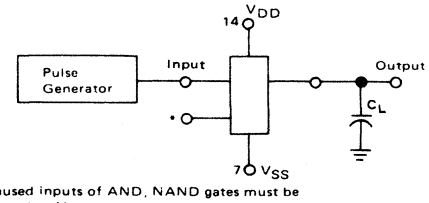
B-SERIES GATE SWITCHING TIMES

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

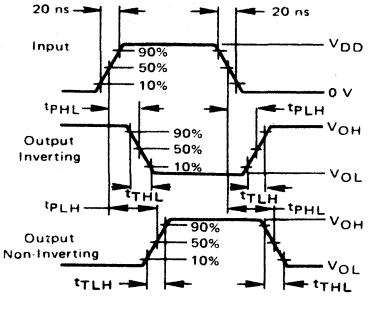
Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time, All B-Series Gates	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Output Fall Time, All B-Series Gates	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
MC14001B, MC14011B only						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 80 ns		5.0	–	125	250	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 32 ns		10	–	50	100	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 27 ns		15	–	40	80	
All Other 2, 3, and 4 Input Gates						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns		5.0	–	160	300	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns		10	–	65	130	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		15	–	50	100	
8-Input Gates (MC14068B, MC14078B)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 155 ns		5.0	–	200	350	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 62 ns		10	–	80	150	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	–	60	110	

*The formulas given are for the typical characteristics only.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

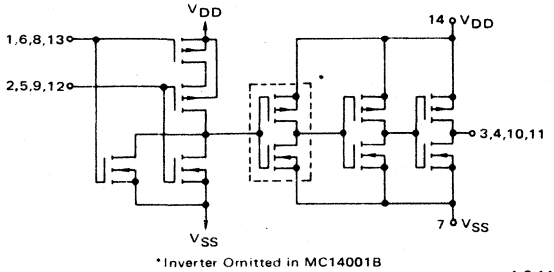


*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.



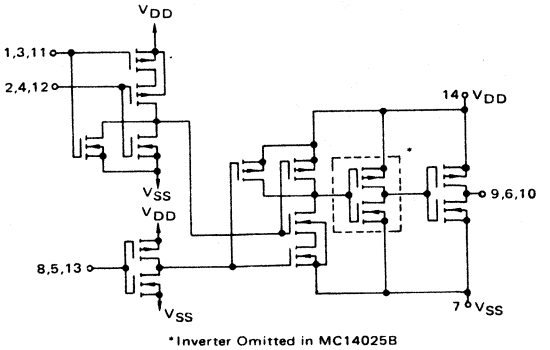
CIRCUIT SCHEMATIC
NOR, OR Gates

MC14001B
MC14071B
One of Four
Gates Shown



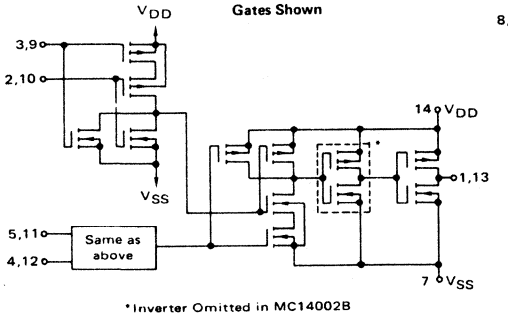
*Inverter Omitted in MC14001B

MC14025B
MC14075B
One of Three
Gates Shown



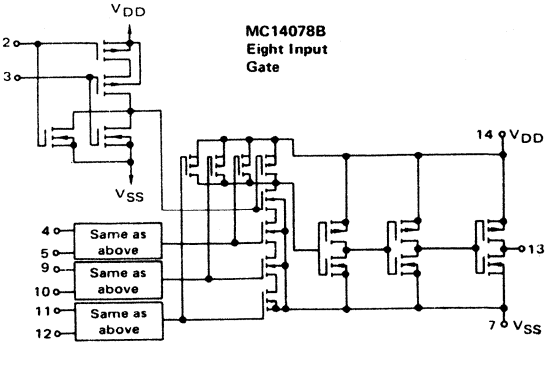
*Inverter Omitted in MC14025B

MC14002B
MC14072B
One of Two
Gates Shown



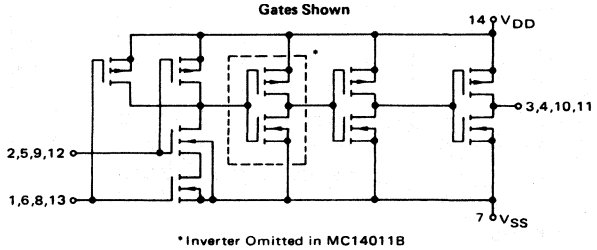
*Inverter Omitted in MC14002B

MC14078B
Eight Input
Gate



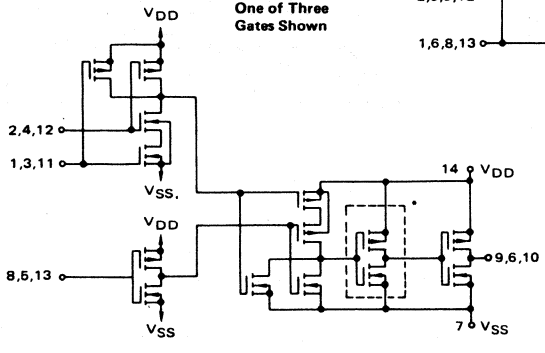
CIRCUIT SCHEMATICS
NAND, AND Gates

MC14011B
MC14081B
One of Four Gates Shown



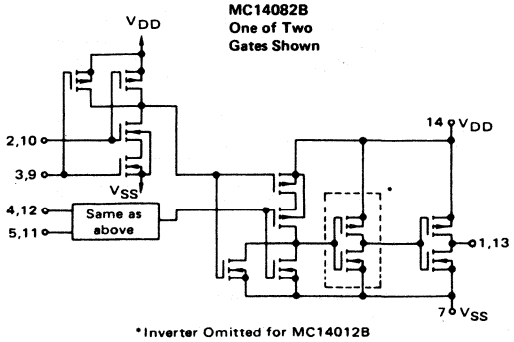
*Inverter Omitted in MC14011B

MC14023B
MC14073B
One of Three Gates Shown



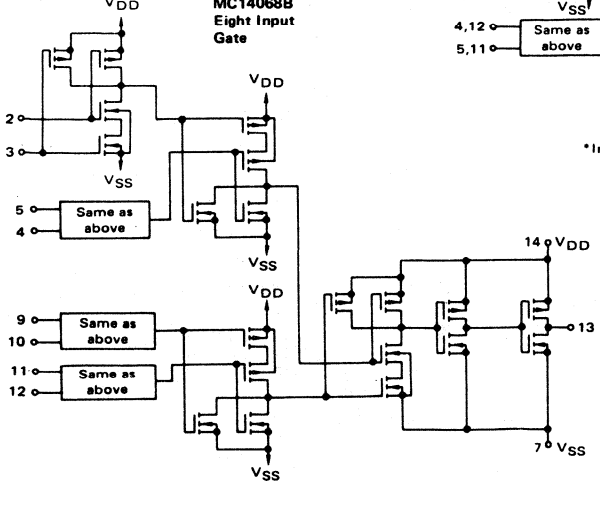
*Inverter Omitted in MC14023B

MC14012B
MC14082B
One of Two Gates Shown



*Inverter Omitted for MC14012B

MC14068B
Eight Input Gate



TYPICAL B-SERIES GATE CHARACTERISTICS

N-CHANNEL DRAIN CURRENT (SINK)

FIGURE 2 – V_{GS} = 5.0 Vdc

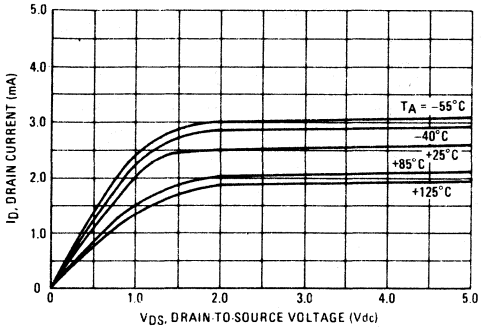


FIGURE 4 – V_{GS} = 10 Vdc

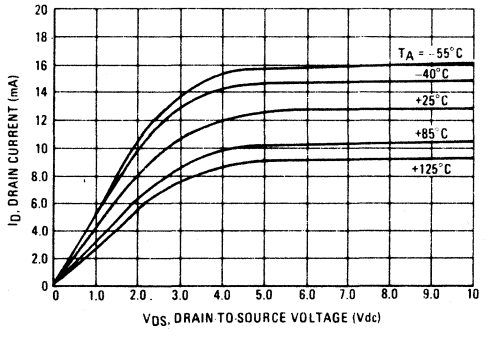
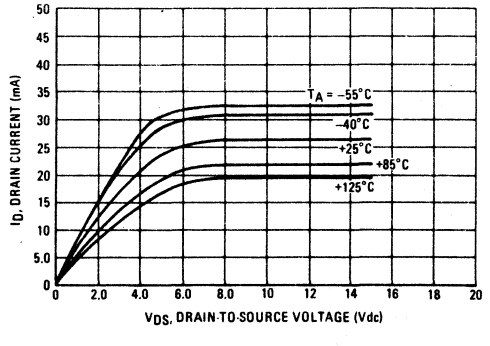


FIGURE 6 – V_{GS} = 15 Vdc



P-CHANNEL DRAIN CURRENT (SOURCE)

FIGURE 3 – V_{GS} = −5.0 Vdc

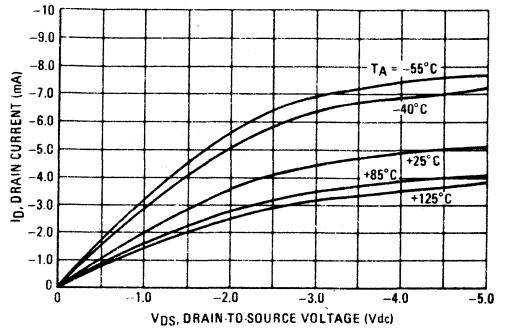


FIGURE 5 – V_{GS} = −10 Vdc

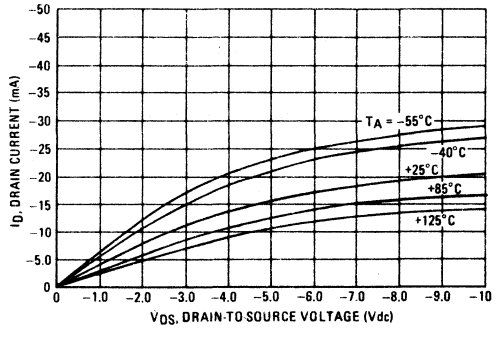
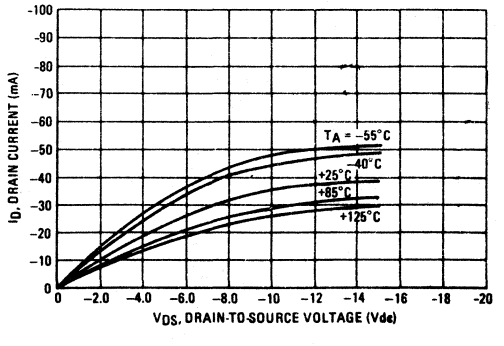


FIGURE 7 – V_{GS} = −15 Vdc



TYPICAL B-SERIES GATE CHARACTERISTICS (cont'd)

VOLTAGE TRANSFER CHARACTERISTICS

FIGURE 8 – V_{DD} = 5.0 Vdc

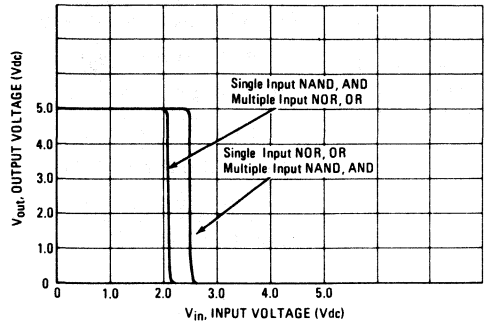


FIGURE 9 – V_{DD} = 10 Vdc

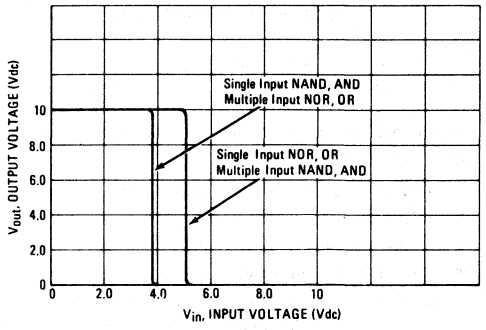
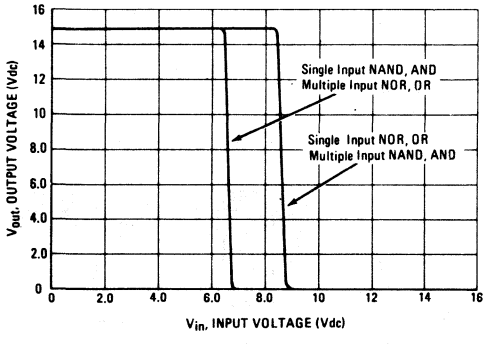


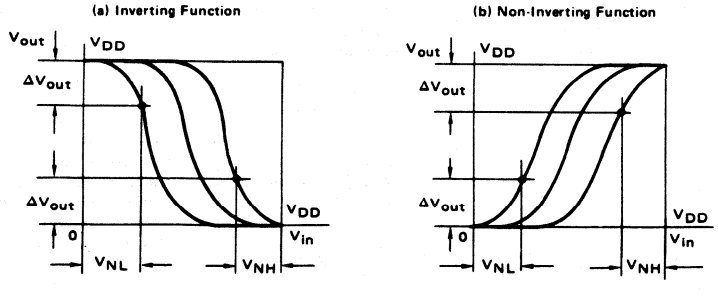
FIGURE 10 – V_{DD} = 15 Vdc



DC NOISE IMMUNITY (V_{NL} AND V_{NH})

The dc noise immunity is defined as the input voltage range from an ideal "1" or "0" input level (assuming the previous CMOS driving state is unloaded which does not produce output state (combination) change(s). The typical and limit values of the input ranges V_{NL} and V_{NH} for the output to stay within a range ΔV_{out} from either V_{DD} or V_{SS} are given in the Electrical Characteristics table. The definitions of V_{NL}, V_{NH}, and ΔV_{out} are illustrated in Figure 11 for inverting and non-inverting functions.

FIGURE 11 – DC NOISE IMMUNITY



V_{SS} = 0 volts dc

MOTOROLA

MC14001UB
Quad 2-Input NOR Gate

MC14002UB
Dual 4-Input NOR Gate

MC14011UB
Quad 2-Input NAND Gate

MC14012UB
Dual 4-Input NAND Gate

MC14023UB
Triple 3-Input NAND Gate

MC14025UB
Triple3-Input NOR Gate

3

UB-SUFFIX SERIES CMOS GATES

The UB Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired. The UB set of CMOS gates are inverting non-buffered functions.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linear and Oscillator Applications
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series UB Suffix Devices
- Formerly Listed without UB Suffix

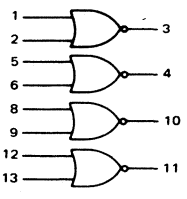
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

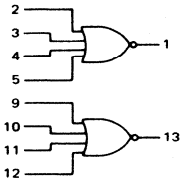
UB-SERIES GATES

LOGIC DIAGRAMS

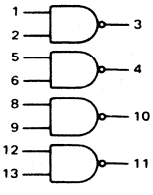
MC14001UB
Quad 2-Input NOR Gate



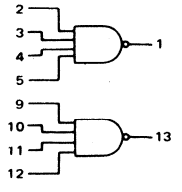
MC14002UB
Dual 4-Input NOR Gate



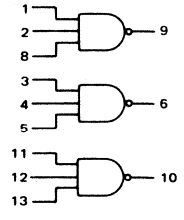
MC14011UB
Quad 2-Input NAND Gate



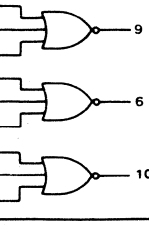
MC14012UB
Dual 4-Input NAND Gate



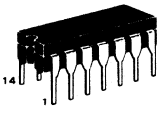
MC14023UB
Triple 3-Input NAND Gate



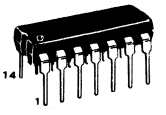
MC14025UB
Triple 3-Input NOR Gate



V_{DD} = Pin 14
V_{SS} = Pin 7
for All Devices



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

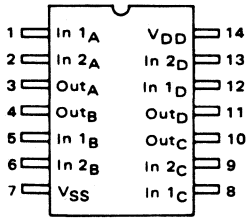
MC14XXXUB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

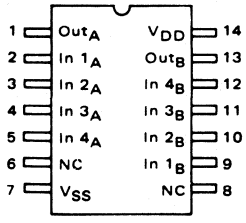
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN ASSIGNMENTS

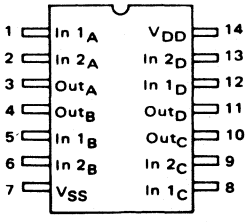
MC14001UB
Quad 2-Input NOR Gate



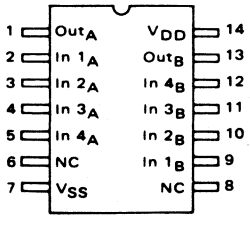
MC14002UB
Dual 4-Input NOR Gate



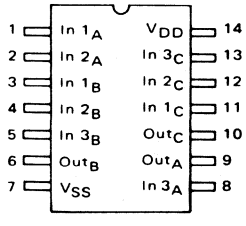
MC14011UB
Quad 2-Input NAND Gate



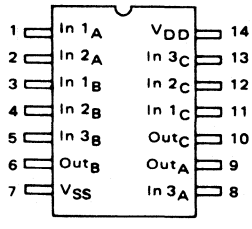
MC14012UB
Dual 4-Input NAND Gate



MC14023UB
Triple 3-Input NAND Gate



MC14025UB
Triple 3-Input NOR Gate



NC = No Connection

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5 Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0 Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate, C_L = 50 pF)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}/N							µAdc
		10	I_T = (0.6 µA/kHz) f + I_{DD}/N							
		15	I_T = (0.8 µA/kHz) f + I_{DD}/N							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
0.5 Vdc min @ V_{DD} = 5.0 Vdc
1.0 Vdc min @ V_{DD} = 10 Vdc
1.0 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + N \times 10^{-3}(C_L - 50)V_{DD}f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency and N is number of gates per package.

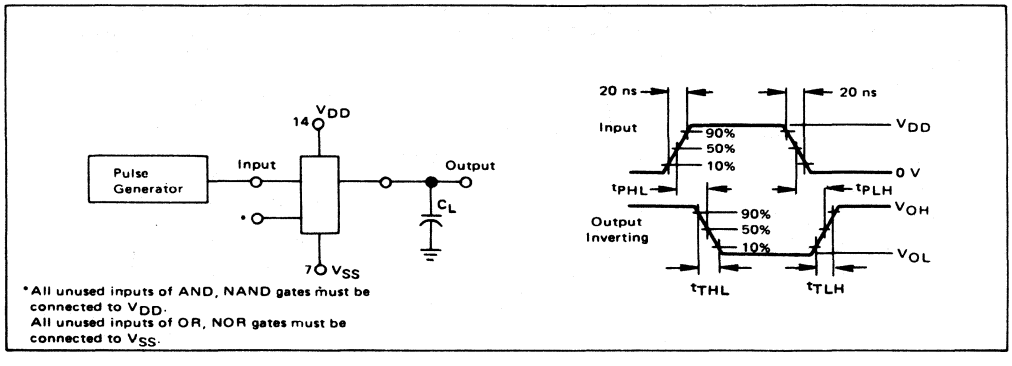
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns		5.0	–	90	180	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	–	50	100	
t_{PLH}, t_{PHL} = (0.50 ns/pF) C_L + 15 ns		15	–	40	80	

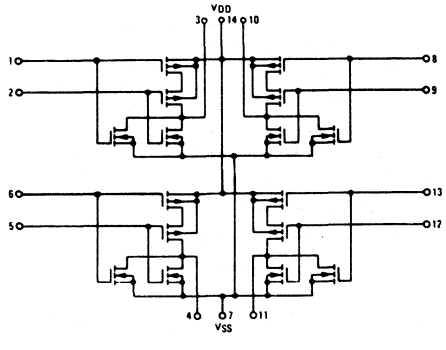
* The Formulae given are for the Typical Characteristics only.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

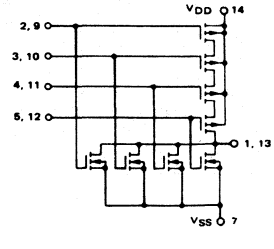


*All unused inputs of AND, NAND gates must be connected to V_{DD}.
All unused inputs of OR, NOR gates must be connected to V_{SS}.

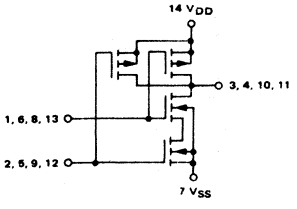
MC14001UB CIRCUIT SCHEMATIC



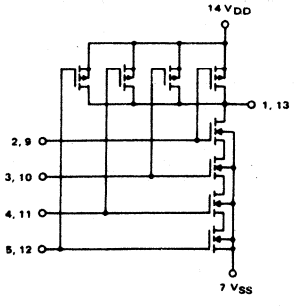
MC14002UB CIRCUIT SCHEMATIC
(1/2 of Device Shown)



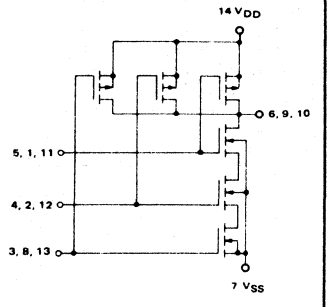
MC14011UB CIRCUIT SCHEMATIC
(1/4 of Device Shown)



MC14012UB CIRCUIT SCHEMATIC
(1/2 of Device Shown)



MC14023UB CIRCUIT SCHEMATIC
(1/3 of Device Shown)



MC14025UB CIRCUIT SCHEMATIC
(1/3 of Device Shown)

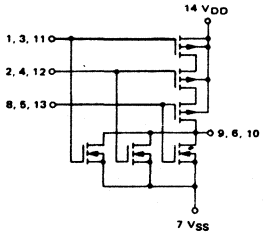


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

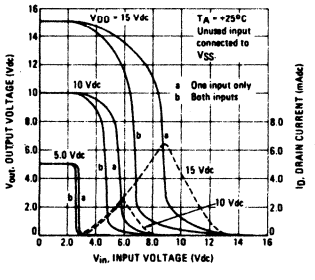


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

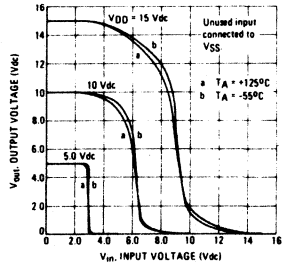


FIGURE 4 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

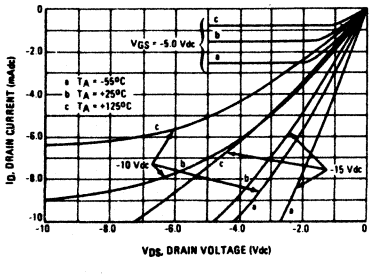
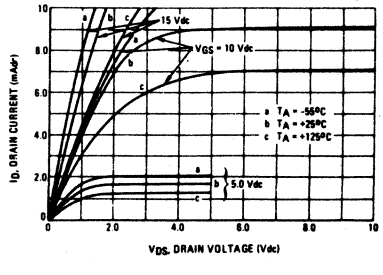


FIGURE 5 – TYPICAL OUTPUT SINK CHARACTERISTICS



MOTOROLA

MC14002B
MC14002UB

DUAL 4-INPUT "NOR" GATE

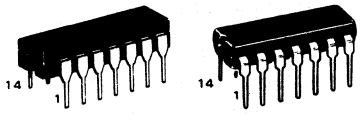
The MC14002B and MC14002UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14002B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14002B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4002B and CD4002UB

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB or UB as Applicable — Suffix — Denotes

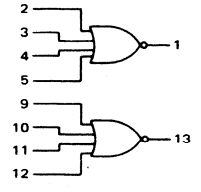
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics of the B-Series device.
See the MC14001UB data sheet for complete characteristics for the UB device.

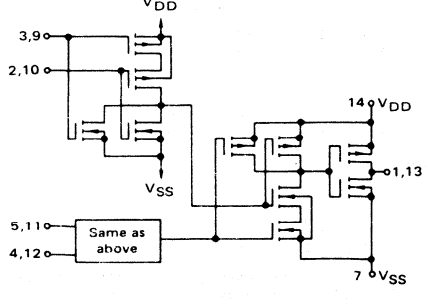
LOGIC DIAGRAM



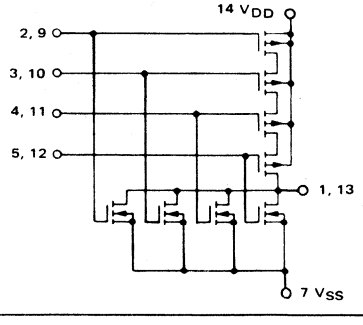
V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATICS
(1/2 of Device Shown)

MC14002B



MC14002UB



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14006B

CMOS MSI

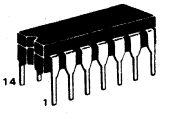
(LOW-POWER COMPLEMENTARY MOS)

18-BIT STATIC SHIFT REGISTER

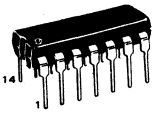
18-BIT STATIC SHIFT REGISTER

The MC14006B shift register is comprised of four separate shift register sections sharing a common clock: two sections have four stages, and two sections have five stages with an output tap on both the fourth and fifth stages. This makes it possible to obtain a shift register of 4, 5, 8, 9, 10, 12, 13, 14, 16, 17, or 18 bits by appropriate selection of inputs and outputs. This part is particularly useful in serial shift registers and time delay circuits.

- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Quiescent Current - 5nA/package typical @ 5 Vdc
- Fully Static Operation
- 8-MHz Shift Rate typical
- Can be Cascaded to Provide Longer Shift Register Lengths
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4006B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

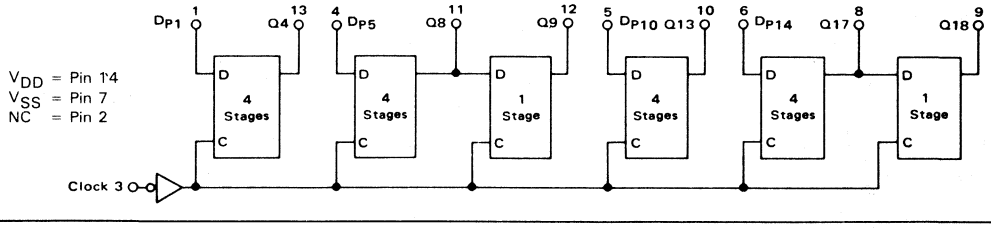
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE
(Single Stage)

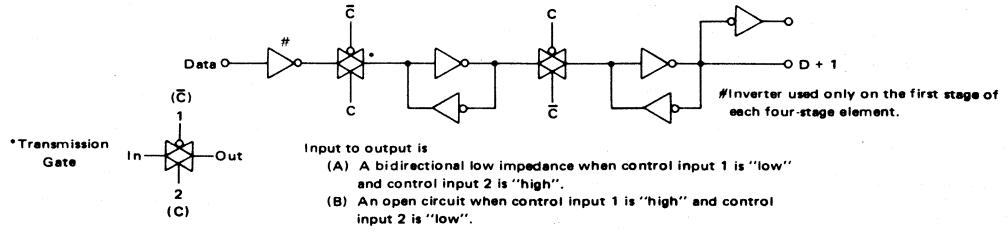
D_n	C	Q_{n+1}
0	⌐	0
1	⌐	1
X	_	Q_n

X = Don't Care

BLOCK DIAGRAM



LOGIC DIAGRAM
(ONE REGISTER STAGE)



#Inverter used only on the first stage of each four-stage element.

*Transmission Gate

Input to output is
(A) A bidirectional low impedance when control input 1 is "low" and control input 2 is "high".
(B) An open circuit when control input 1 is "high" and control input 2 is "low".

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.3 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.6 μA/kHz) f + I_{DD}							
		15	I_T = (3.9 μA/kHz) f + I_{DD}							

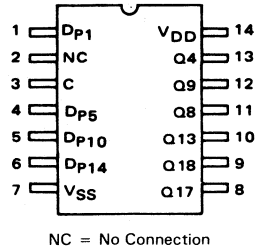
*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



NC = No Connection

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
T_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 220 ns	t_{PHL}	5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 77 ns		10	–	110	220	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 55 ns		15	–	80	160	
Clock Pulse Width	t_{WH}	5.0	200	100	–	ns
		10	120	60	–	
		15	80	40	–	
Clock Pulse Frequency	f_{cl}	5.0	–	5.0	2.5	MHz
		10	–	8.3	4.2	
		15	–	12	6.0	
Clock Pulse Rise and Fall Time#	t_{TLH}	5.0	–	–	15	μs
	t_{THL}	10	–	–	5	
		15	–	–	4	
Setup Time	t_{su}	5.0	0	-50	–	ns
		10	0	-15	–	
		15	0	-8.0	–	
Hold Time	t_h	5.0	180	75	–	ns
		10	90	25	–	
		15	75	20	–	

* The formulae given are for typical characteristics only.

\# When shift register sections are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the rise and fall times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitance load.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

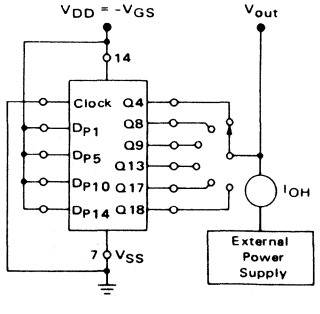


FIGURE 2 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT

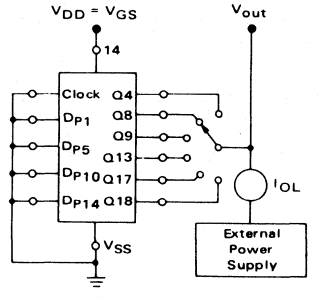


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

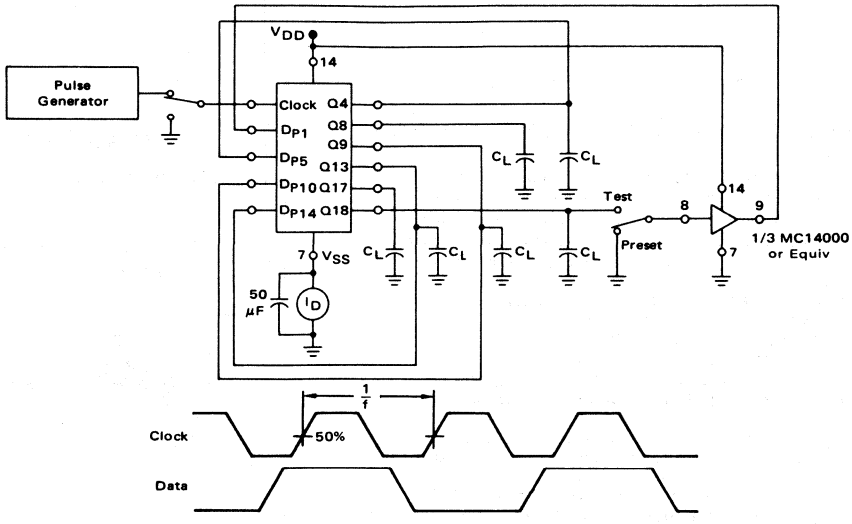
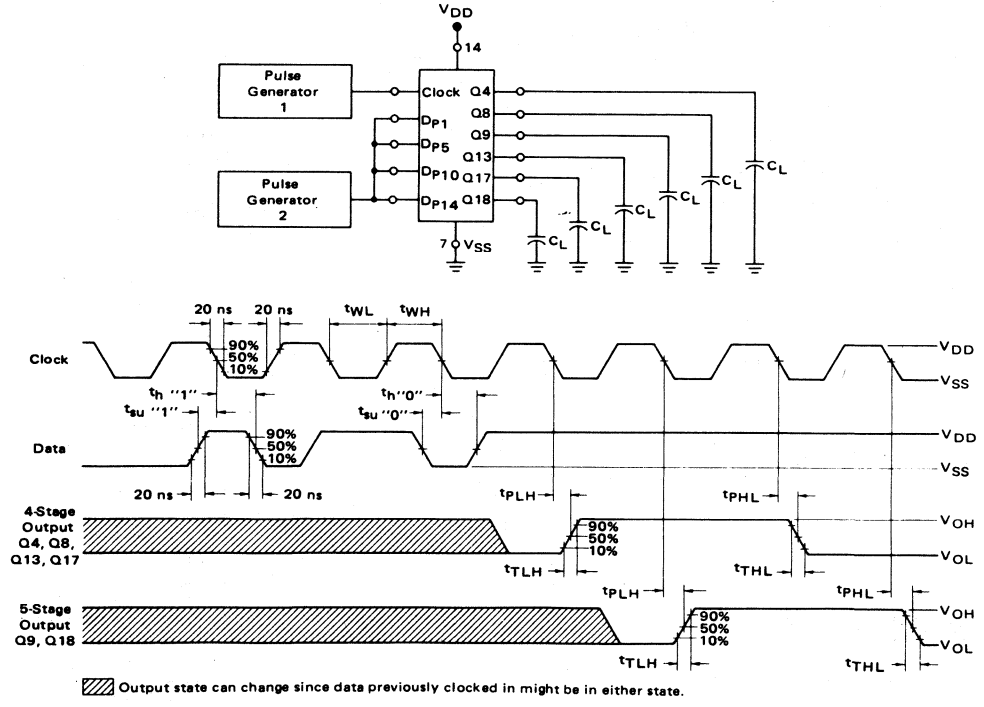


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MOTOROLA

MC14007UB

DUAL COMPLEMENTARY PAIR PLUS INVERTER

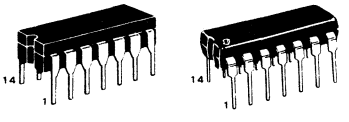
The MC14007UB multi-purpose device consists of three N-channel and three P-channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse-shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation = Positive or Negative
- Symmetrical Output Impedance — 200 ohms typical @ 10 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4007A or CD4007UB
- This device has 2 outputs without ESD Protection. Anti-static precautions must be taken.

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL COMPLEMENTARY PAIR PLUS INVERTER



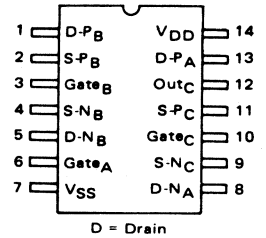
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS})

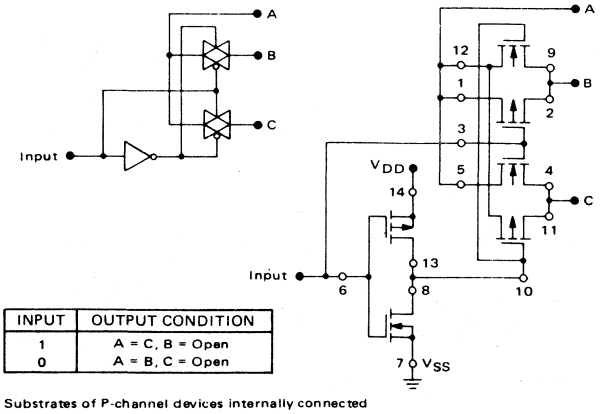
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN ASSIGNMENT



D = Drain
S = Source

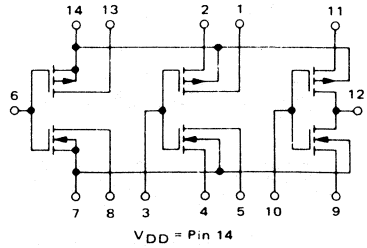
FIGURE 1 — TYPICAL APPLICATION: 2-INPUT ANALOG MULTIPLEXER



INPUT	OUTPUT CONDITION
1	A = C, B = Open
0	A = B, C = Open

Substrates of P-channel devices internally connected to V_{DD}; substrates of N-channel devices internally connected to V_{SS}.

SCHEMATIC



V_{DD} = Pin 14
V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS (Connected as Inverters)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-5.0	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-1.0	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.5	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-10	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	1.0	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.5	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	10	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-5.0	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-1.0	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.5	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-10	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	1.0	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.5	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	10	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)	I_T	5.0	I_T = (0.7 µA/kHz) f + I_{DD}/6							µAdc
		10	I_T = (1.4 µA/kHz) f + I_{DD}/6							
		15	I_T = (2.2 µA/kHz) f + I_{DD}/6							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device

†To calculate total supply current at loads other than 50 pF

$$I_T(C_L) = I_T(50\ pF) + 3 \times 10^{-3}(C_L - 50)V_{DD}f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
0.5 Vdc min @ V_{DD} = 5.0 Vdc
1.0 Vdc min @ V_{DD} = 10 Vdc
1.0 Vdc min @ V_{DD} = 15 Vdc

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

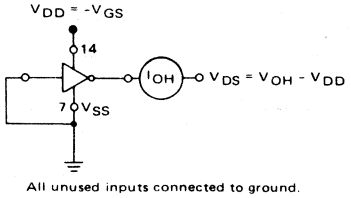
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.2 ns/pF) C_L + 30 ns		5.0	–	90	180	
t_{TLH} = (0.5 ns/pF) C_L + 20 ns		10	–	45	90	
t_{TLH} = (0.4 ns/pF) C_L + 15 ns		15	–	35	70	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.2 ns/pF) C_L + 15 ns		5.0	–	75	150	
t_{THL} = (0.5 ns/pF) C_L + 15 ns		10	–	40	80	
t_{THL} = (0.4 ns/pF) C_L + 10 ns		15	–	30	60	
Turn-Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.5 ns/pF) C_L + 35 ns		5.0	–	60	125	
t_{PLH} = (0.2 ns/pF) C_L + 20 ns		10	–	30	75	
t_{PLH} = (0.15 ns/pF) C_L + 17.5 ns		15	–	25	55	
Turn-On Delay Time	t_{PHL}					ns
t_{PHL} = (1.0 ns/pF) C_L + 10 ns		5.0	–	60	125	
t_{PHL} = (0.3 ns/pF) C_L + 15 ns		10	–	30	75	
t_{PHL} = (0.2 ns/pF) C_L + 15 ns		15	–	25	55	

3

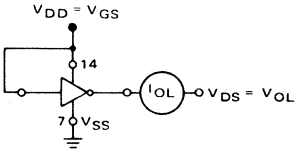
* The formulae given are for the typical characteristics only.
Switching specifications are for device connected as an inverter.

FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

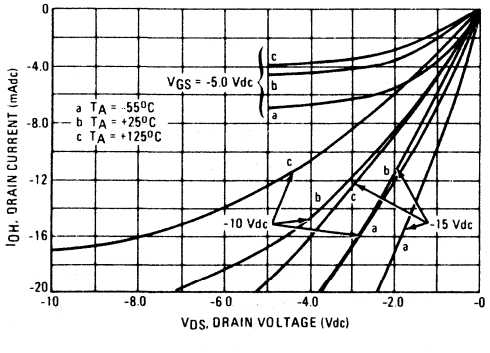


All unused inputs connected to ground.

FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS



All unused inputs connected to ground.



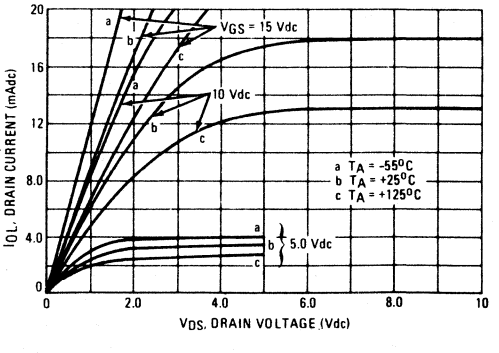
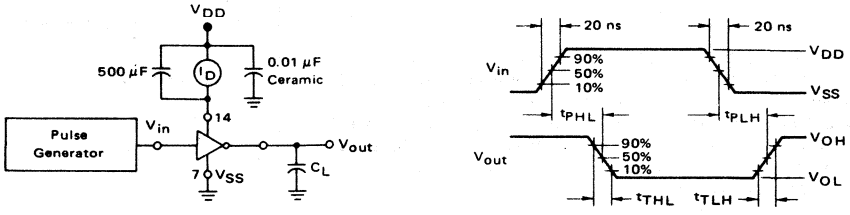


FIGURE 4 – SWITCHING TIME AND POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

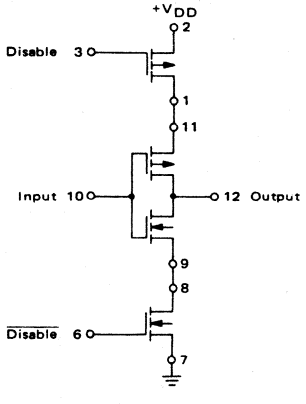


3

APPLICATIONS

The MC14007UB dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 5, and 6 are a few examples of the device flexibility.

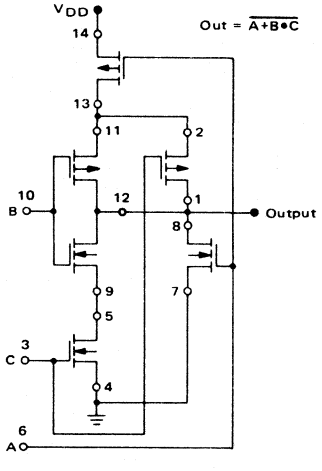
FIGURE 5 – 3-STATE BUFFER



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	Open

X = Don't Care

FIGURE 6 – AOI FUNCTIONS USING TREE LOGIC



Substrates of P-channel devices internally connected to V_{DD};
Substrates of N-channel devices internally connected to V_{SS}.

MOTOROLA

MC14008B

4-BIT FULL ADDER

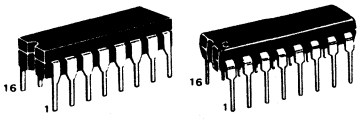
The MC14008B 4-bit full adder is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications.The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

- Look-Ahead Carry Output
- High-Speed Operation – 160 ns typical from Sum_{in} to Sum_{out}
- Quiescent Current – 5.0 nA/package typical @ 5 Vdc
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4008B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT FULL ADDER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

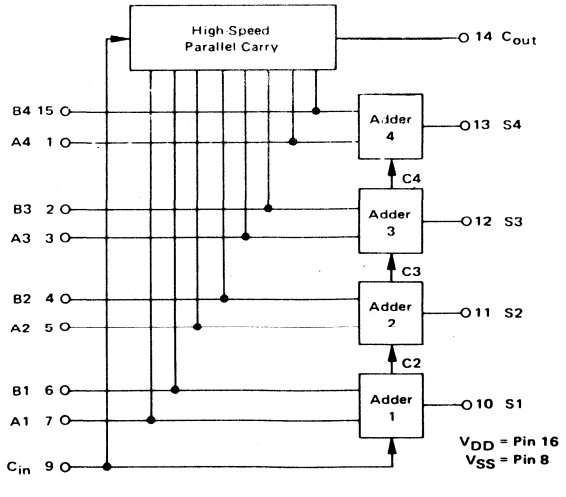
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

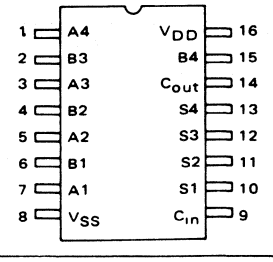
BLOCK DIAGRAM



TRUTH TABLE
(One Stage)

C_{in}	B	A	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.7 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.4 μA/kHz) f + I_{DD}							
		15	I_T = (5.0 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$
where I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time,	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time,	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Sum In to Sum Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 127 ns		10	–	160	320	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	–	115	230	
Sum In to Carry Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 220 ns		5.0	–	305	610	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 112 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Carry In to Sum Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 290 ns		5.0	–	375	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	–	155	310	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 90 ns		15	–	115	230	
Carry In to Carry Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 85 ns		5.0	–	170	340	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 30 ns		15	–	55	110	

*The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

FIGURE 1 – TYPICAL SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

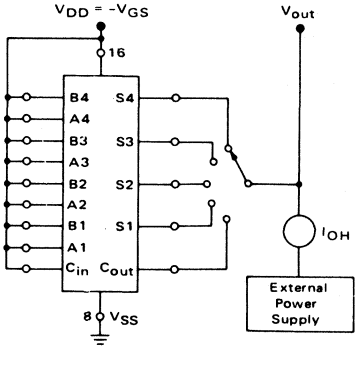


FIGURE 2 – TYPICAL SINK CURRENT CHARACTERISTICS TEST CIRCUIT

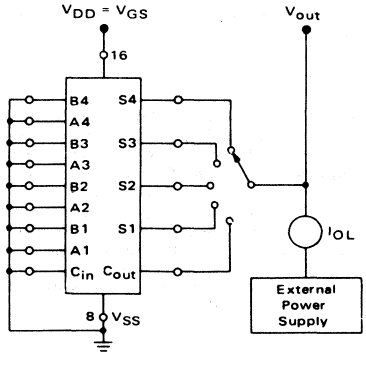


FIGURE 3 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

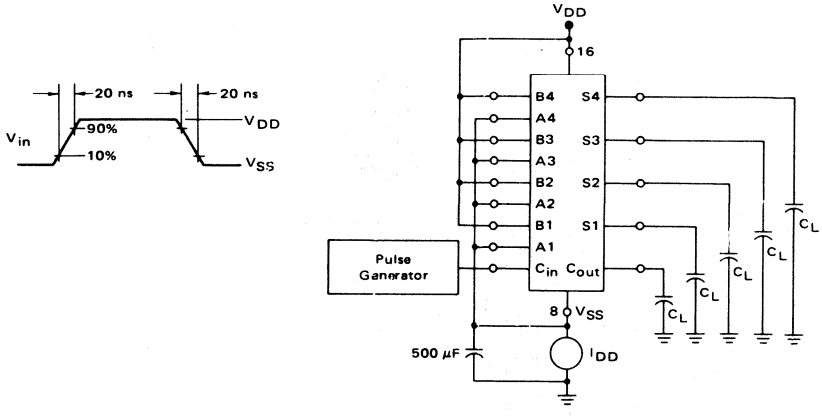


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

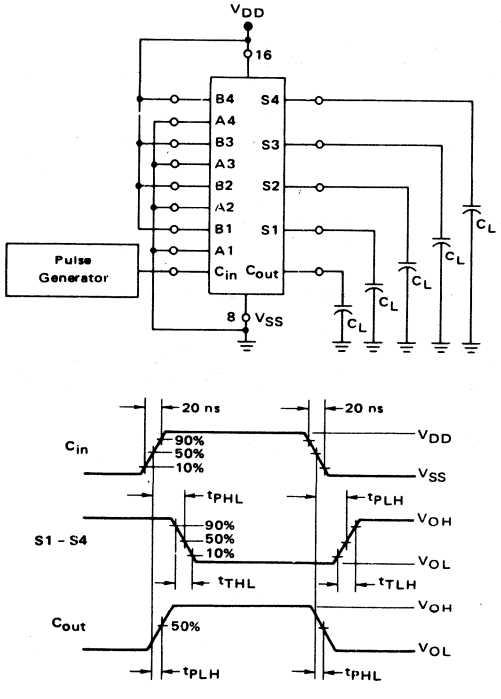
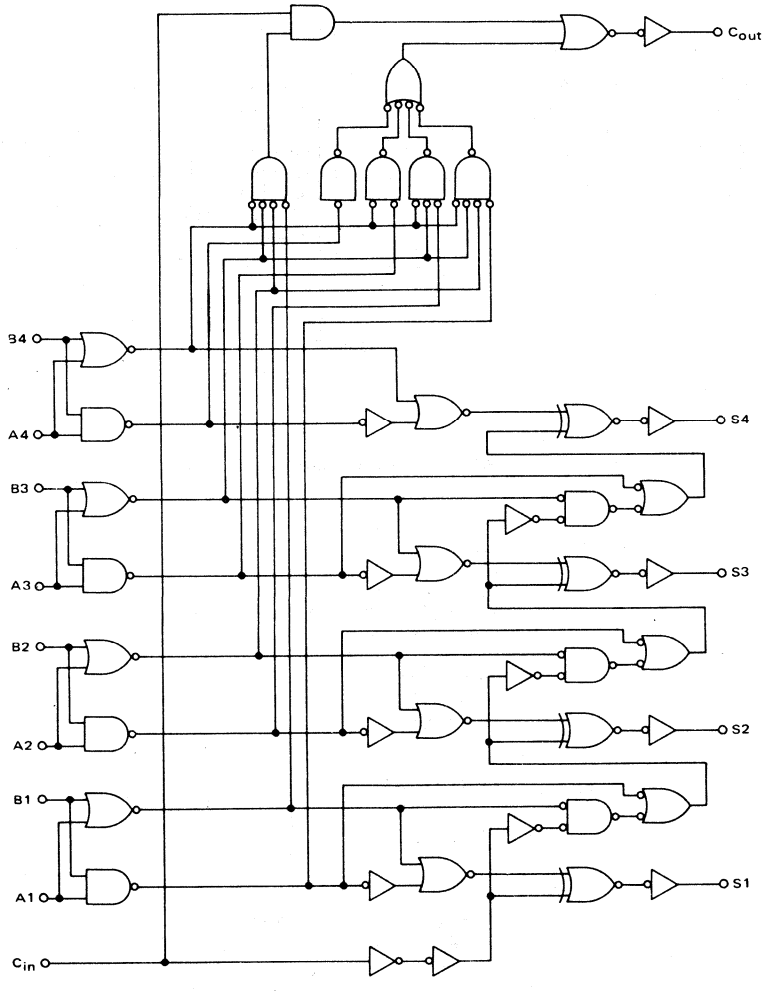
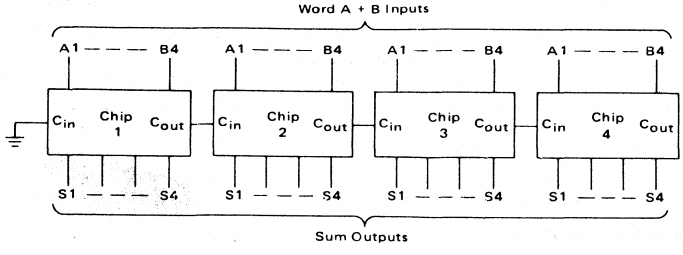


FIGURE 5 – LOGIC DIAGRAM



TYPICAL APPLICATION

FIGURE 6 – USING THE MC14008B IN A 16-BIT ADDER CONFIGURATION



Calculation of 16-bit adder speed:

tp total = tp (Sum to Carry) + tp (Carry to Sum) + 2 tp (Carry to Carry)

Typically, the overall 16-bit adder speed at 10 V is:

tp total = 115 + 125 + 90 = 330 ns typ

3

MOTOROLA

MC14011B
MC14011UB

QUAD 2-INPUT "NAND" GATE

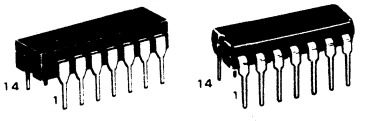
The MC14011B and MC14011UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14011B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14011B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4011B and CD4011UB

CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

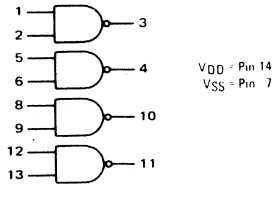
MC14XXXB — Suffix — Denotes
or UB, as applicable
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL, CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

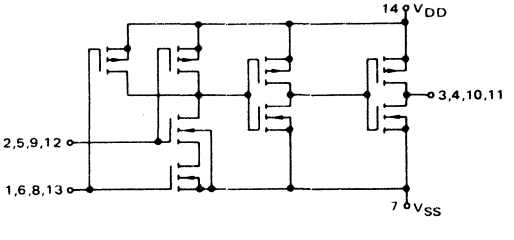
See the MC14001B data sheet for complete characteristics of the B-Series device.
See the MC14001UB data sheet for complete characteristics for the UB device.

LOGIC DIAGRAM

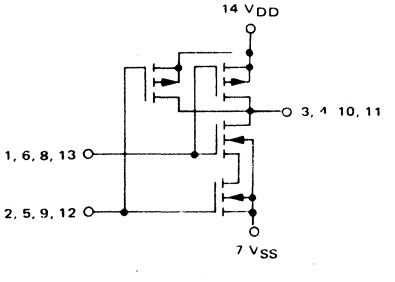


CIRCUIT SCHEMATICS
(1/4 of Device Shown)

MC14011B



MC14011UB



MOTOROLA

MC14012B
MC14012UB

DUAL 4-INPUT "NAND" GATE

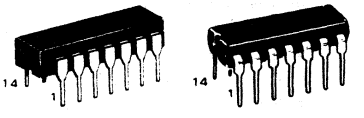
The MC14012B and MC14012UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14012B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14012B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4012B and CD4012UB

CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

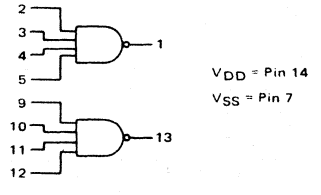
MC14XXXB — Suffix — Denotes
or UB as applicable
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

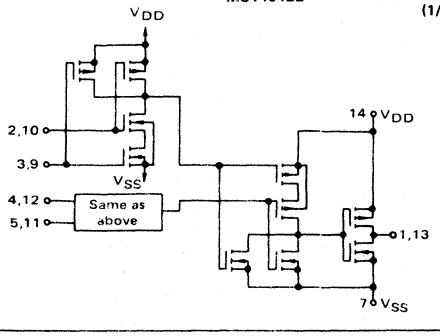
See the MC14001B data sheet for complete characteristics of the B-Series device.
See the MC14001UB data sheet for complete characteristics for the UB device.

LOGIC DIAGRAM

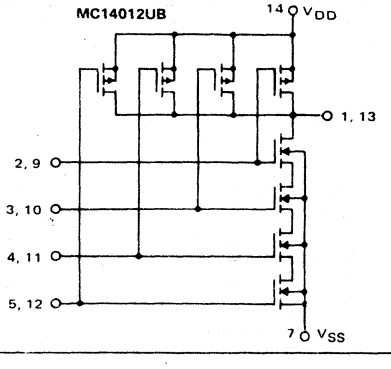


CIRCUIT SCHEMATICS (1/2 of Device Shown)

MC14012B



MC14012UB



3

MOTOROLA

MC14013B

DUAL TYPE D FLIP-FLOP

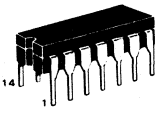
The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Toggle Rate = 4 MHz typical @ 5 Vdc
- Logic Edge-Clocked Flip-Flop Design -- Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013B

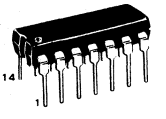
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL TYPE D FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

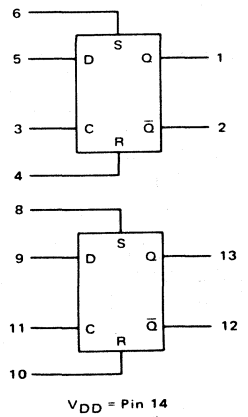
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range -- AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS				OUTPUTS		
CLOCK†	DATA	RESET	SET	Q	$\overline{Q}$	
⎍	0	0	0	0	1	
⎍	1	0	0	1	0	
⎎	X	0	0	Q	$\overline{Q}$	No Change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = Don't Care
† = Level Change

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

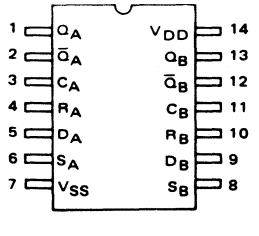
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.1	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.5 μA/kHz) f + I_{DD}							
		15	I_T = (2.3 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
Clock to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Set to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	350	450	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 50 ns		15	–	75	150	
Setup Times	t_{su}	5.0	40	20	–	ns
		10	20	10	–	
		15	15	7.5	–	
Hold Times	t_h	5.0	40	20	–	ns
		10	20	10	–	
		15	15	7.5	–	
Clock Pulse Width	t_{WL}, t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	70	35	–	
Clock Pulse Frequency	f_{cl}	5.0	–	4.0	2.0	MHz
		10	–	10	5.0	
		15	–	14	7.0	
Clock Pulse Rise and Fall Time	t_{TLH}	5.0	–	–	15	μs
	t_{THL}	10	–	–	5.0	
		15	–	–	4.0	
Set and Reset Pulse Width	t_{WL}, t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	70	35	–	

*The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

LOGIC DIAGRAM
(1/2 of Device Shown)

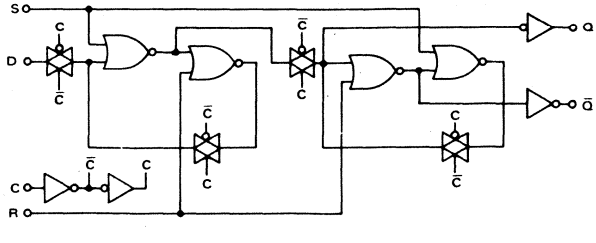


FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS
(Data, Clock, and Output)

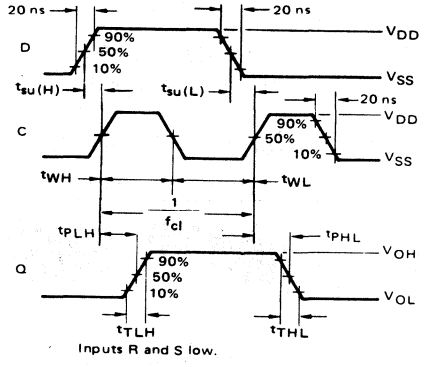
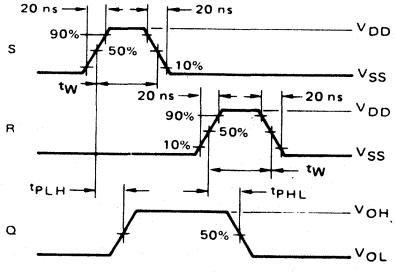


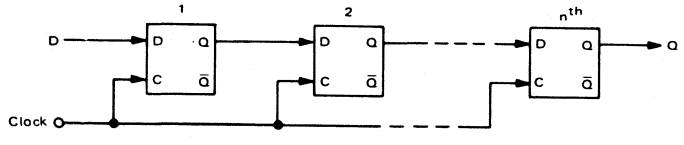
FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, and Output)



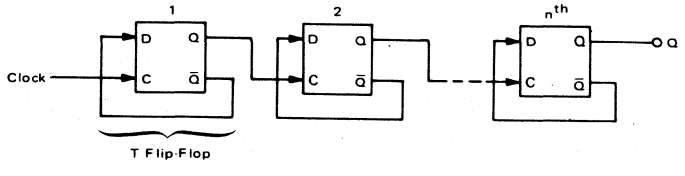
3

TYPICAL APPLICATIONS

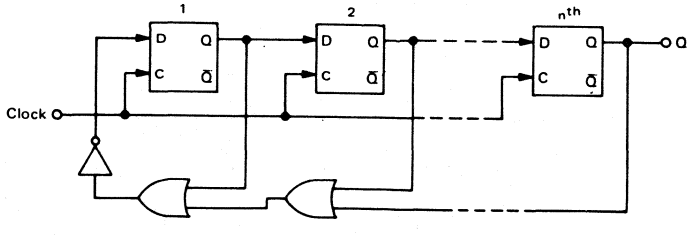
n-STAGE SHIFT REGISTER



BINARY RIPPLE UP-COUNTER (Divide-by-2^n)



MODIFIED RING COUNTER (Divide-by-(n + 1))



MOTOROLA

MC14014B
MC14021B

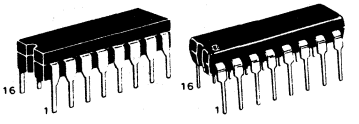
CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER

8-BIT STATIC SHIFT REGISTER

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation from DC to typ. 6.0 MHz at 10V V_{DD}
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

SERIAL OPERATION:

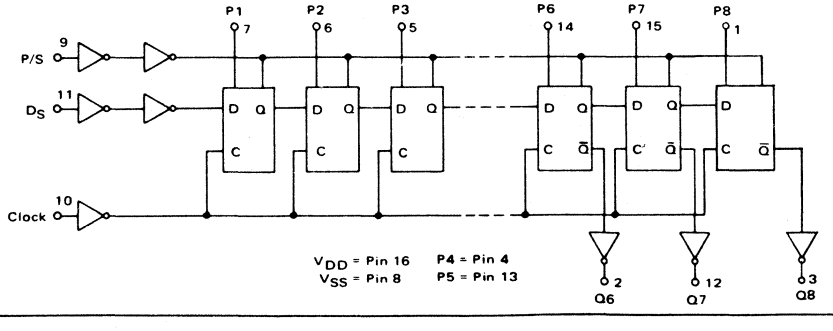
t	CLOCK	D_S	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n	⌐	0	0	0	?	?
n+1	⌐	1	0	1	0	?
n+2	⌐	0	0	0	1	0
n+3	⌐	1	0	1	0	1
-	⌙	X	0	Q6	Q7	Q8

PARALLEL OPERATION:

CLOCK		D_S	P/S	D_M	$*Q_M$
MC14014B	MC14021B				
⌐	X	X	1	0	0
⌐	X	X	1	1	1

*Q6, Q7, & Q8 are available externally
X = Don't Care

LOGIC DIAGRAM



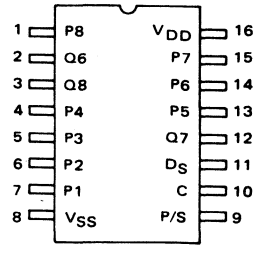
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	**0.005**	5.0	–	150	μAdc
		10	–	10	–	**0.010**	10	–	300	
		15	–	20	–	**0.015**	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	**0.005**	20	–	150	μAdc
		10	–	40	–	**0.010**	40	–	300	
		15	–	80	–	**0.015**	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.50 μA/kHz) f + I_{DD}							
		15	I_T = (2.25 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1.5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



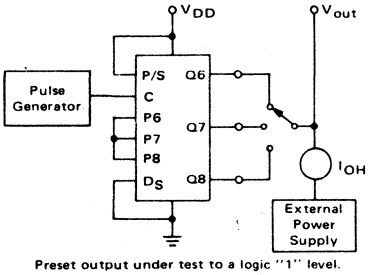
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time (Clock to Q, P/S to Q)	t_{PLH},					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns	t_{PHL}	5.0	–	400	800	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns		10	–	170	340	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 90 ns		15	–	115	230	
Clock Pulse Width	t_{WH}	5.0	400	150	–	ns
		10	175	75	–	
		15	135	40	–	
Clock Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Parallel/Serial Control Pulse Width	t_{WH}	5.0	400	150	–	ns
		10	175	75	–	
		15	135	40	–	
Setup Time	t_{su}	5.0	350	150	–	ns
		10	80	50	–	
		15	60	30	–	
Input Clock Rise Time	$t_{r(cl)}$	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	

*The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT



Preset output under test to a logic "1" level.

FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT

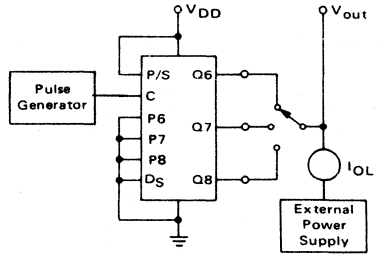


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

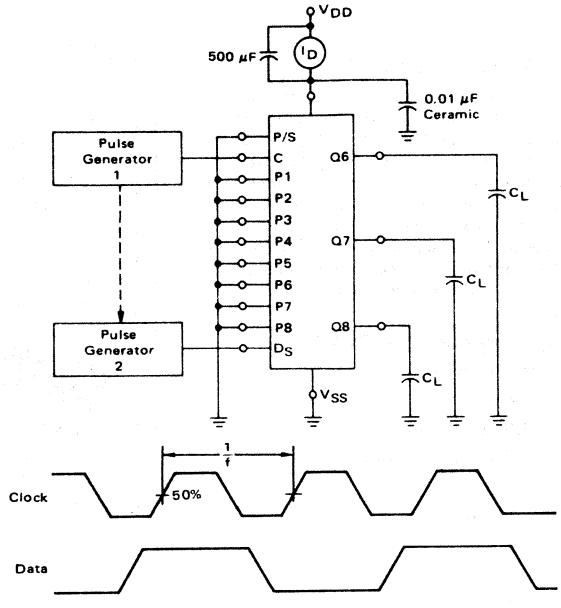
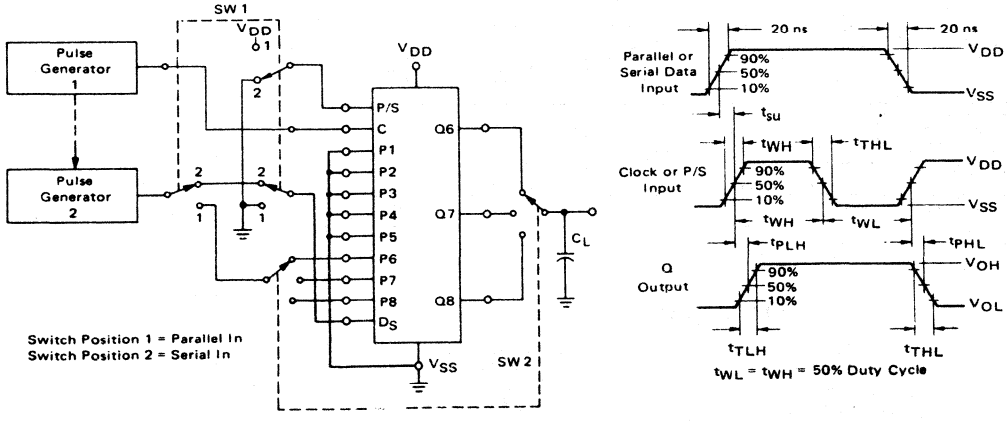


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MOTOROLA

MC14015B

DUAL 4-BIT STATIC SHIFT REGISTER

The MC14015B dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-state serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. There complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation -- Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Low Input Capacitance – 5.0 pF typical
- Logic Swing Independent of Fanout
- Toggle Rate = 6.0 MHz @ 10 Vdc
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive going edge of the clock pulse.
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLES

CLOCKED OPERATION (SYNCHRONOUS)

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$Q_{n+1} = D_n$, R = 0

DIRECT OPERATION (ASYNCHRONOUS)

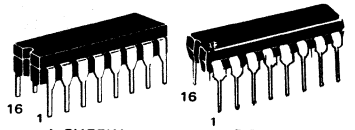
R	Q
0	Q
1	0

C = D = Don't Care

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-BIT STATIC SHIFT REGISTER



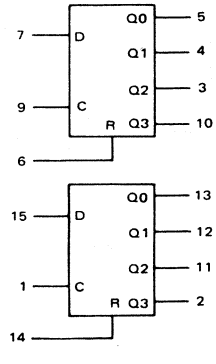
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

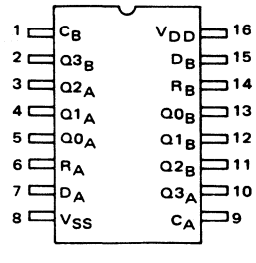
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.4 μA/kHz) f + I_{DD}							
		15	I_T = (3.6 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pf, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock, Data to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 225 ns		5.0	–	310	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	170	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 375 ns		5.0	–	460	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	120	170	
Clock Pulse Width	t_{WH}	5.0	–	185	400	ns
		10	–	85	175	
		15	–	55	135	
Clock Pulse Frequency	f_{cl}	5.0	–	2.0	1.5	MHz
		10	–	6.0	3.0	
		15	–	7.5	3.75	
Clock Pulse Rise and Fall Times	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
Reset Pulse Width	t_{WH}	5.0	400	200	–	ns
		10	160	80	–	
		15	120	60	–	
Setup Time	t_{su}	5.0	350	100	–	ns
		10	100	50	–	
		15	75	40	–	

*The formulae given are for typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

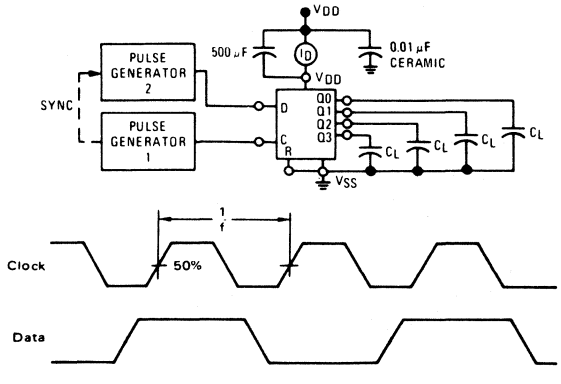


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

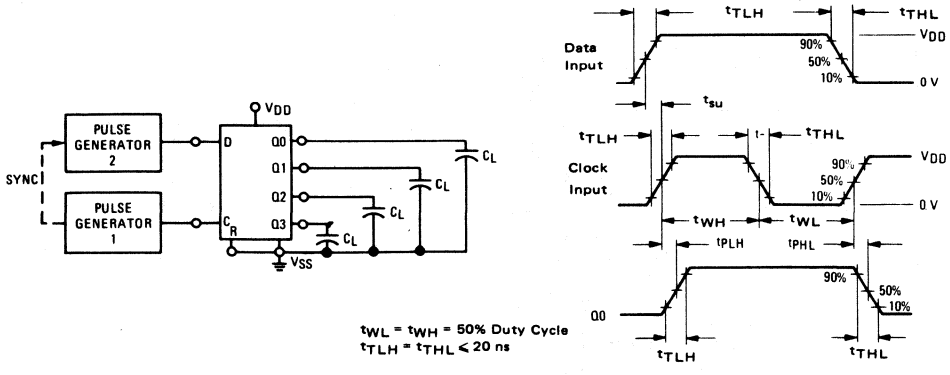
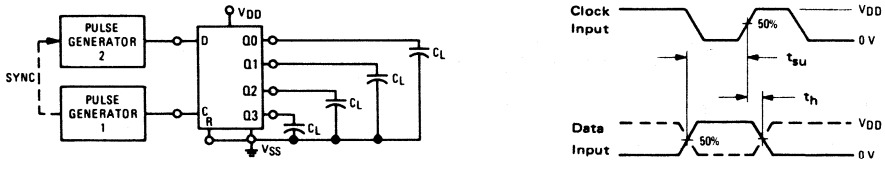
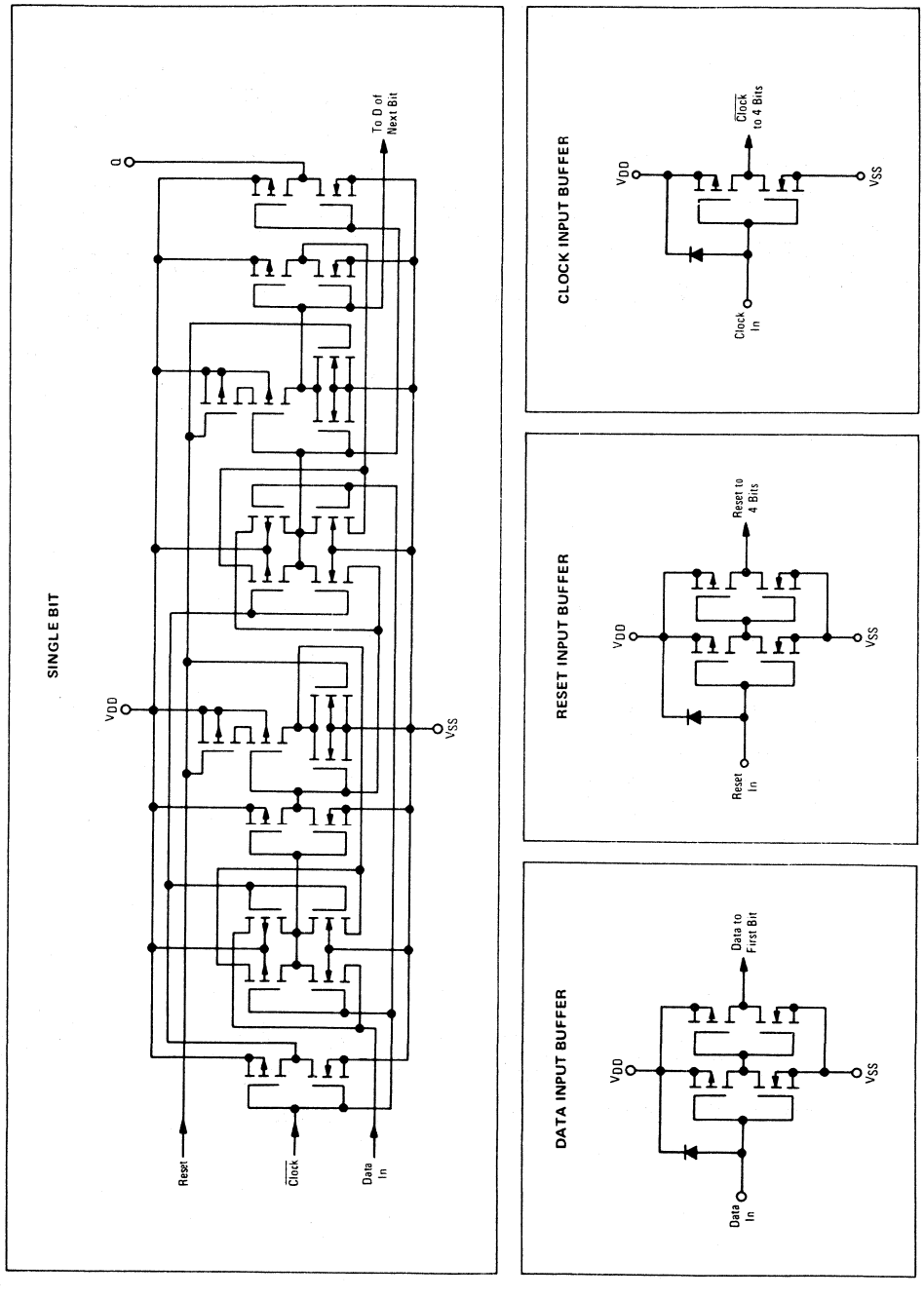


FIGURE 3 – SETUP AND HOLD TIME TEST CIRCUIT AND WAVEFORMS



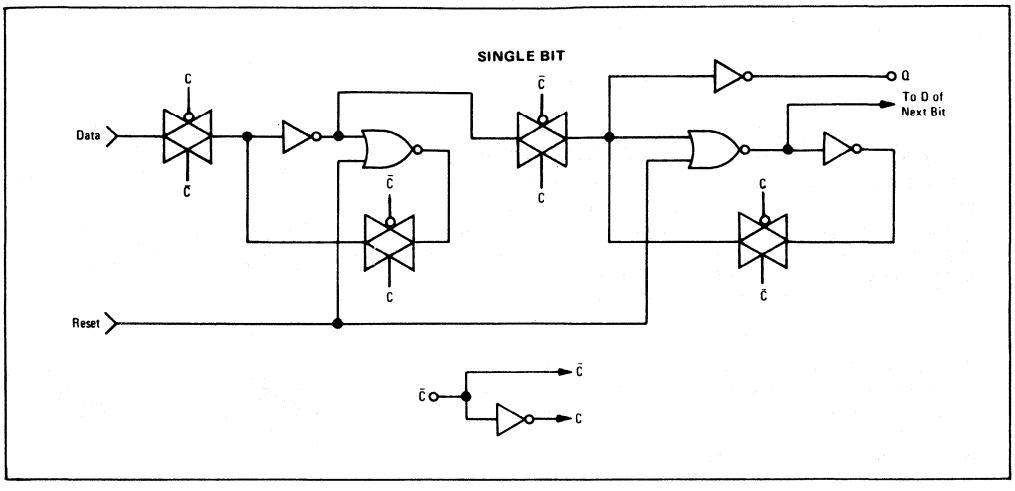
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CIRCUIT SCHEMATICS

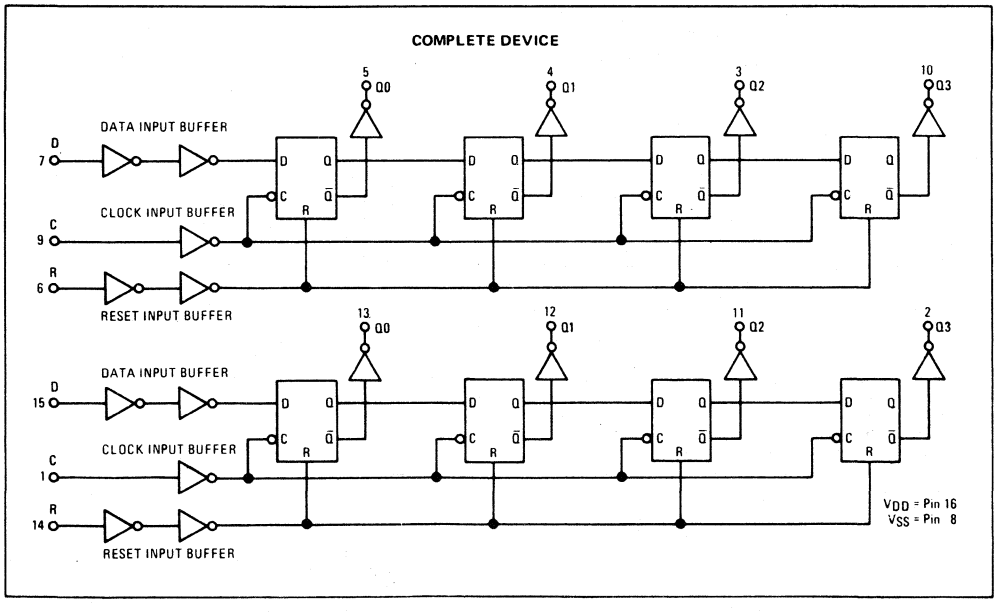


LOGIC DIAGRAMS

SINGLE BIT



COMPLETE DEVICE



MOTOROLA

MC14016B

CMOS SSI

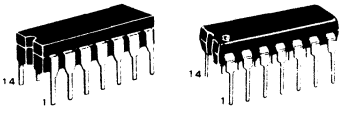
(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH
QUAD MULTIPLEXER

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14016B quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- High On/Off Output Voltage Ratio — 65 dB Typical
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches — 80 dB typical @ 1.0 MHz
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 54 MHz @ 5 Vdc
- Linearized Transfer Characteristics
- Low Noise — 12nV/$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4016B, CD4066B
- This device has Inputs and Outputs which do not have ESD protection. Antistatic precautions must be taken.



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

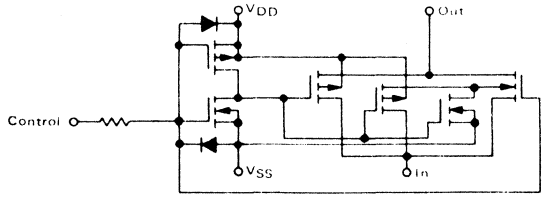
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

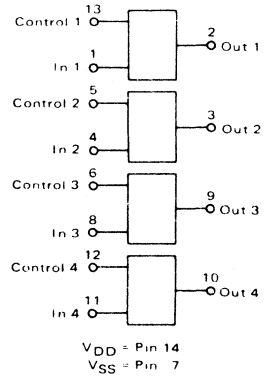
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
Through Current	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the control inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} and V_{out} is not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)



BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

CONTROL	SWITCH
0	OFF
1	ON

ELECTRICAL CHARACTERISTICS

Characteristics	Figure	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Voltage# Control Input	1	V_{IL}	5.0	–	–	–	1.5	0.9	–	–	Vdc
			10	–	–	–	1.5	0.9	–	–	
			15	–	–	–	1.5	0.9	–	–	
		V_{IH}	5.0	–	–	3.5	2.0	–	–	–	Vdc
			10	–	–	8.0	6.0	–	–	–	
			15	–	–	13	11	–	–	–	
Input Current (AL Device) Control	–	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device) Control	–	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance	–	C_{in}									pF
Control			–	–	–	–	5.0	–	–	–	
Switch Input			–	–	–	–	5.0	–	–	–	
Switch Output			–	–	–	–	5.0	–	–	–	
Feed Through			–	–	–	–	0.2	–	–	–	
Quiescent Current (AL Device) (Per Package)	2,3	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
			10	–	0.50	–	0.0010	0.50	–	15	
			15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device) (Per Package)	2,3	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
			10	–	2.0	–	0.0010	2.0	–	15	
			15	–	4.0	–	0.0015	4.0	–	30	
"ON" Resistance (AL Device) ($V_C = V_{DD}$, R_L = 10 kΩ)	4,5,6	R_{ON}									Ohms
(V_{in} = +5.0 Vdc)			5.0	–	600	–	300	660	–	960	
(V_{in} = –5.0 Vdc) V_{SS} = –5 Vdc				–	600	–	300	660	–	960	
(V_{in} = ±0.25 Vdc)				–	600	–	280	660	–	960	
(V_{in} = +7.5 Vdc)			7.5	–	360	–	240	400	–	600	
(V_{in} = –7.5 Vdc) V_{SS} = –7.5 Vdc				–	360	–	240	400	–	600	
(V_{in} = ±0.25 Vdc)				–	360	–	180	400	–	600	
(V_{in} = +10 Vdc)			10	–	600	–	260	660	–	960	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	600	–	260	660	–	960	
(V_{in} = +5.6 Vdc)				–	600	–	310	660	–	960	
(V_{in} = +15 Vdc)			15	–	360	–	260	400	–	600	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	360	–	260	400	–	600	
(V_{in} = +9.3 Vdc)				–	360	–	300	400	–	600	
"ON" Resistance (CL/CP Device) ($V_C = V_{DD}$, R_L = 10 kΩ)	4,5,6	R_{ON}									Ohms
(V_{in} = +5.0 Vdc)			5.0	–	610	–	300	660	–	840	
(V_{in} = –5.0 Vdc) V_{SS} = –5 Vdc				–	610	–	300	660	–	840	
(V_{in} = ±0.25 Vdc)				–	610	–	280	660	–	840	
(V_{in} = +7.5 Vdc)			7.5	–	370	–	240	400	–	520	
(V_{in} = –7.5 Vdc) V_{SS} = –7.5 Vdc				–	370	–	240	400	–	520	
(V_{in} = ±0.25 Vdc)				–	370	–	180	400	–	520	
(V_{in} = +10 Vdc)			10	–	610	–	260	660	–	840	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	610	–	260	660	–	840	
(V_{in} = +5.6 Vdc)				–	610	–	310	660	–	840	
(V_{in} = +15 Vdc)			15	–	370	–	260	400	–	520	
(V_{in} = +0.25 Vdc) V_{SS} = 0 Vdc				–	370	–	260	400	–	520	
(V_{in} = +9.3 Vdc)				–	370	–	300	400	–	520	
Δ"ON" Resistance Between any 2 circuits in a common package ($V_C = V_{DD}$)	–	ΔR_{ON}									Ohms
(V_{in} = ±5.0 Vdc) V_{SS} = –5 Vdc			5.0	–	–	–	15	–	–	–	
(V_{in} = ±7.5 Vdc) V_{SS} = –7.5 Vdc			7.5	–	–	–	10	–	–	–	
Input/Output Leakage Current ($V_C = V_{SS}$)	–	–									µAdc
(V_{in} = +7.5, V_{out} = –7.5 Vdc)			7.5	–	±0.100	–	±0.0015	±0.100	–	±1.0	
(V_{in} = –7.5, V_{out} = +7.5 Vdc)			7.5	–	±0.100	–	±0.0015	±0.100	–	±1.0	

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
Input Voltage specified as the voltage required at the Control Input for a 10 µA current through the transmission gate with an input-to-output stress of $V_{DD} - V_{SS}$ for V_{IL} and V_{IH}.

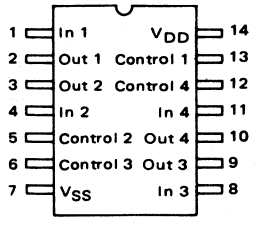
NOTE: All unused control inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

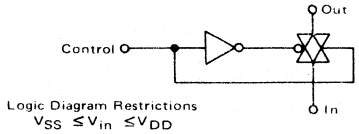
Characteristic	Figure	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Propagation Delay Time (V_{SS} = 0 Vdc)	7	t_{PLH},	5.0	–	15	45	ns
V_{in} to V_{out}		t_{PHL}	10	–	7.0	15	
(V_C = V_{DD}, R_L = 10 kΩ)			15	–	6.0	12	
Control to Output	8		5.0	–	34	90	ns
(V_{in} ≤ 10 Vdc, R_L = 10 kΩ)			10	–	20	45	
			15	–	15	35	
Crosstalk, Control to Output (V_{SS} = 0 Vdc)	9	–	5.0	–	30	–	mV
(V_C = V_{DD}, R_{in} = 1.0 kΩ, R_{out} = 10 kΩ,			10	–	50	–	
f = 1kHz)			15	–	100	–	
Crosstalk between any two switches (V_{SS} = 0 Vdc)	–	–	5.0	–	–80	–	dB
(R_L = 1.0 kΩ, f = 1.0 MHz,							
crosstalk = $20 \log_{10}\frac{V_{out1}}{V_{out2}}$)							
Maximum Control Input Pulse Frequency (V_{SS} = 0 Vdc)	–	–	5.0	–	5.0	–	MHz
(R_L = 1.0 kΩ)			10	–	10	–	
			15	–	12	–	
Noise Voltage (V_{SS} = 0 Vdc)	10,11	–	5.0	–	24	–	nV/√Cycle
(V_C = V_{DD}, f = 100 Hz)			10	–	25	–	
			15	–	30	–	
(V_C = V_{DD}, f = 100 kHz)			5.0	–	12	–	
			10	–	12	–	
			15	–	15	–	
Sine Wave (Distortion) (V_{SS} = -5 Vdc)	–	–	5.0	–	0.16	–	%
(V_{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc,							
R_L = 10 kΩ, f = 1.0 kHz)							
Insertion Loss (V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = -5 Vdc,	12	–	5.0	–			dB
RMS centered = 0.0 Vdc, f = 1.0 MHz)							
$I_{loss} = 20 \log_{10}\frac{V_{out}}{V_{in}}$)							
(R_L = 1.0 kΩ)				–	2.3	–	
(R_L = 10 kΩ)				–	0.2	–	
(R_L = 100 kΩ)				–	0.1	–	
(R_L = 1.0 MΩ)				–	0.05	–	
Bandwidth (-3 dB)	12,13	BW	5.0	–			MHz
(V_C = V_{DD}, V_{in} = 1.77 Vdc, V_{SS} = -5 Vdc,							
RMS centered @ 0.0 Vdc)							
(R_L = 1.0 kΩ)				–	64	–	
(R_L = 10 kΩ)				–	40	–	
(R_L = 100 kΩ)				–	38	–	
(R_L = 1.0 MΩ)				–	37	–	
Feedthrough (V_{SS} = -5 Vdc)	–	–	5.0	–			kHz
(V_C = V_{SS}, $20 \log_{10}\frac{V_{out}}{V_{in}}$ = -50 dB)							
(R_L = 1.0 kΩ)				–	1250	–	
(R_L = 10 kΩ)				–	140	–	
(R_L = 100 kΩ)				–	18	–	
(R_L = 1.0 MΩ)				–	2.0	–	

*The formulae given are for the typical characteristics only.

PIN ASSIGNMENT



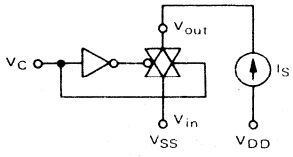
LOGIC DIAGRAM
(1/4 OF DEVICE SHOWN)



Logic Diagram Restrictions
$V_{SS} \leq V_{in} \leq V_{DD}$
$V_{SS} < V_{out} \leq V_{DD}$

$V_{control}$	V_{in} to V_{out} Resistance
V_{SS}	$>10^9$ Ohms typ
V_{DD}	3×10^2 Ohms typ

FIGURE 1 – INPUT VOLTAGE TEST CIRCUIT



V_{IL} = V_C when V_C has been raised from V_{SS} and when I_S = 10 μA
V_{IH} = V_C when V_C has been lowered from V_{DD} and when I_S = 10 μA

3

FIGURE 2 – QUIESCENT POWER DISSIPATION TEST CIRCUIT

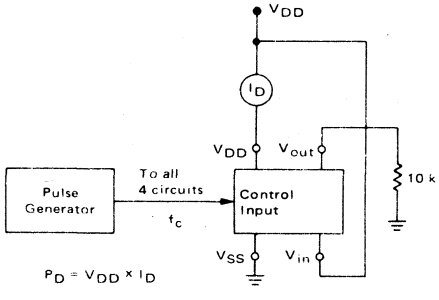
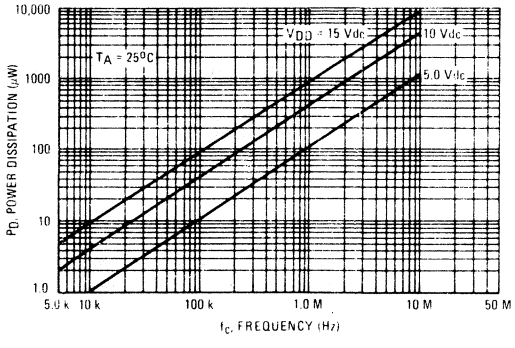


FIGURE 3 – TYPICAL POWER DISSIPATION PER CIRCUIT (1/4 OF DEVICE SHOWN)



TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 4 – V_{SS} = –5.0 V AND –7.5 V

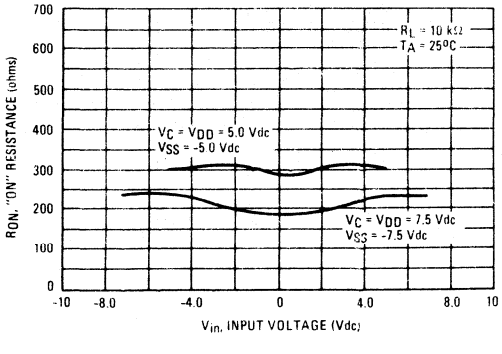


FIGURE 5 – V_{SS} = 0 V

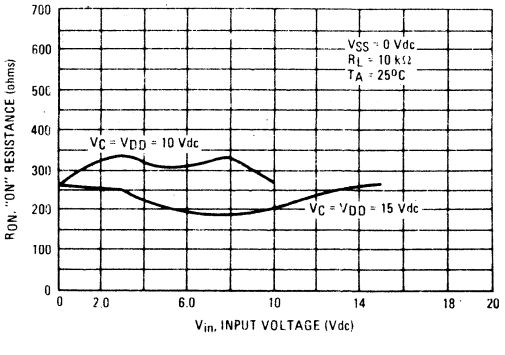


FIGURE 6 – R_{ON} CHARACTERISTICS TEST CIRCUIT

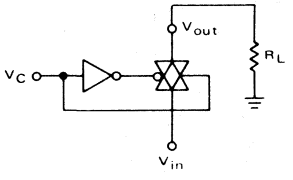
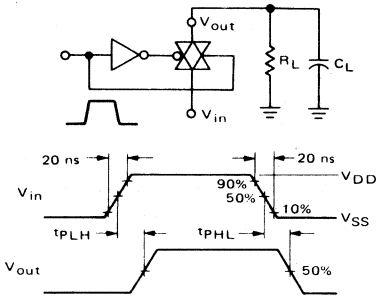


FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS



3

FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

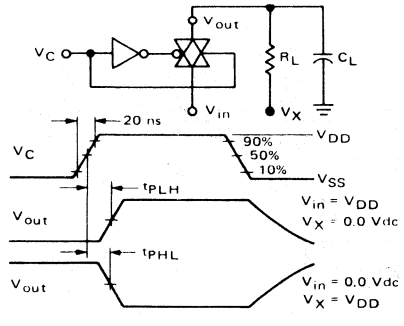


FIGURE 9 – CROSSTALK TEST CIRCUIT

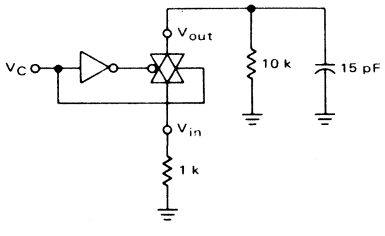


FIGURE 10 – NOISE VOLTAGE TEST CIRCUIT

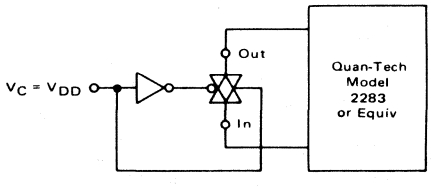


FIGURE 11 – TYPICAL NOISE CHARACTERISTICS

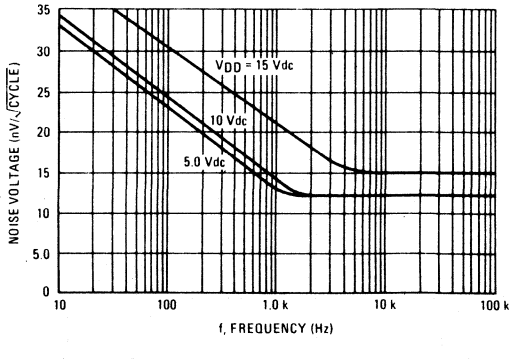


FIGURE 12 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS

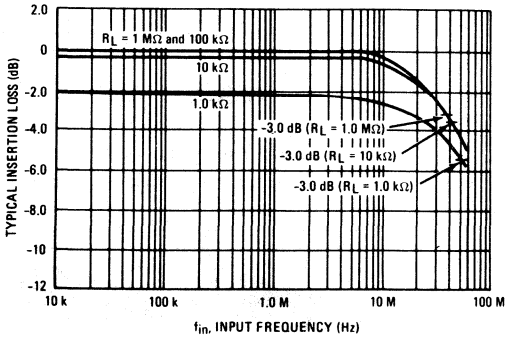
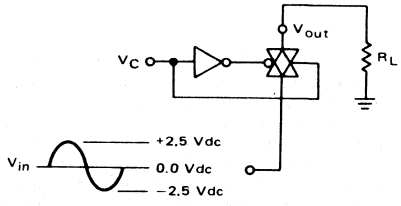


FIGURE 13 – FREQUENCY RESPONSE TEST CIRCUIT



3

MOTOROLA

MC14017B

CMOS MSI

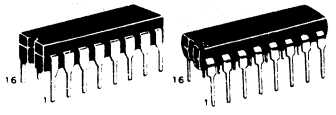
(LOW-POWER COMPLEMENTARY MOS)

DECADE COUNTER/DIVIDER

DECADE COUNTER/DIVIDER

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ V_{DD} = 10 Vdc
- Divide-by-N Counting
- Quiescent Current = 5.0 nA/package Typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B



L SUFFIX	P SUFFIX
CERAMIC PACKAGE	PLASTIC PACKAGE
CASE 620	CASE 648

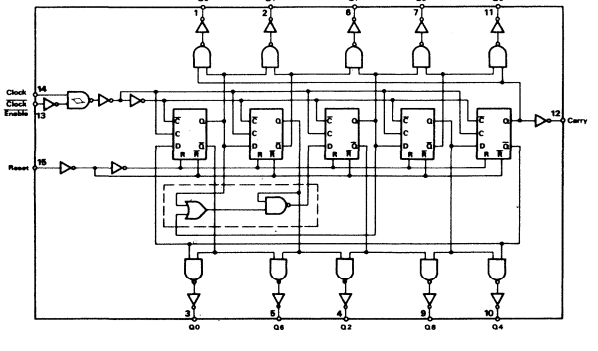
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL, CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



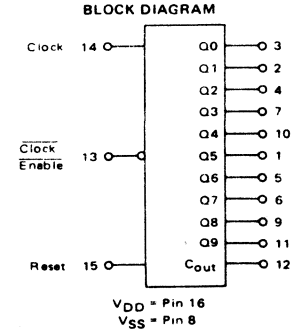
FUNCTIONAL TRUTH TABLE

(Positive Logic)

CLOCK	CLOCK ENABLE	RESET	DECODE OUTPUT = n
0	X	0	n
X	1	0	n
X	X	1	Q0
⎍	0	0	n+1
⎍	X	0	n
X	⎍	0	n
1	⎍	0	n+1

X = Don't Care. If n < 5 Carry = "1", Otherwise = "0"

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.27 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.55 μA/kHz) f + I_{DD}							
		15	I_T = (0.83 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

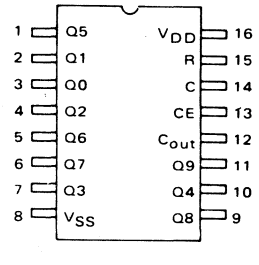
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1.1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN ASSIGNMENT

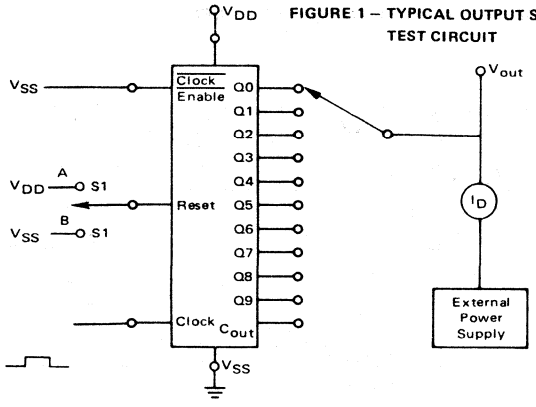


SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Reset to Decade Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns		15	–	175	350	
Propagation Delay Time	t_{PLH},					ns
Clock to C_{out}	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 142 ns		10	–	175	350	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 100 ns		15	–	125	250	
Propagation Delay Time	t_{PLH},					ns
Clock to Decode Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns		15	–	175	350	
Turn-Off Delay Time	t_{PLH}					ns
Reset to C_{out}						
t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH} = (0.66 ns/pF) C_L + 142 ns		10	–	175	350	
t_{PLH} = (0.5 ns/pF) C_L + 100 ns		15	–	125	250	
Clock Pulse Width	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	75	35	–	
Clock Frequency	f_{cl}	5.0	–	5.0	2.0	MHz
		10	–	12	5.0	
		15	–	16	6.7	
Reset Pulse Width	t_{WH}	5.0	500	250	–	ns
		10	250	125	–	
		15	190	95	–	
Reset Removal Time	t_{rem}	5.0	750	375	–	ns
		10	275	135	–	
		15	210	105	–	
Clock Input Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Clock Enable Setup Time	t_{su}	5.0	350	175	–	ns
		10	150	75	–	
		15	115	52	–	
Clock Enable Removal Time	t_{rem}	5.0	420	260	–	ns
		10	200	100	–	
		15	140	70	–	

*The formula given is for the typical characteristics only.

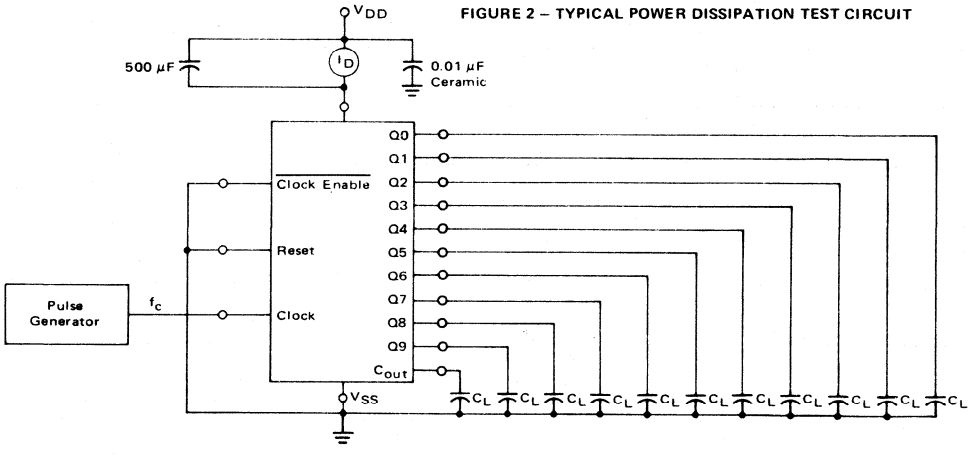
FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



	OUTPUT SINK DRIVE	OUTPUT SOURCE DRIVE
DECODE OUTPUTS	(S1 to A)	Clock to desired outputs (S1 to B)
Carry	Clock to 5 thru 9 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

3

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT



APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 3 – COUNTER EXPANSION

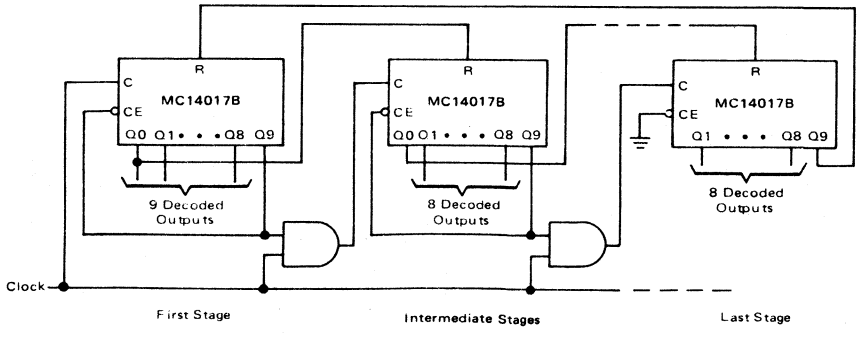
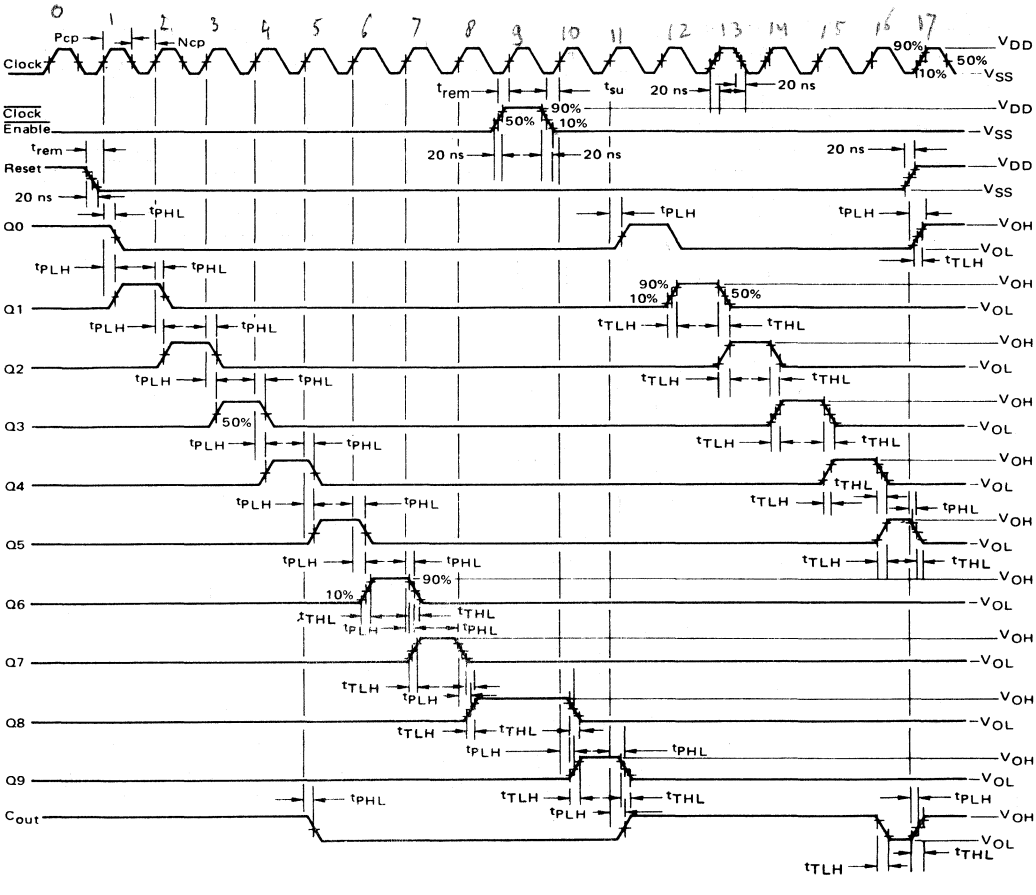


FIGURE 4 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



MOTOROLA

MC14018B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PRESETTABLE DIVIDE-BY-N COUNTER

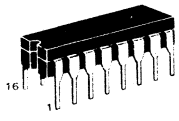
PRESETTABLE DIVIDE-BY-N COUNTER

The MC14018B contains five Johnson counter stages which are asynchronously presettable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

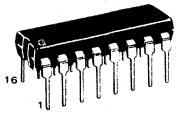
Presetting is accomplished by a logic 1 on the preset enable input. Data on the Jam inputs will then be transferred to their respective $\overline{Q}$ outputs (inverted). A logic 1 on the reset input will cause all $\overline{Q}$ outputs to go to a logic 1 state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate $\overline{Q}$ outputs to the data input, as shown in the Function Selection table. Anti-lock gating is included in the MC14018B to assure proper counting sequence.

- Fully Static Operation
- Medium Speed – 6.5 MHz typical @ 10 V
- Schmitt Trigger on Clock Input
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4018B



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

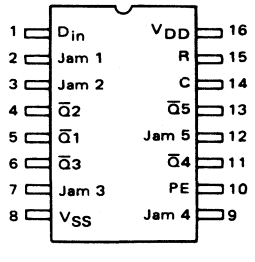
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FUNCTIONAL TRUTH TABLE

Clock	Reset	Preset Enable	Jam Input	$\overline{Q}n$
↓	0	0	X	$\overline{Q}n$
↑	0	0	X	$\overline{D}n^*$
X	0	1	0	1
X	0	1	1	0
X	1	X	X	1

*D_n is the Data input for that stage. Stage 1 has Data brought out to Pin 1.

PIN ASSIGNMENT



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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–			–	5.0	7.5			pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10		10	–	0.010	10		300	
		15		20	–	0.015	20		600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.3 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.7 μA/kHz) f + I_{DD}							
		15	I_T = (1.0 μA/kHz) f + I_{DD}							

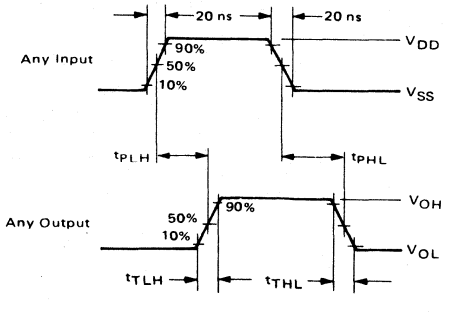
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

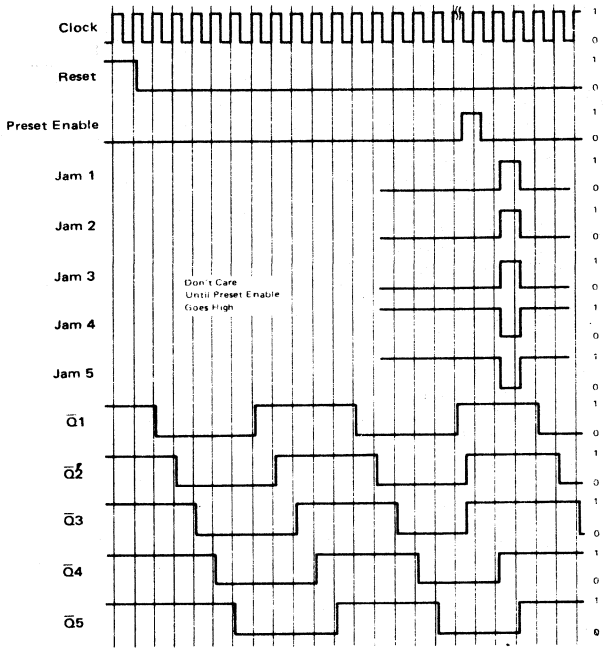
Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to $\overline{Q}$						
t_{PLH},t_{PHL} = (0.90 ns/pF) C_L + 265 ns		5.0	–	310	620	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 102 ns		10	–	120	240	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 72 ns		15	–	85	170	
Reset to $\overline{Q}$						ns
t_{PLH} = (0.90 ns/pF) C_L + 325 ns		5.0	–	370	740	
t_{PLH} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH} = (0.26 ns/pF) C_L + 81 ns		15	–	100	200	
Preset Enable to $\overline{Q}$						ns
t_{PLH},t_{PHL} = (0.90 ns/pF) C_L + 325 ns		5.0	–	370	740	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 81 ns		15	–	100	200	
Setup Time	t_{su}					ns
Data (Pin 1) to Clock		5.0	200	0	–	
		10	100	0	–	
		15	80	0	–	
Jam Inputs to Preset Enable		5.0	200	0	–	ns
		10	100	0	–	
		15	80	0	–	
Data (Jam Inputs)-to-Preset Enable Hold Time	t_h	5.0	540	270	–	ns
		10	500	250	–	
		15	480	240	–	
Clock Pulse Width	t_{WH}	5.0	400	200	–	ns
		10	200	100	–	
		15	160	80	–	
Reset or Preset Enable Pulse Width	t_{WH}	5.0	290	145	–	ns
		10	130	65	–	
		15	110	55	–	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			ns
		10				
		15				
Clock Pulse Frequency	f_{cl}					MHz
		5.0	–	2.5	1.25	
		10	–	6.5	3.25	
		15	–	8.0	4.0	

* The formulae given are for the typical characteristics only.

FIGURE 1 – SWITCHING TIME WAVEFORMS



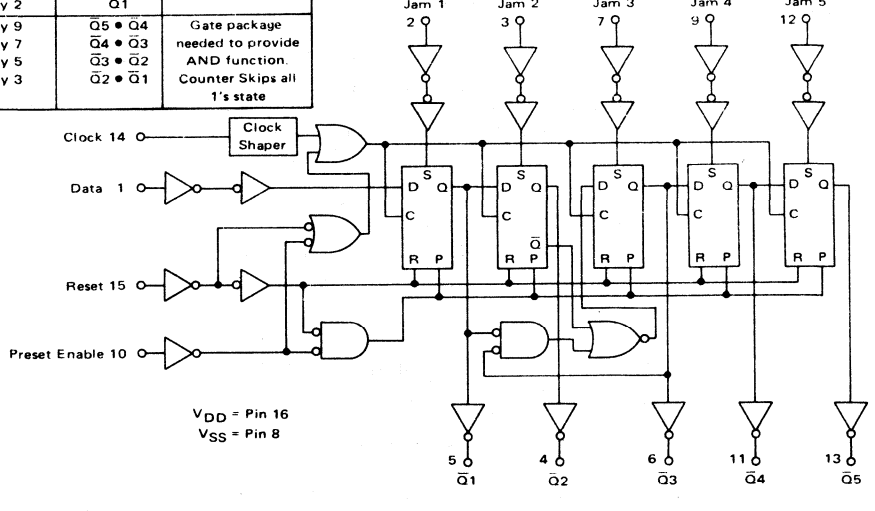
TIMING DIAGRAM
($\overline{Q}5$ Connected to Data Input)



FUNCTION SELECTION

Counter Mode	Connect Data Input (Pin 1) to:	Comments
Divide by 10	$\overline{Q}5$	No external components needed.
Divide by 8	$\overline{Q}4$	
Divide by 6	$\overline{Q}3$	
Divide by 4	$\overline{Q}2$	
Divide by 2	$\overline{Q}1$	
Divide by 9	$\overline{Q}5 \bullet \overline{Q}4$	Gate package needed to provide AND function. Counter Skips all 1's state
Divide by 7	$\overline{Q}4 \bullet \overline{Q}3$	
Divide by 5	$\overline{Q}3 \bullet \overline{Q}2$	
Divide by 3	$\overline{Q}2 \bullet \overline{Q}1$	

LOGIC DIAGRAM



MOTOROLA

MC14020B

14-BIT BINARY COUNTER

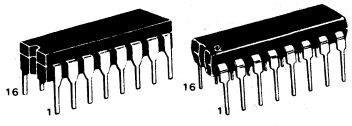
The MC14020B 14-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

- Fully Static Operation
- Quiescent Current =5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Low Input Capacitance = 5.0pF typical
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- 13 MHz Typical Counting Rate @ V_{DD} = 15V
- Pin-for-Pin Replacement for CD4020B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

14-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

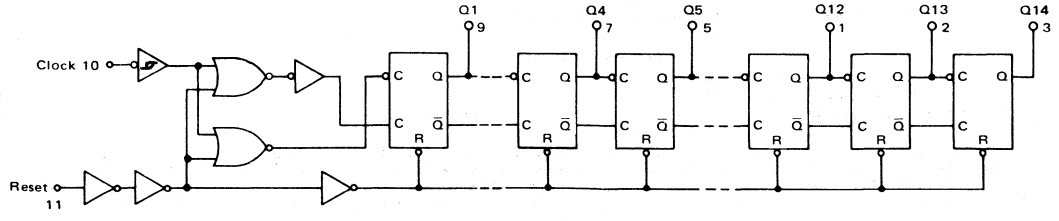
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
⌐	0	No Change
¬	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



Q6 = Pin 4
Q7 = Pin 6
Q8 = Pin 13

Q9 = Pin 12
Q10 = Pin 14
Q11 = Pin 15

V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**†	I_T	5.0	I_T = (0.42 μA/kHz) f + I_{DD}							μAdc
(Dynamic plus Quiescent,		10	I_T = (0.85 μA/kHz) f + I_{DD}							
Per Package)		15	I_T = (1.43 μA/kHz) f + I_{DD}							
(C_L = 50 pF on all outputs, all buffers switching)										

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (CL = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q1						
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	750	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns		10	–	170	300	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 95 ns		15	–	120	230	
Clock to Q14						μs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 2715 ns		5.0	–	2.8	5.6	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 967 ns		10	–	1.0	2.0	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 575 ns		15	–	0.6	1.5	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 510 ns		5.0	–	595	3500	
t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	900	
t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	180	680	
Clock Pulse Width	t_{WH}	5.0	500	140	–	ns
		10	165	55	–	
		15	125	38	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.5	1.0	MHz
		10	–	9.0	3.0	
		15	–	13	4.0	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Reset Pulse Width	t_{WL}	5.0	3000	320	–	ns
		10	550	120	–	
		15	420	80	–	

* The formulae given are for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

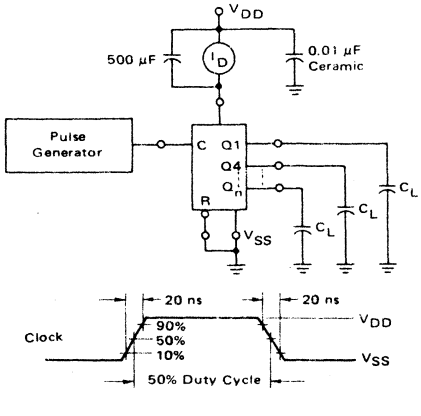


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

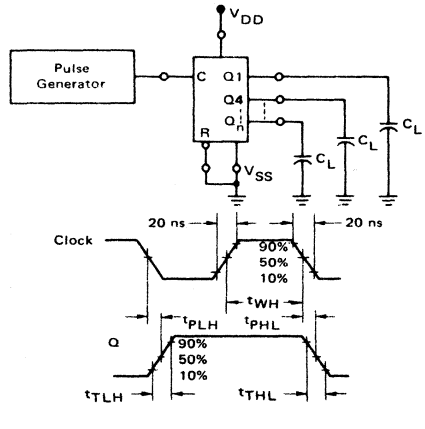
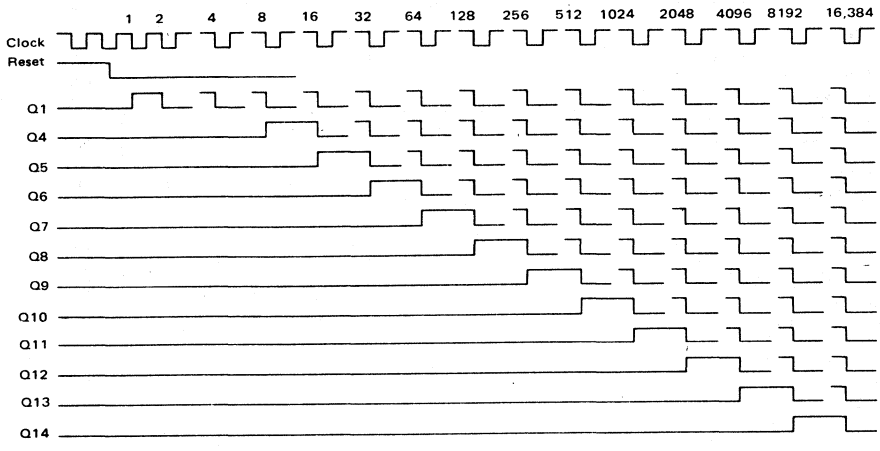
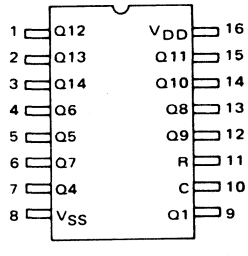


FIGURE 3 – TIMING DIAGRAM



PIN ASSIGNMENT



MOTOROLA

MC14021B

FOR COMPLETE DATA
SEE MC14014B

CMOS MSI

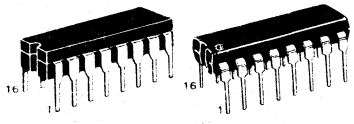
(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER

8-BIT STATIC SHIFT REGISTER

The MC14014B and MC14021B 8-bit static shift registers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel-to-serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- Full Static Operation from DC to typical 6.0 MHz at 10 V V_{DD}
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

SERIAL OPERATION:

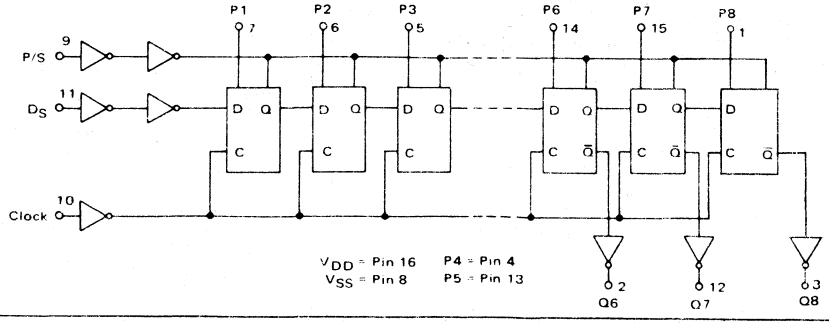
t	CLOCK	D_S	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n		0	0	0	?	?
n+1		1	0	1	0	?
n+2		0	0	0	1	0
n+3		1	0	1	0	1
		X	0	Q6	Q7	Q8

PARALLEL OPERATION:

CLOCK MC14014B	CLOCK MC14021B	D_S	P/S	D_M	$*Q_M$
	X	X	1	0	0
	X	X	1	1	1

*Q6, Q7, & Q8 are available externally
X = Don't Care

LOGIC DIAGRAM



MOTOROLA

MC14022B

CMOS MSI

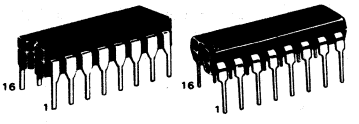
(LOW-POWER COMPLEMENTARY MOS)

OCTAL COUNTER/DIVIDER

OCTAL COUNTER/DIVIDER

The MC14022B is a four-stage Johnson octal counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ V_{DD} = 10 Vdc
- Divide-by-N Counting
- Quiescent Current = 5.0 nA/package Typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4022B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

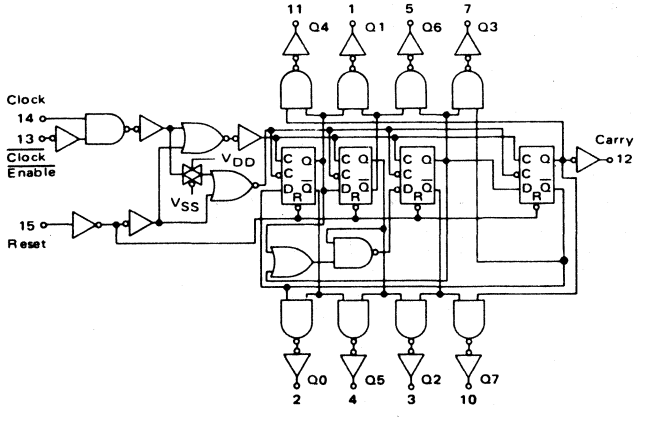
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FUNCTIONAL TRUTH TABLE
(Positive Logic)

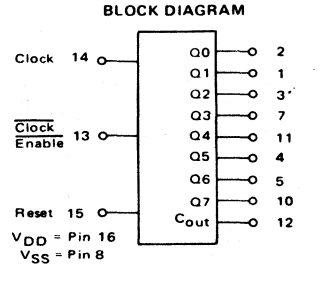
CLOCK	$\overline{\text{CLOCK}}$ ENABLE	RESET	OUTPUT - n
0	X	0	n
X	1	0	n
⌐	0	0	n+1
¬	X	0	n
1	¬	0	n+1
X	⌐	0	n
X	X	1	Q0

X Don't Care If n< 4 Carry = 1, Otherwise = 0

LOGIC DIAGRAM



BLOCK DIAGRAM



NC = Pin 6,9

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	**0.005**	5.0	–	150	µAdc
		10	–	10	–	**0.010**	10	–	300	
		15	–	20	–	**0.015**	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	**0.005**	20	–	150	µAdc
		10	–	40	–	**0.010**	40	–	300	
		15	–	80	–	**0.015**	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.28\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (0.56\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (0.85\ \mu A/kHz)\ f + I_{DD}$							

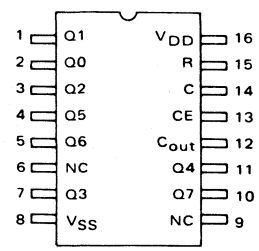
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1.25 \times 10^{-3} (C_L - 50)\ V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



NC = No Connection

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

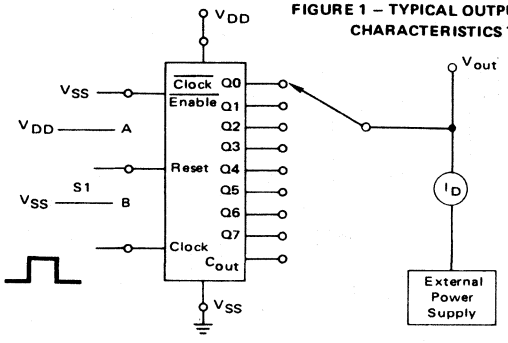
Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Reset to Decode Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns		15	–	175	350	
Propagation Delay Time	t_{PLH},					ns
Clock to C_{out}	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 142 ns		10	–	175	350	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 100 ns		15	–	125	250	
Propagation Delay Time	t_{PLH},					ns
Clock to Decode Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	275	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	125	460	
t_{PLH}, t_{PHL} = 0.5 ns/pF) C_L + 150 ns		15	–	95	350	
Turn-Off Delay Time	t_{PLH}					ns
Reset to C_{out}						
t_{PLH} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH} = (0.66 ns/pF) C_L + 142 ns		10	–	175	350	
t_{PLH} = (0.5 ns/pF) C_L + 100 ns		15	–	125	250	
Clock Pulse Width	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	75	35	–	
Clock Frequency	f_{cl}	5.0	–	5.0	2.0	MHz
		10	–	12	5.0	
		15	–	16	6.7	
Reset Pulse Width	t_{WH}	5.0	500	250	–	ns
		10	250	125	–	
		15	190	95	–	
Reset Removal Time	t_{rem}	5.0	750	375	–	ns
		10	275	135	–	
		15	210	105	–	
Clock Input Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Clock Enable Setup Time	t_{su}	5.0	350	175	–	ns
		10	150	75	–	
		15	115	52	–	
Clock Enable Removal Time	t_{rem}	5.0	420	260	–	ns
		10	200	100	–	
		15	140	70	–	

* The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

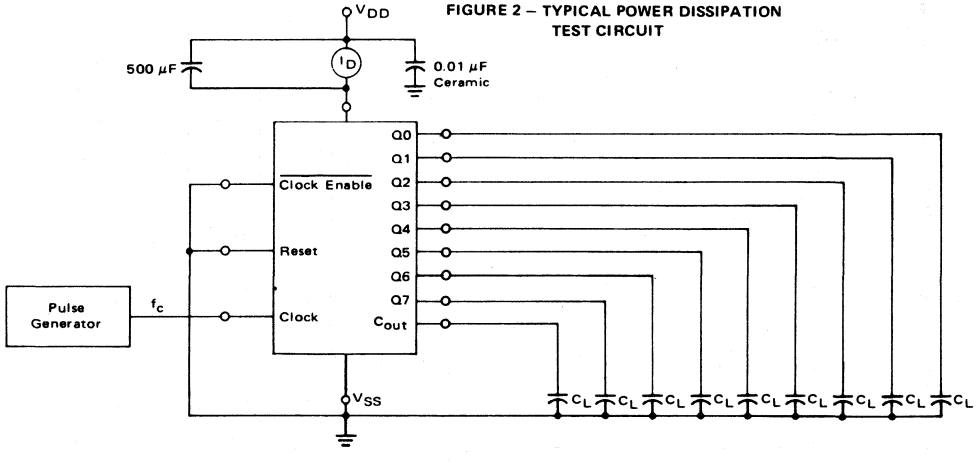
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



	Output Sink Drive	Output Source Drive
Outputs	(S1 to A)	Clock to desired Output (S1 to B)
Carry	Clock to Q5 thru Q7 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT



APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

FIGURE 3 – COUNTER EXPANSION

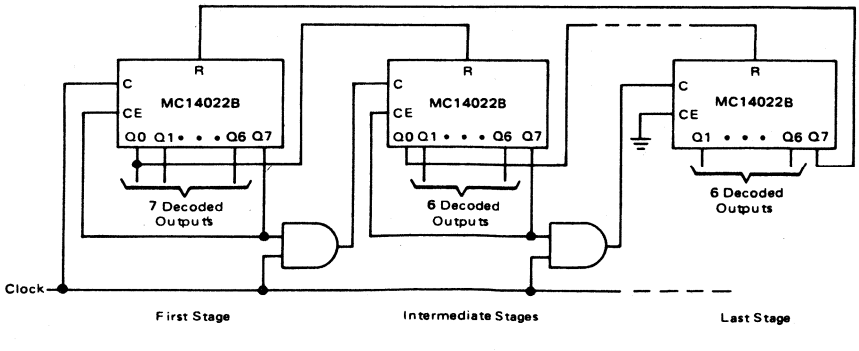
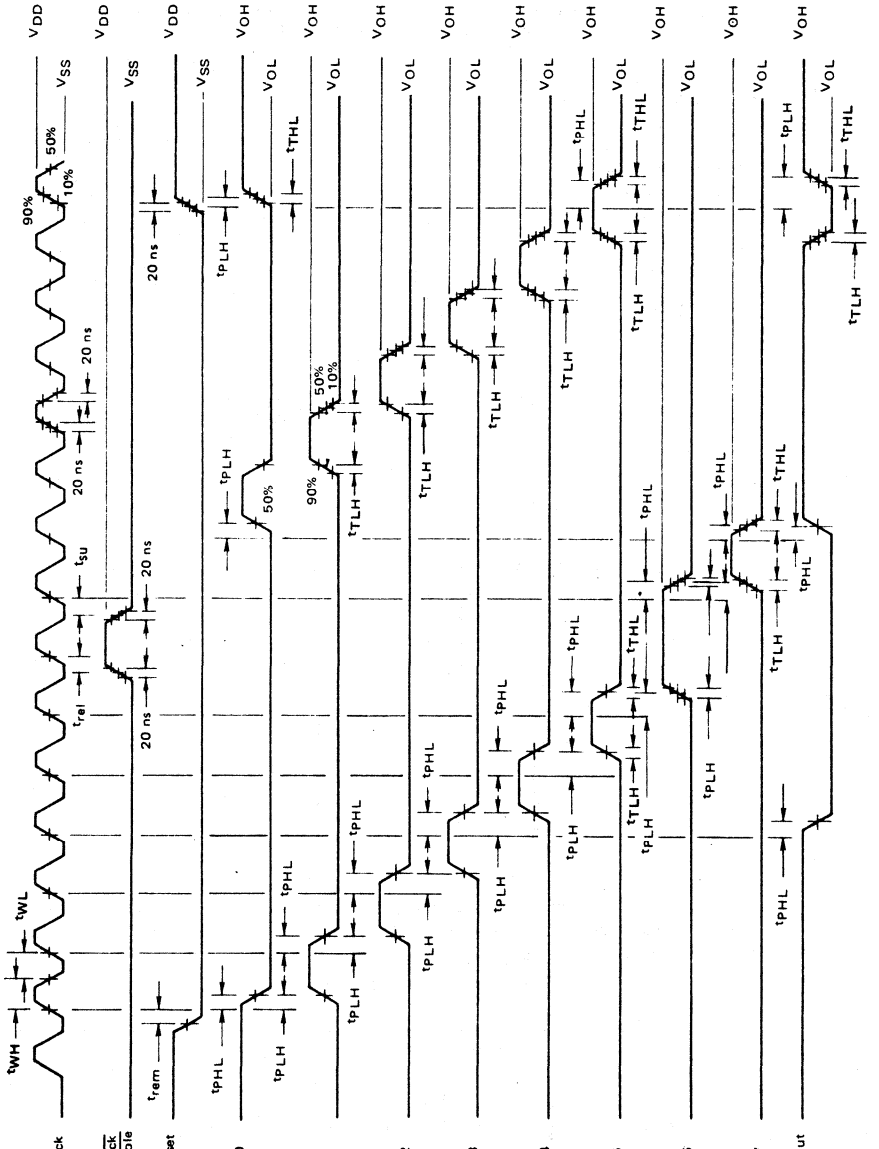


FIGURE 4 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



MOTOROLA

MC14023B
MC14023UB

TRIPLE 3-INPUT "NAND" GATE

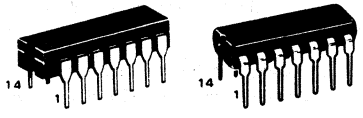
The MC14023B and MC14023UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14023B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14023B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4023B and CD4023UB.

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

or UB, as applicable

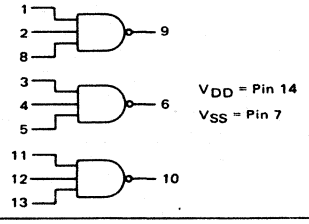
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics of the B-Series device.

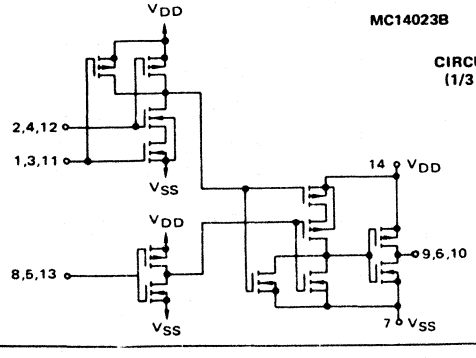
See the MC14001UB data sheet for complete characteristics for the UB device.

LOGIC DIAGRAM

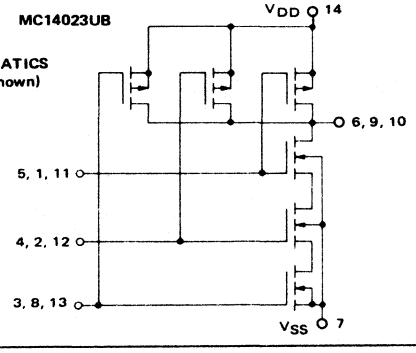


CIRCUIT SCHEMATICS
(1/3 of Device Shown)

MC14023B



MC14023UB



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14024B

CMOS SSI

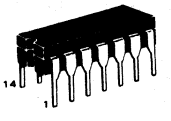
(LOW-POWER COMPLEMENTARY MOS)

SEVEN STAGE
RIPPLE COUNTER

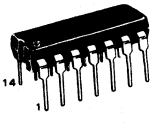
SEVEN STAGE RIPPLE COUNTER

The MC14024B is a seven stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity (typically 45% of V_{DD}), however the $\overline{Clock}$ input has increased noise immunity due to Hysteresis, with no maximum Clock input rise or fall time. The output of each counter stage is buffered.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- 8-MHz Operation @ V_{DD} = 10 Vdc typical
- Exceedingly Slow Input Transition Rates may be Applied to the Clock Input
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4024B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

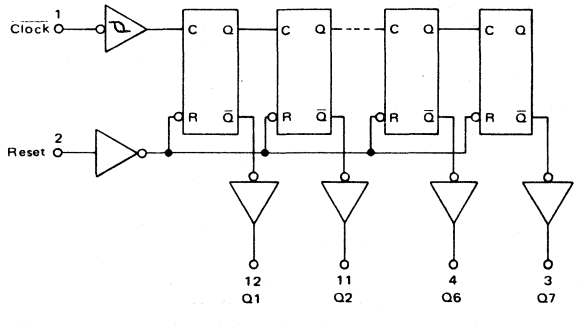
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

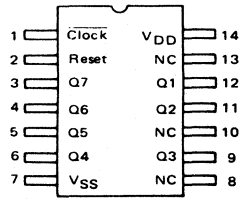
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



Q3 = Pin 9
Q4 = Pin 6
Q5 = Pin 5

PIN ASSIGNMENT



V_{DD} = Pin 14
V_{SS} = Pin 7

NC = No Connection

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage≠ "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.31 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.60 μA/kHz) f + I_{DD}							
		15	I_T = (0.89 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
≠Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q1						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	–	380	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	150	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	175	
Clock to Q7						
t_{PLH}, t_{PHL} = (1,7 ns/pF) C_L + 915 ns		5.0	–	1000	3000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 367 ns		10	–	400	750	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 275 ns		15	–	300	565	
Reset to Q_n						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	–	250	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	180	300	
Clock Pulse Width	t_{WH}	5.0	500	200	–	ns
		10	165	60	–	
		15	125	40	–	
Reset Pulse Width	t_{WH}	5.0	600	375	–	ns
		10	350	200	–	
		15	260	150	–	
Reset Removal Time	t_{rem}	5.0	625	250	–	ns
		10	190	75	–	
		15	145	50	–	
Clock Input Rise and Fall Times	t_{TLH}, t_{THL}	5.0	–	–	0	
		10	–	–	8.0	ms
		15	–	–	200	µs
Input Pulse Frequency	f_{cl}	5.0	–	2.5	1.0	MHz
		10	–	8.0	3.0	
		15	–	12	4.0	

* The formulae given are for the typical characteristics only.

TRUTH TABLE

$\overline{CLOCK}$	RESET	STATE
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
⌐	0	No Change
⌐	1	All Outputs Low
¬	0	Advance One Count
¬	1	All Outputs Low

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

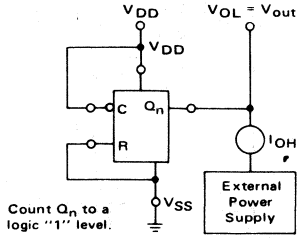
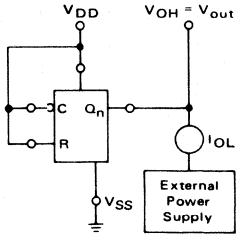
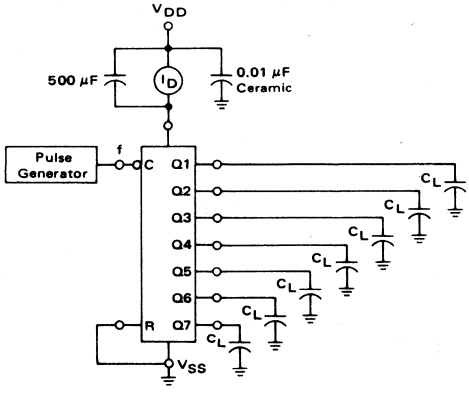


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



3

FIGURE 3 – POWER DISSIPATION TEST CIRCUIT



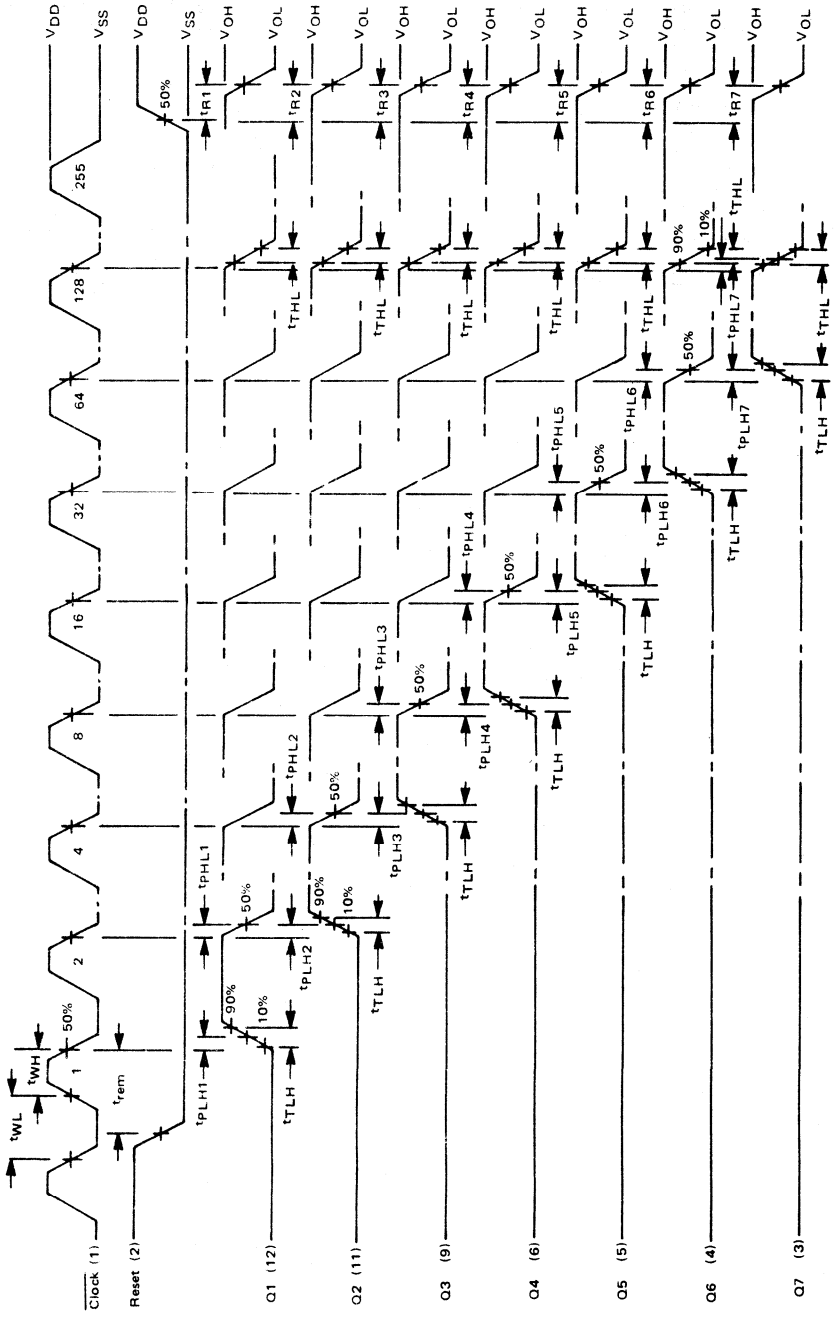


FIGURE 4 – FUNCTIONAL WAVEFORMS

MOTOROLA

MC14025B
MC14025UB

TRIPLE 3-INPUT "NOR" GATE

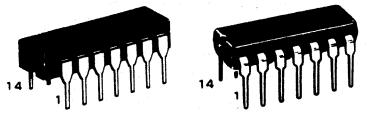
The MC14025B and MC14025UB are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered (MC14025B only)
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14025B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for CD4025B and CD4025UB.

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes
or UB, as applicable
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

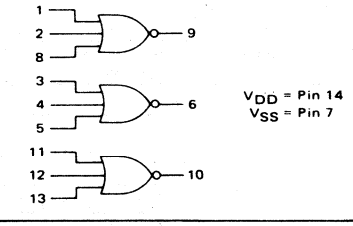
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics of the B-Series device.

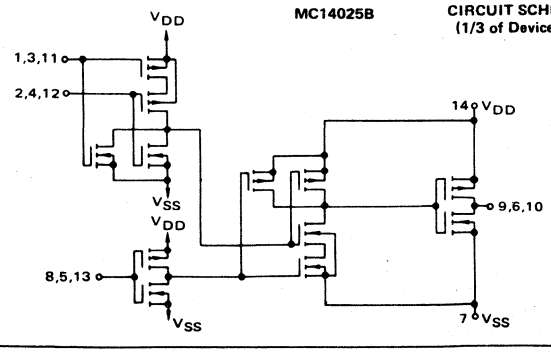
See the MC14001UB data sheet for complete characteristics for the non-B device.

LOGIC DIAGRAM

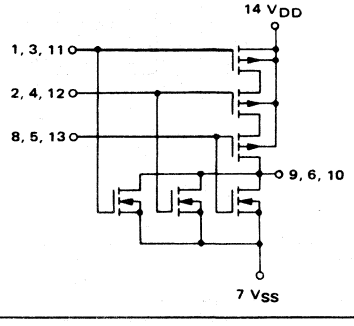


CIRCUIT SCHEMATICS
(1/3 of Device Shown)

MC14025B



MC14025UB



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14027B

DUAL J-K FLIP-FLOP

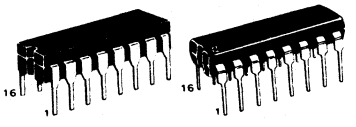
The MC14027B dual J-K flip-flop has independent J, K, Clock (C), Set (S) and Reset (R) inputs for each flip-flop. These devices may be used in control, register, or toggle functions.

- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- Toggle Rate = 3.0 MHz typical @ 5 Vdc
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design – Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4027B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL J-K FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

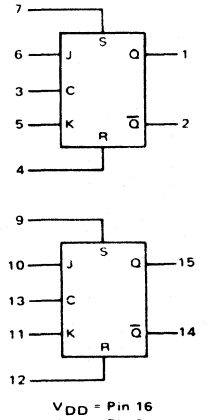
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS						OUTPUTS*		
C†	J	K	S	R	Q_n‡	Q_{n+1}	$\overline{Q_{n+1}}$	
↑	1	X	0	0	0	1	0	
↑	X	0	0	0	1	1	0	
↑	0	X	0	0	0	0	1	
↑	X	1	0	0	1	0	1	
↑	1	1	0	0	Q_0	$\overline{Q_0}$	Q_0	
↓	X	X	0	0	X	Q_n	$\overline{Q_n}$	No Change
X	X	X	1	0	X	1	0	
X	X	X	0	1	X	0	1	
X	X	X	1	1	X	1	1	

X = Don't Care
† = Level Change
‡ = Present State
* = Next State

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

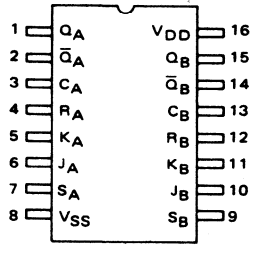
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.80 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.60 µA/kHz) f + I_{DD}							
		15	I_T = (2.40 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT

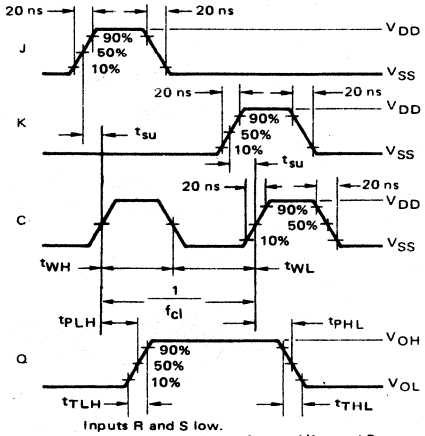


SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Set to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	ns
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	350	450	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	200	ns
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 50 ns		15	–	75	150	
Setup Times	t_{su}	5.0	140	70	–	ns
		10	50	25	–	
		15	35	17	–	
Minimum Hold Times	t_h	5.0	140	70	–	ns
		10	50	25	–	
		15	35	17	–	
Clock Pulse Width	t_{WH}, t_{WL}	5.0	330	165	–	ns
		10	110	55	–	
		15	75	38	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	9.0	4.5	
		15	–	13	6.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5.0	
		15	–	–	4.0	
Set and Reset Pulse Width	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	70	35	–	

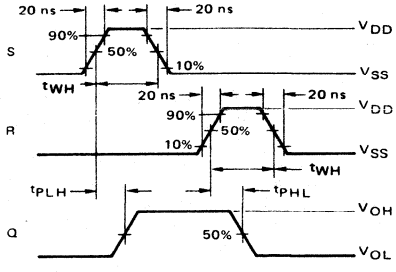
* The formulae given are for the typical characteristics only.

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS
(J, K, Clock, and Output)



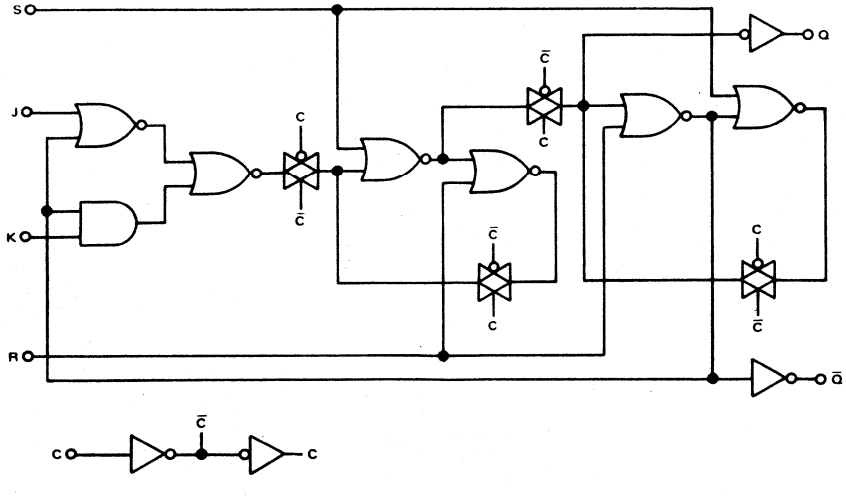
Inputs R and S low.
For the measurement of t_{WH}, $1/f_{cl}$, and P_D the Inputs J and K are kept high.

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, and Output)



Inputs J and K low.

LOGIC DIAGRAM
(1/2 of Device Shown)



MOTOROLA

MC14028B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

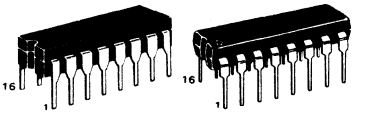
BCD-TO-DECIMAL DECODER BINARY-TO-OCTAL DECODER

3

BCD-TO-DECIMAL DECODER BINARY-TO-OCTAL DECODER

The MC14028B decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0". Expanded decoding such as binary-to-hexadecimal (one-of-16), etc., can be achieved by using other MC14028B devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or read-out decoding.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Positive Logic Design
- Quiescent Current 5.0 nA /package typical @ 5 Vdc
- Low Outputs on All Illegal Input Combinations
- Similar to CD4028B.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

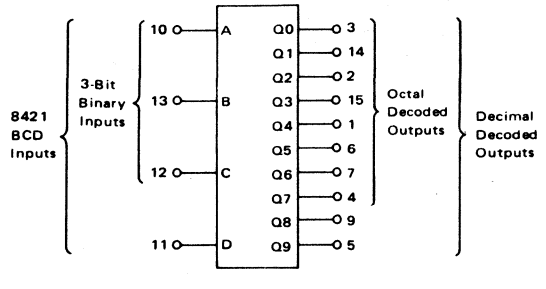
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUT				OUTPUT									
D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

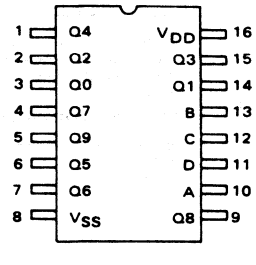
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4		
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.3 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.6 μA/kHz) f + I_{DD}							
		15	I_T = (0.9 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

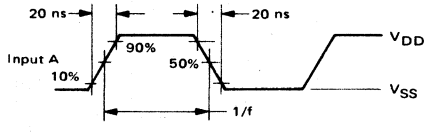
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns	t_{PHL}	5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	

* The formulae given are for the typical characteristics only.

3

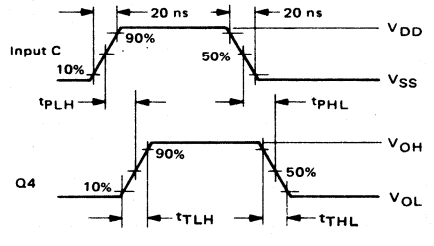
FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS

Inputs B, C, and D switching in respect to a BCD code.



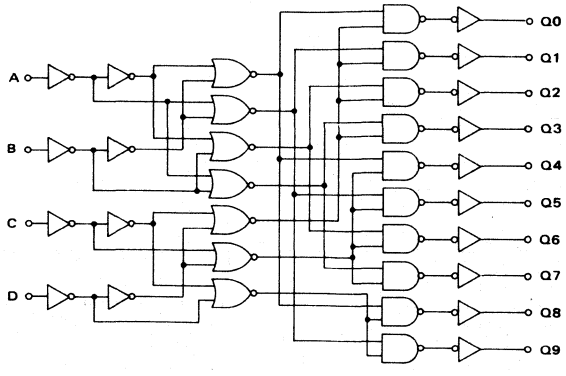
All outputs connected to respective C_L loads. f in respect to a system clock.

Inputs A, B, and D low.



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

LOGIC DIAGRAM

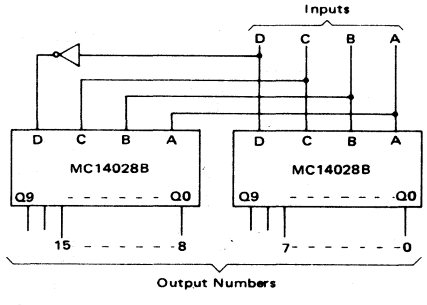


APPLICATION INFORMATION

Expanded decoding can be performed by using the MC14028B and other McMOS Integrated Circuits. The circuits in Figure 2 converts any 4-bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4-bit binary, 4-bit gray, excess-3, or excess-3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6-bit binary 1-of-64 decoder using nine MC14028B circuits and two MC14069B inverters.

The MC14028B can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

FIGURE 2 – CODE CONVERSION CIRCUIT AND TRUTH TABLE



INPUTS				OUTPUT NUMBERS																CODE AND REDEFINED OUTPUT NUMBERS					
																				Hexadecimal		Decimal			
D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4-Bit Binary	4-Bit Gray	Excess-3	Excess-3 Gray	Aiken	4221
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0			0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1			1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3		0	2	2
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	0	3	3	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4	4	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	5	6	2			3
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	6	4	3	1		4
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	7	5	4	2		
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8	15	5			
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	9	14	6			5
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	10	12	7	9		6
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11	13	8		5	
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6	
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7	7
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11		8	8	8
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9	9

FIGURE 3 – SIX-BIT BINARY 1-OF-64 DECODER

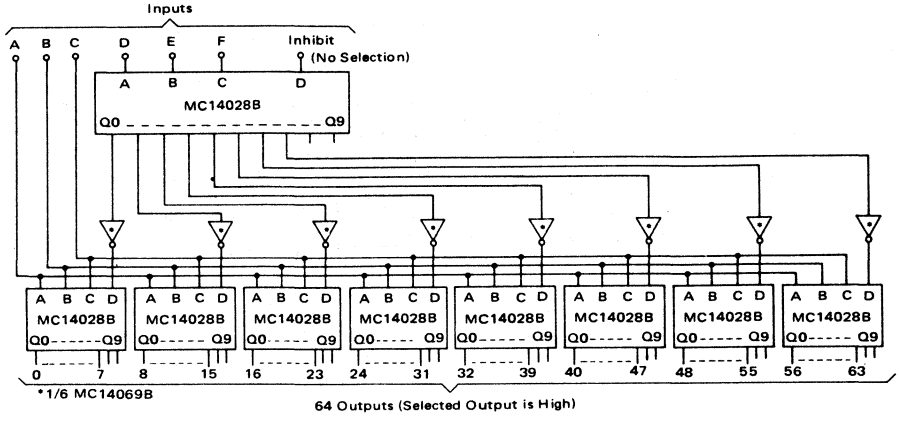
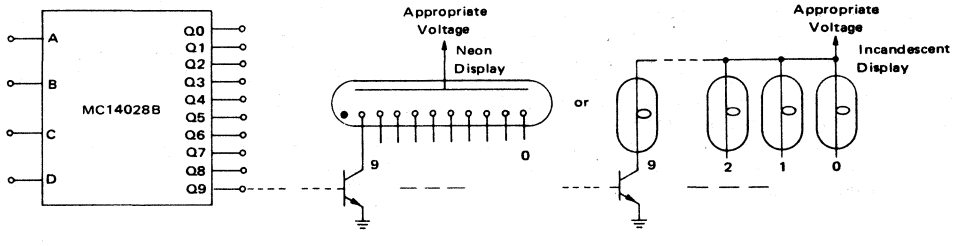


FIGURE 4 – DECIMAL DIGIT DISPLAY APPLICATION



MOTOROLA

MC14029B

BINARY/DECADE UP/DOWN COUNTER

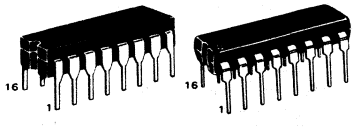
The MC14029B Binary/Decade up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide toggle flip-flop capability. The counter can be used in either Binary or BCD operation. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Quiescent Current = 5.0 nA/package typical @ 5.0 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Proection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance – 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design – Count Occurs on Positive Going Edge of Clock
- 8.0 MHz Counting Rate Typ at 10 Vdc
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin for Pin Replacment for CD4029B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BINARY/DECADE
UP/DOWN COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
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- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

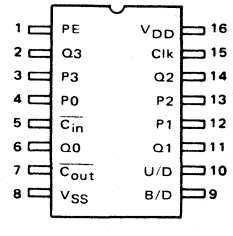
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

$\overline{\text{Carry In}}$	Up/Down	Preset Enable	Action
1	X	0	No Count
0	1	0	Count Up
0	0	0	Count Down
X	X	1	Preset

X = Don't Care

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_r = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_r = (1.5 ns/pF) C_L +15 ns		10	–	50	100	
t_r = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_f = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_f = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_f = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clk to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	90	180	
Clk to $\overline{C_{out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	250	500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	85	190	
$\overline{C_{in}}$ to $\overline{C_{out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns		5.0	–	175	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	–	50	120	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	50	100	
PE to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	235	470	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	80	160	
PE to $\overline{C_{out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	320	640	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	105	210	
Clock Pulse Width	$t_{W(cl)}$	5.0	–	90	180	ns
		10	–	40	80	
		15	–	30	60	
Clock Pulse Frequency	f_{cl}	5.0	2.0	4.0	–	MHz
		10	4.0	8.0	–	
		15	5.0	10	–	
Preset Removal Time**	t_{rem}	5.0	–	80	160	ns
		10	–	40	80	
		15	–	30	60	
Clock Rise and Fall Time	$t_{r(cl)}$	5.0	–	–	15	μs
	$t_{f(cl)}$	10	–	–	5	
		15	–	–	4	
$\overline{Carry}$ In Setup Time	t_{su}	5.0	200	150	–	ns
		10	80	60	–	
		15	55	40	–	
Up/Down Setup Time		5.0	340	170	–	ns
		10	140	70	–	
		15	100	50	–	
Binary/Decade Setup Time		5.0	320	160	–	ns
		10	140	70	–	
		15	100	50	–	
Preset Enable Pulse Width	t_W	5.0	130	65	–	ns
		10	70	35	–	
		15	50	25	–	

*The formulae given are for the typical characteristics only.

**The Preset Signal must be low prior to a positive-going transition of the clock.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

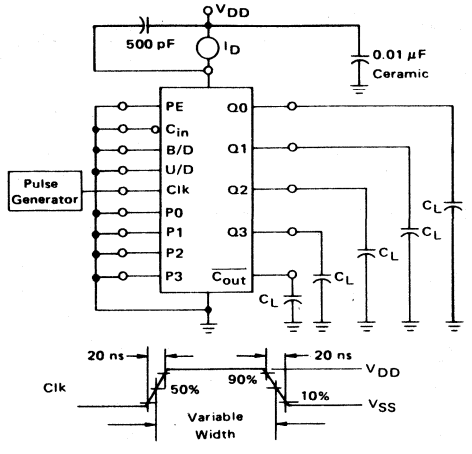
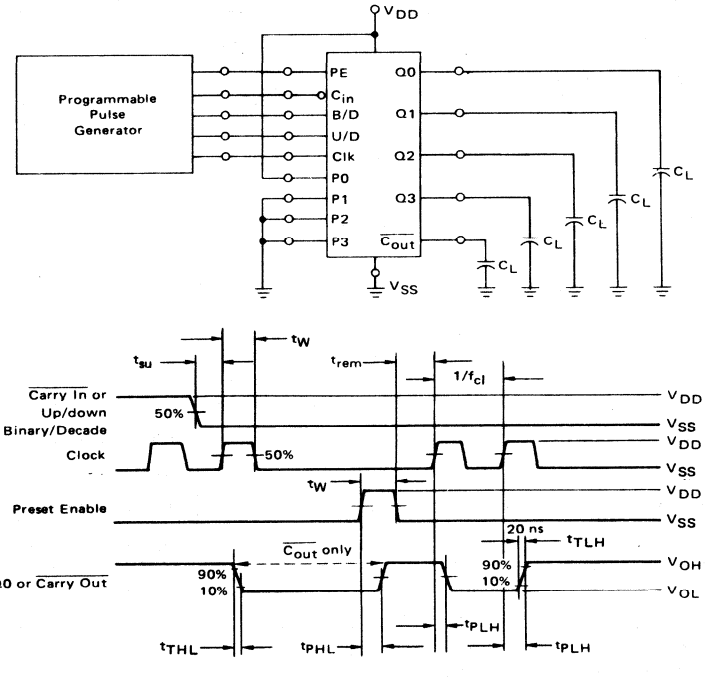


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TIMING DIAGRAM

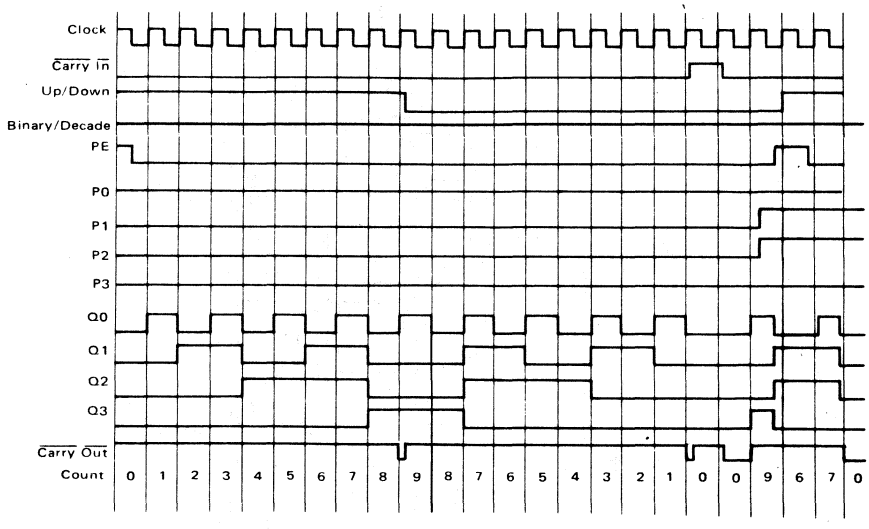
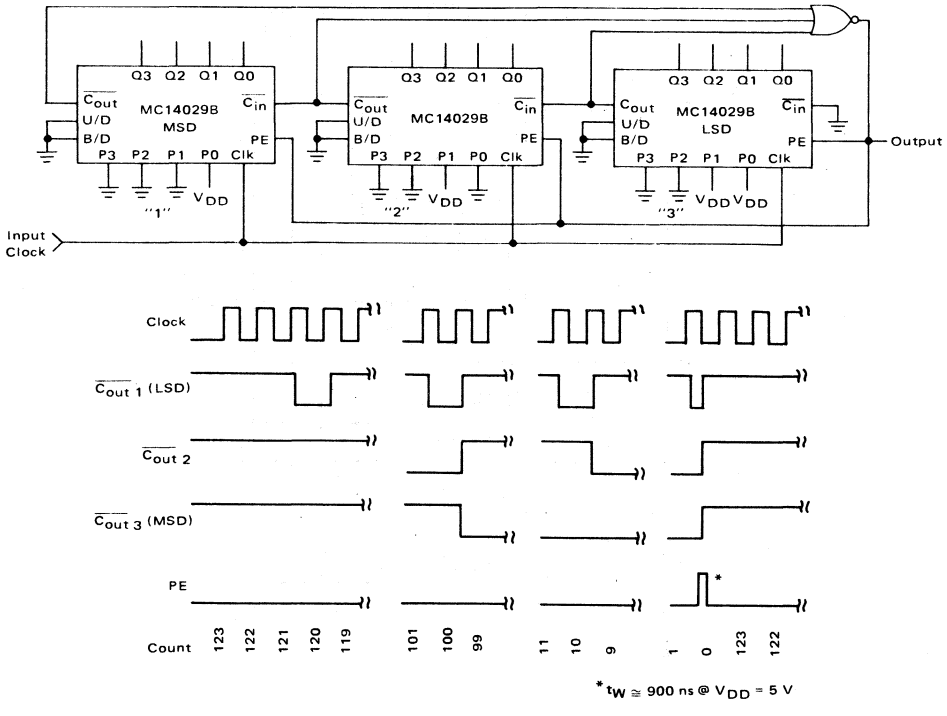
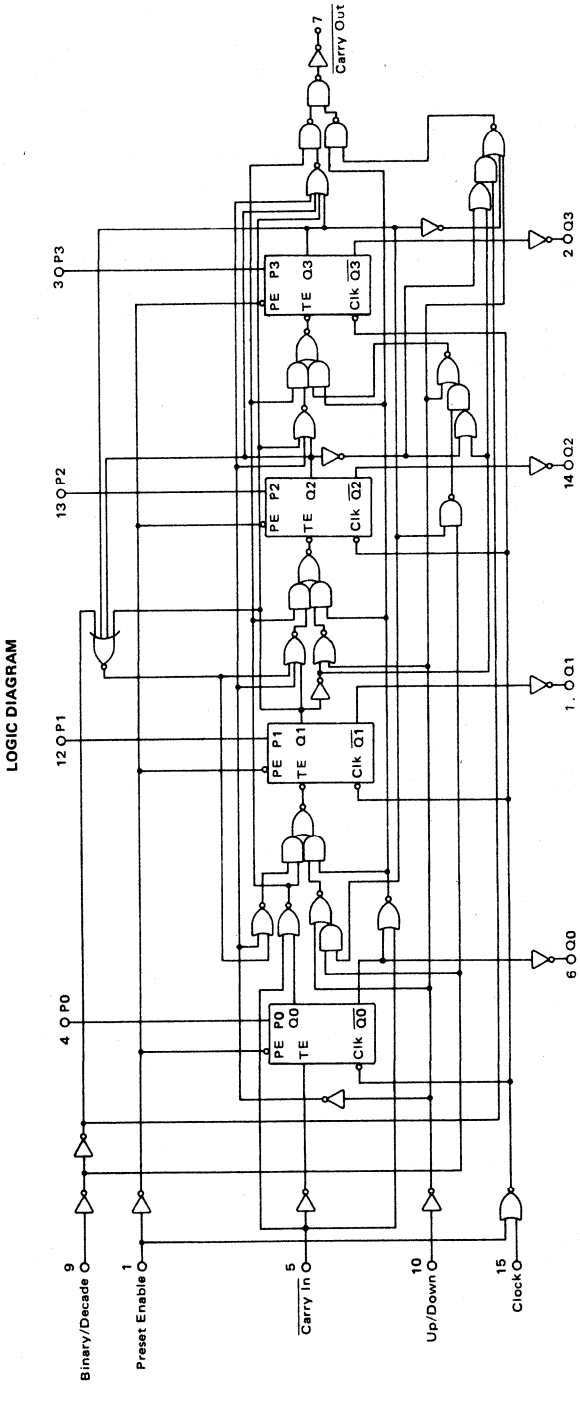


FIGURE 3 – DIVIDE BY N BCD DOWN COUNTER and TIMING DIAGRAM
(Shown for N = 123)



3

LOGIC DIAGRAM



MOTOROLA

MC14032B
MC14038B

CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

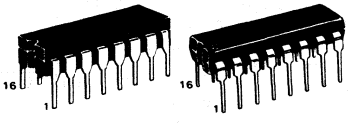
TRIPLE SERIAL ADDERS

Positive Logic – MC14032B
Negative Logic – MC14038B

TRIPLE SERIAL ADDERS

The MC14032B and MC14038B triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032B, and on the negative-going clock transition for the MC14038B. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

- Static Operation from dc to 5.0 MHz
- Buffered Outputs
- Single-Phase Clocking
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4032B and CD4038B.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

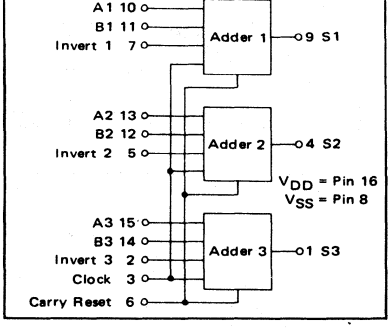
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

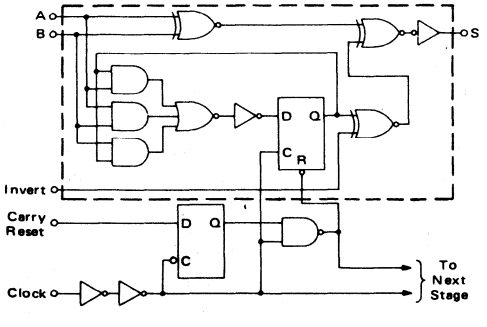
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM

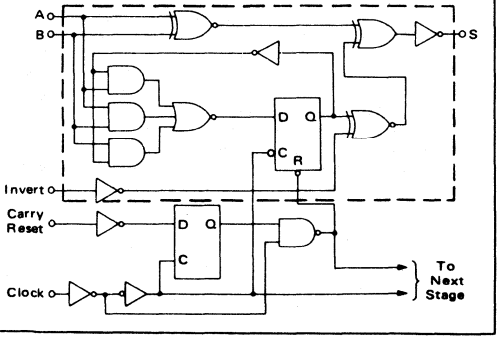


LOGIC DIAGRAMS
(ONE SECTION AND COMMON INPUTS SHOWN)

MC14032B



MC14038B



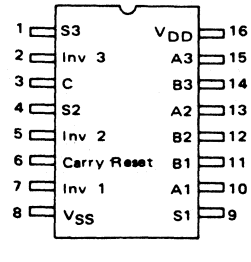
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.96 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.93 µA/kHz) f + I_{DD}							
		15	I_T = (2.8 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT

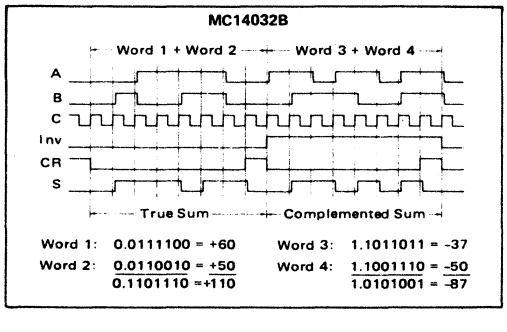


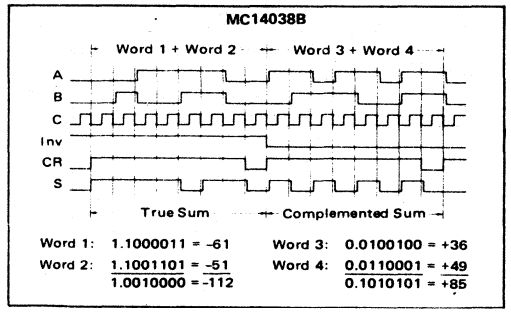
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
A, B or Invert to Sum						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 195 ns		5.0	–	280	1400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns		10	–	120	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	230	
Clock to Sum						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	2400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 110 ns		15	–	135	450	
Input Setup Time	t_{su}	5.0	10	-10	–	ns
		10	10	0	–	
		15	10	0	–	
Clock Pulse Frequency	f_{cl}	5.0	–	4.0	1.0	MHz
		10	–	10	2.5	
		15	–	12	4.0	
Clock Rise and Fall Times	t_{THL}, t_{TLH}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	

* The formulae given are for the typical characteristics only.

TIMING DIAGRAMS





Note: Unused input pins must be connected to either V_{DD} or V_{SS}.

FIGURE 1 – TYPICAL OUTPUT SOURCE TEST CIRCUIT

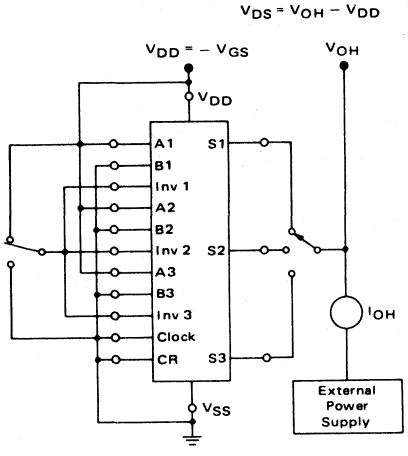


FIGURE 2 – TYPICAL OUTPUT SINK TEST CIRCUIT

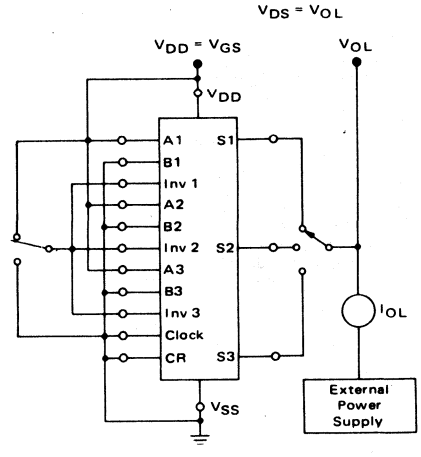
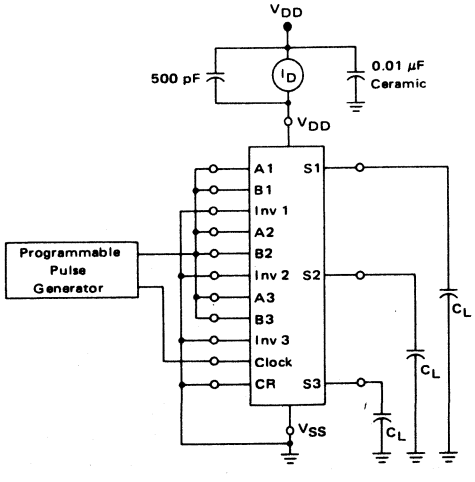


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



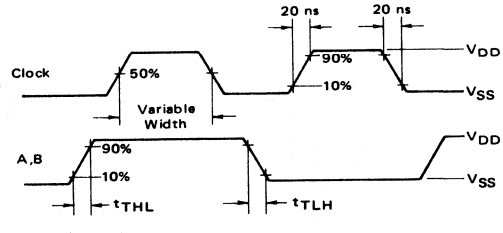
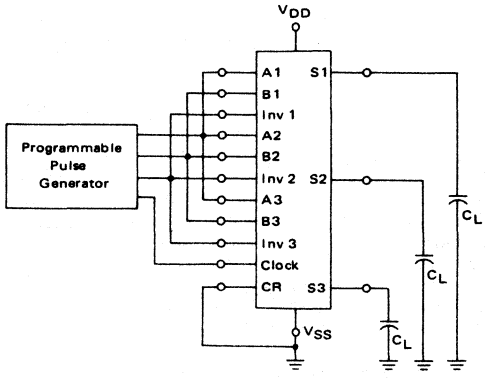
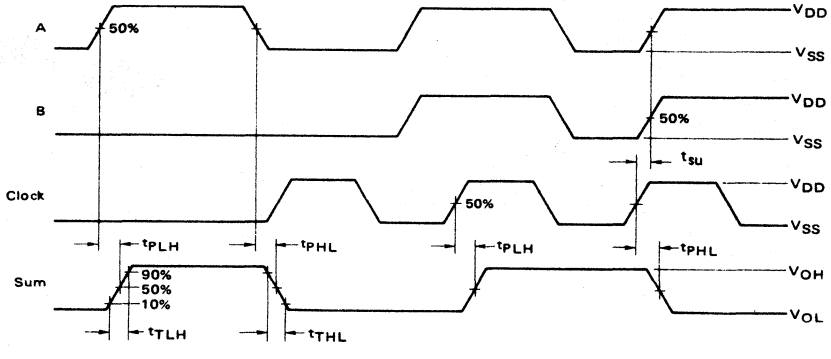


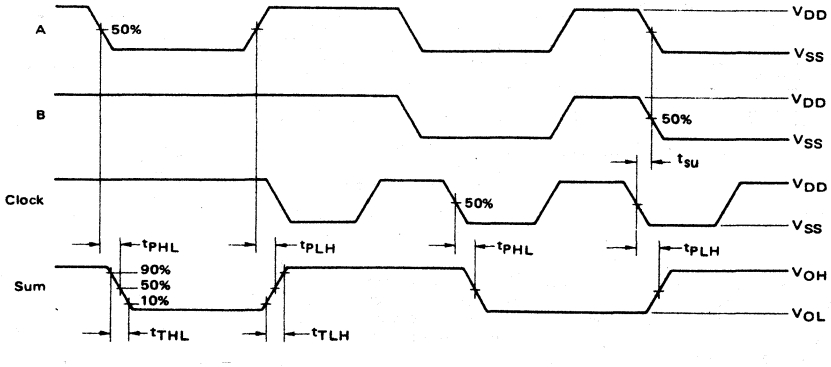
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14032B



MC14038B



MOTOROLA

MC14034B

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

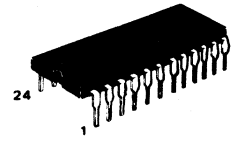
8-BIT UNIVERSAL BUS REGISTER

8-BIT UNIVERSAL BUS REGISTER

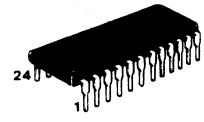
The MC14034B is a bidirectional 8-bit static parallel/serial, input/output bus register. The device contains two sets of input/output lines which allows the bidirectional transfer of data between two buses; the conversion of serial data to parallel form, or the conversion of parallel data to serial form. Additionally the serial data input allows data to be entered shift/right, while shift/left can be accompolished by hard-wiring each parallel output to the previous parallel bit input.

Other useful applications for this device include pseudo-random code generation, sample and hold register, frequency and phase-comparator, address or buffer register, and serial/parallel input/output conversions.

- Bidirectional Parallel Data Input
- Quiescent Current = 10 nA/package typical @ 5 Vdc
- Noise Immunity = 45 % of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Static Operation 0 to 5.0 MHz @ V_{DD} = 10 Vdc
- Single Supply Operation = Positive or Negative
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4034B.



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

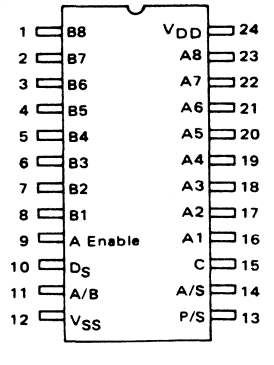
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	−0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	−1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	−0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (2.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (4.4 µA/kHz) f + I_{DD}							
		15	I_T = (6.6 µA/kHz) f + I_{DD}							
3-State Output Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	µAdc
			–		–			–		
3-State Output Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.0001	±1.0	–	±7.5	µAdc
			–		–			–		

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time A or B	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time A or B	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time						
A (B) Synchronous Paralles Data Input,	t_{PLH},					ns
B (A) Parallel Data Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 440 ns		5.0	–	525	1050	
t_{PHL}, t_{PHL} = (0.66 ns/pF) C_L + 172 ns		10	–	205	410	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 120 ns		15	–	145	290	
Propagation Delay Time						
A (B) Asynchronous Parallel Data Input	t_{PLH},					ns
B (A) Parallel Data Output	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 420 ns		5.0	–	505	1010	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	–	130	260	
Clock Pulse Width	t_{WH}	5.0	340	170	–	ns
		10	140	70	–	
		15	110	55	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.2	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Clock Pulse Rise	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
A, B Input Setup Time	t_{su}	5.0	100	35	–	ns
		10	45	15	–	
		15	35	12	–	
High Level SE, P/S, A/S Pulse Width	t_{WH}	5.0	600	200	–	ns
		10	270	90	–	
		15	200	80	–	

*The formulae given are for the typical characteristics only.

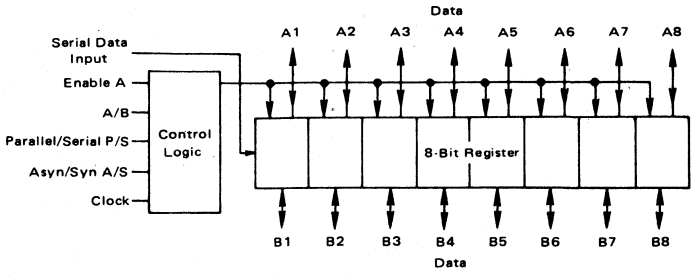
TRUTH TABLE

"A" Enable	P/S	A/B	A/S	MODE	OPERATION†
0	0	0	X	Serial	Synchronous Serial data input, A and B parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs.
1	0	0	X	Serial	Synchronous serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous serial data input, B-Parallel data output.
1	1	0	0	Parallel	B-Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B-Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A-Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A-Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

†Outputs change at positive transition of clock in the serial mode and when the A/S input is low in the parallel mode. During transfer from parallel to serial operation, A/S should remain low in order to prevent D_S transfer into flip-flops.

EXPANDED BLOCK DIAGRAM



OPERATING CHARACTERISTICS

The MC14034B is composed of eight register cells connected in cascade with additional control logic. Each register cell is composed of one "D" master-slave flip-flop with separate internal clocks, and two data transfer gates allowing the data to be transferred bidirectionally from bus A to bus B and from bus B to bus A, and to be memorized. Besides the single phase clock and the serial data inputs, the control logic provides four other features:

A Enable Input – When high, this input enables the bus A data lines.

A/B Input (Data A or B) – This input controls the direction of data flow: when high, the data flows from bus A to bus B; when low, the data flows from bus B to bus A.

P/S Input (Parallel/Serial) – This input controls the data input mode (parallel or serial). When high, the data is transferred to the register in a parallel asynchronous mode or a parallel synchronous mode (positive clock transition). When low, the data is entered into the register in a serial synchronous mode (positive clock transition).

A/S Input (Asynchronous/Synchronous to the Clock) – When this input is high, the data is transferred independently from the clock rate; when low, the clock is enabled and the data is transferred synchronously.

LOGIC DIAGRAM

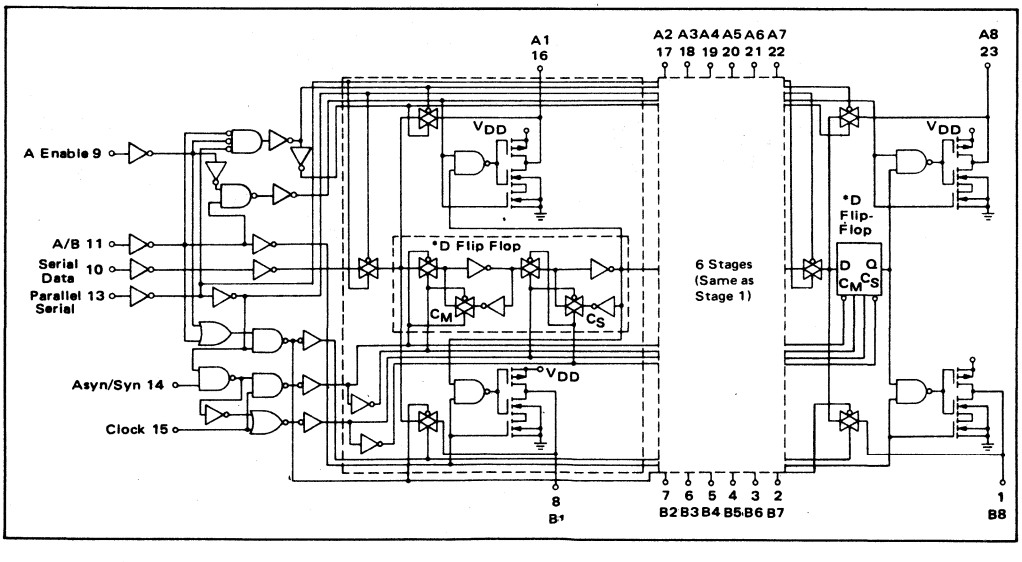
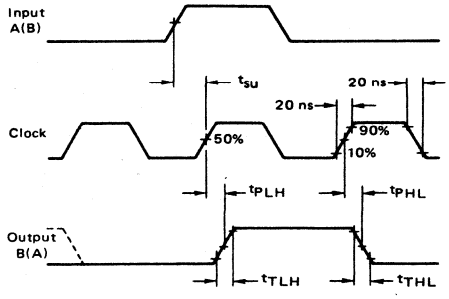


FIGURE 1 – PROPAGATION DELAY AND TRANSITION TIMES WAVEFORMS



3

PROPAGATION AND TRANSITION TIME TEST CIRCUITS

FIGURE 2 – A SYNCHRONOUS DATA INPUT, B PARALLEL DATA OUTPUT AND SETUP TIME

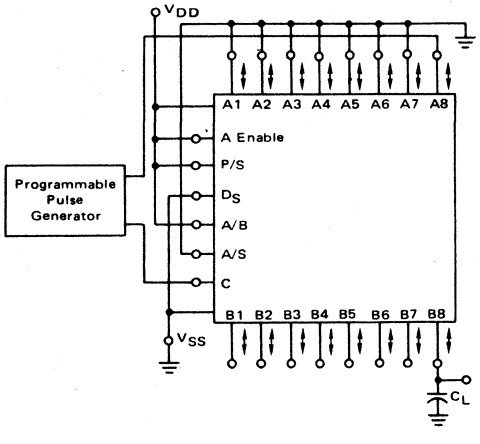


FIGURE 3 – B SYNCHRONOUS DATA INPUT, B PARALLEL DATA OUTPUT AND SETUP TIME

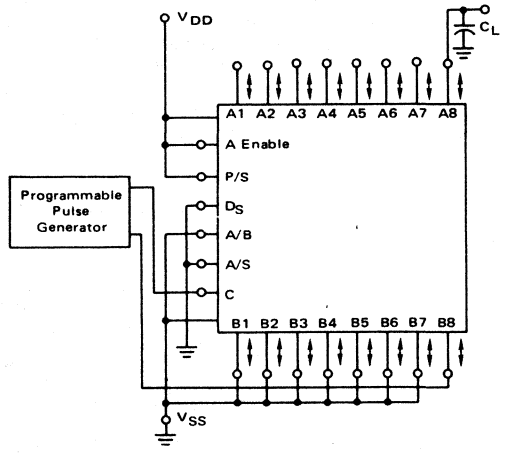


FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

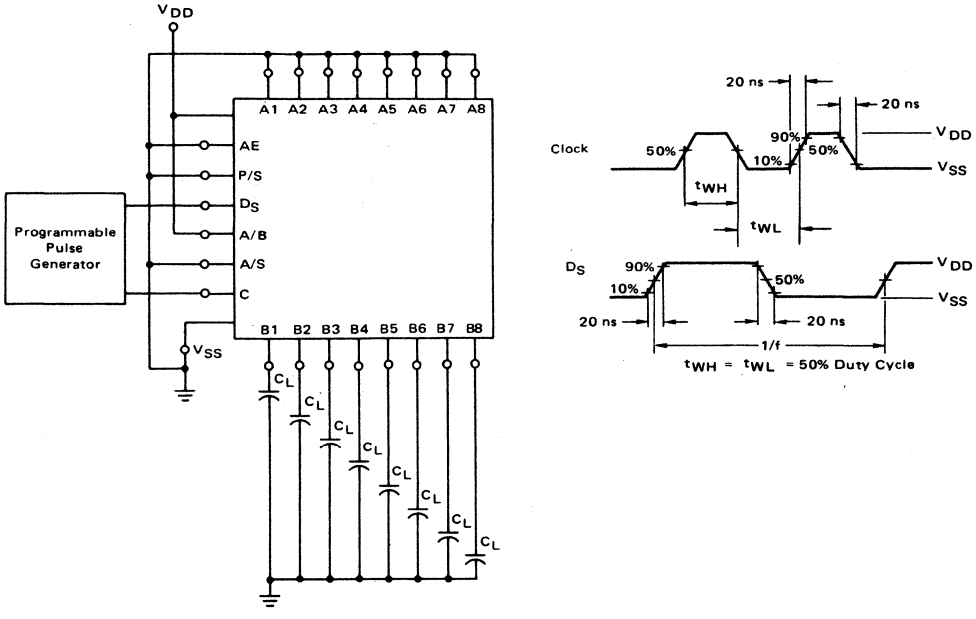


FIGURE 5 – 16-BIT PARALLEL IN/PARALLEL OUT, PARALLEL IN/SERIAL OUT, SERIAL IN/PARALLEL OUT, SERIAL IN/SERIAL OUT REGISTER

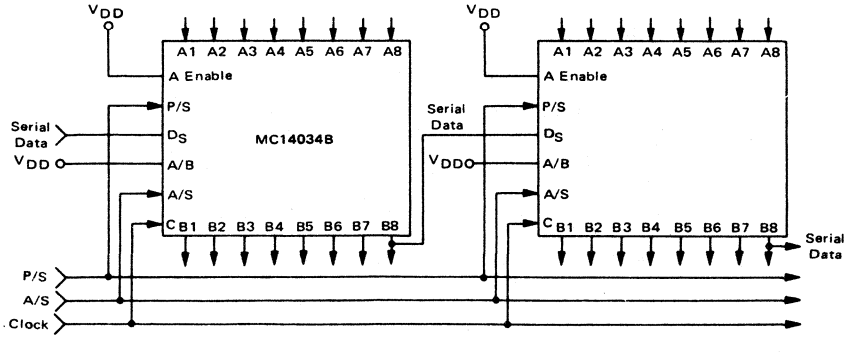
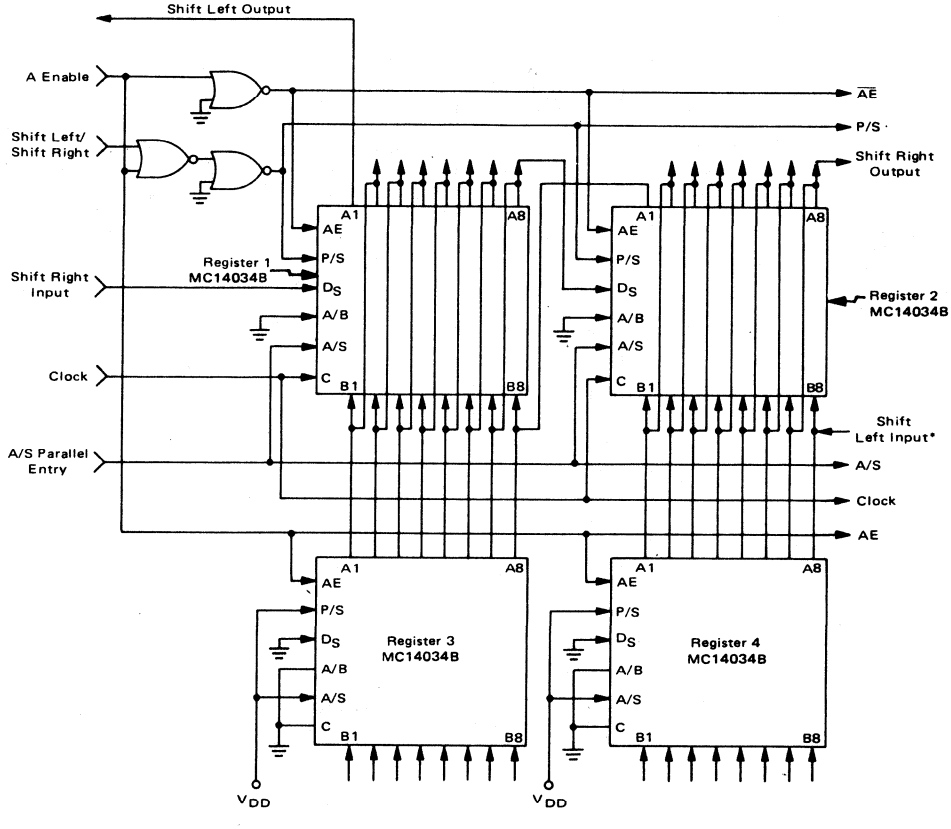


FIGURE 6 – SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUTS



A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

*Shift left input must be disabled during parallel entry.

MOTOROLA

MC14035B

4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

The MC14035B 4-bit shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of a 4-stage clocked serial-shift register with synchronous parallel inputs and buffered parallel outputs. The Parallel/Serial (P/S) input allows serial-right shifting of data or synchronous parallel loading via inputs D_{P0} thru D_{P3}. The True/Complement (T/C) input determines whether the outputs display the Q or $\overline{Q}$ outputs of the flip-flop stages. J-K logic forms the serial input to the first stage. With the J and K inputs connected together they operate as a serial "D" input.

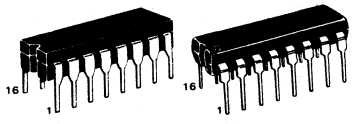
This device may be effectively used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, sample and hold registers, etc. . .

- 4-Stage Clocked Serial-Shift Operation
- Synchronous Parallel Loading of all Four Stages
- J-K Serial Inputs on First Stage
- Asynchronous True/Complement Control of all Outputs
- Fully Static Operation
- Asynchronous Master Reset
- Data Transfer Occurs on the Positive-Going Clock Transition
- No Limit on Clock Rise and Fall Times
- All Inputs are Buffered
- 6.0 MHz Operation @ V_{DD} = 10 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT
PARALLEL-IN/PARALLEL-OUT
SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

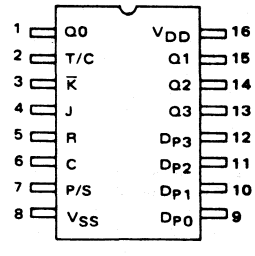
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS				t_n OUTPUT
C	J	$\overline{K}$	R	Q0
⎍	0	0	0	0
⎍	0	1	0	$\overline{Q0}$ (n - 1)
⎍	1	0	0	$\overline{Q0}$ (n - 1)
⎍	1	1	0	1
⎍	x	x	0	Q0 (n-1)
x	x	x	1	0

x = Don't Care
P/S = 0 = Serial Mode
T/C = 1 = True Outputs

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	**0.005**	5.0	–	150	μAdc
		10	–	10	–	**0.010**	10	–	300	
		15	–	20	–	**0.015**	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	**0.005**	20	–	150	μAdc
		10	–	40	–	**0.010**	40	–	300	
		15	–	80	–	**0.015**	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.0\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (2.0\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.0\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

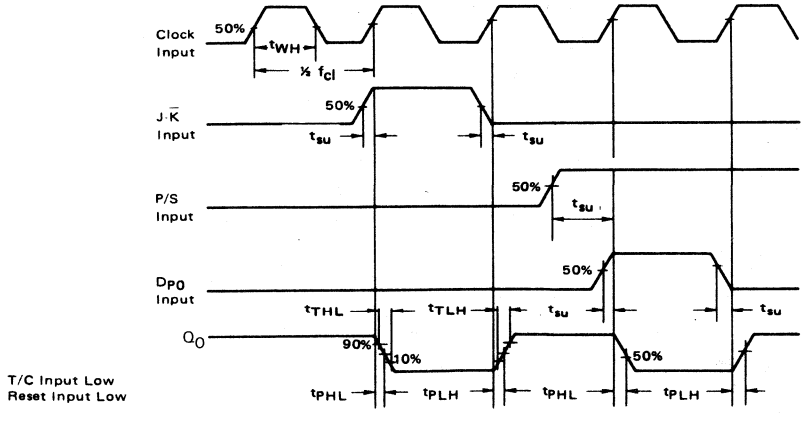
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

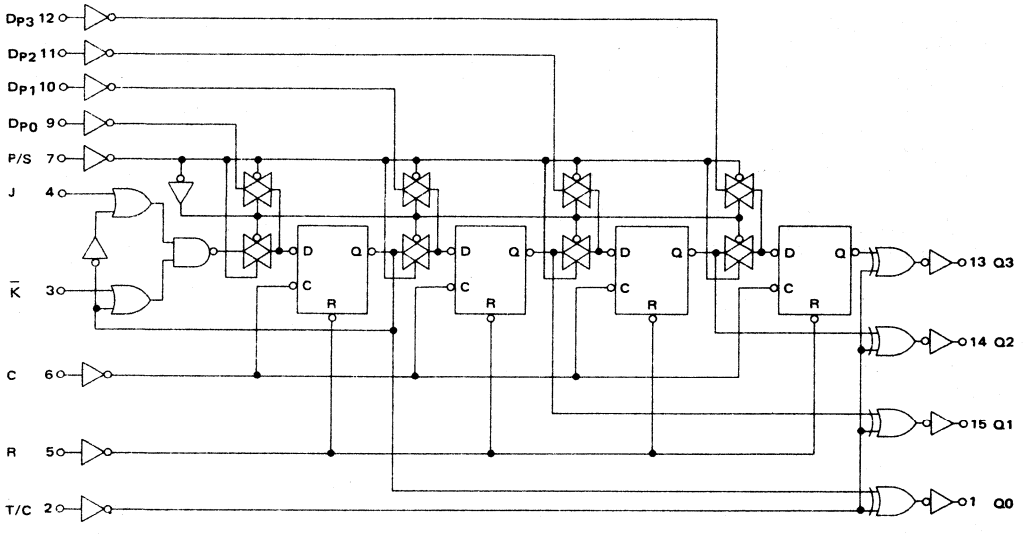
Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 12 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 8.0 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 47 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 24 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 17 ns		15	–	40	80	
Propagation Delay Time, Clock or Reset to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 223 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 89 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 67 ns		15	–	95	190	
Clock Pulse Width	t_{WH}	5.0	335	135	–	ns
		10	165	45	–	
		15	125	40	–	
Reset Pulse Width	t_{WH}	5.0	400	80	–	ns
		10	175	40	–	
		15	130	35	–	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.2	MHz
		10	–	6.0	2.0	
		15	–	10	3.0	
J-K Setup Time	t_{su}	5.0	500	120	–	ns
		10	200	50	–	
		15	150	30	–	
P/S Control Setup Time	t_{su}	5.0	500	25	–	ns
		10	200	10	–	
		15	150	7.5	–	
Parallel Input Setup Time	t_{su}	5.0	500	90	–	ns
		10	200	20	–	
		15	150	15	–	

*The formulae given are for the typical characteristics only.

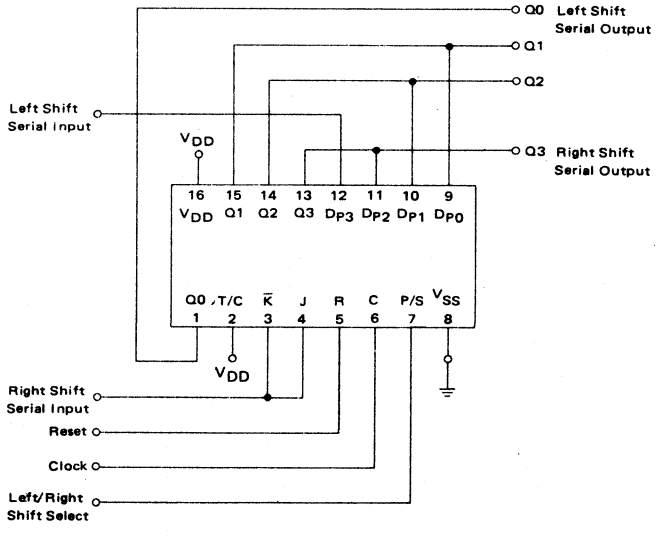
FIGURE 1 – TIMING DIAGRAM



LOGIC DIAGRAM



APPLICATION DIAGRAM
Shift Left/Shift Right Register



MOTOROLA

MC14038B

FOR COMPLETE DATA
SEE MC14032B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

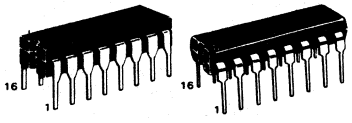
TRIPLE SERIAL ADDERS

Positive Logic – MC14032B
Negative Logic – MC14038B

TRIPLE SERIAL ADDERS

The MC14032B and MC14038B triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032B, and on the negative-going clock transition for the MC14038B. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

- Static Operation from dc to 5.0 MHz
- Buffered Outputs
- Single-Phase Clocking
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin-for-Pin Replacement for CD4032B and CD4038B.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

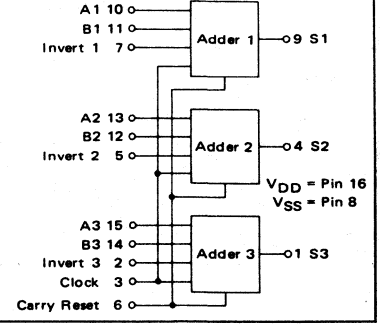
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

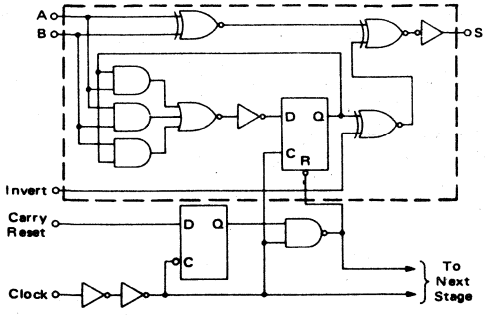
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM

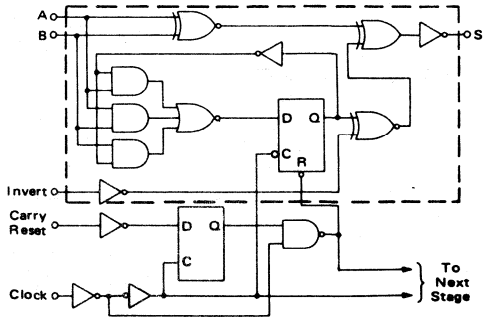


LOGIC DIAGRAMS
(ONE SECTION AND COMMON INPUTS SHOWN)

MC14032B



MC14038B



MOTOROLA

MC14040B

12-BIT BINARY COUNTER

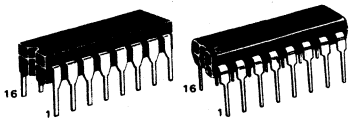
The MC14040B 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Common Reset Line
- 13 MHz Typical Counting Rate @ V_{DD} = 15 V
- Pin-for-Pin Replacement for CD4040B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

12-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

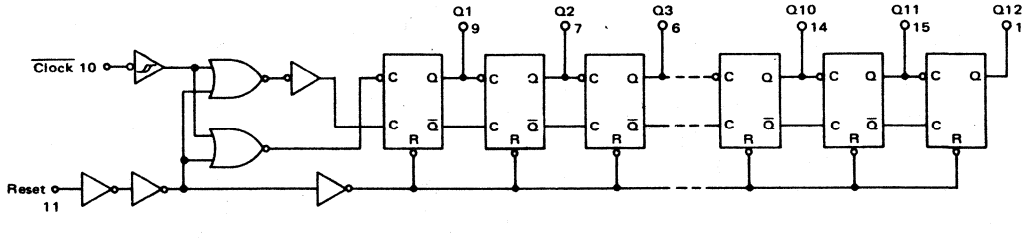
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
↑	0	No Change
↓	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

LOGIC DIAGRAM



Q4 = Pin 5 Q7 = Pin 4 V_{DD} = Pin 16
Q5 = Pin 3 Q8 = Pin 13 V_{SS} = Pin 8
Q6 = Pin 2 Q9 = Pin 12

ELECTRICAL CHARACTERISTICS

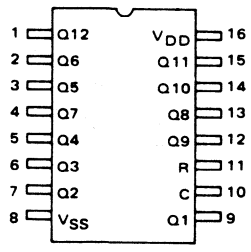
Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.42 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.85 µA/kHz) f + I_{DD}							
		15	I_T = (1.43 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q1						
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 315 ns	t_{PHL}	5.0	–	400	800	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 137 ns		10	–	170	340	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 95 ns		15	–	120	240	
Clock to Q12						µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 2415 ns		5.0	–	2.5	5.0	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 867 ns		10	–	0.9	1.8	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 475 nd		15	–	0.5	1.4	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 485 ns		5.0	–	570	1620	
t_{PHL} = (0.66 ns/pF) C_L + 182 ns		10	–	215	600	
t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	450	
Clock Pulse Width	t_{WH}	5.0	385	140	–	ns
		10	150	55	–	
		15	115	38	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.1	1.5	MHz
		10	–	7.0	3.5	
		15	–	10.0	4.5	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			ns
		10				
		15				
Reset Pulse Width	t_{WH}	5.0	960	320	–	ns
		10	360	120	–	
		15	270	80	–	

* The formulae given are for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

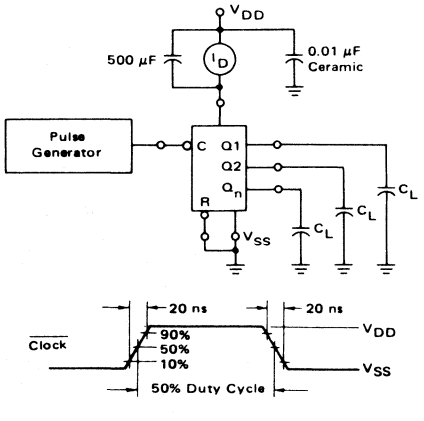


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

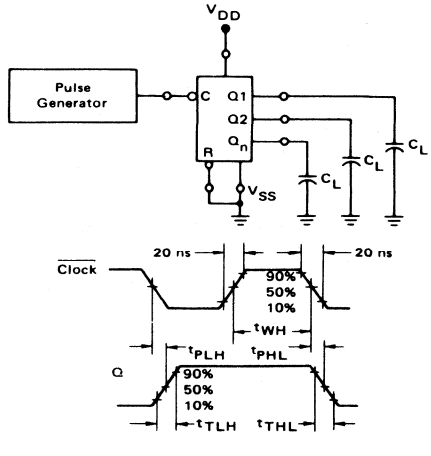
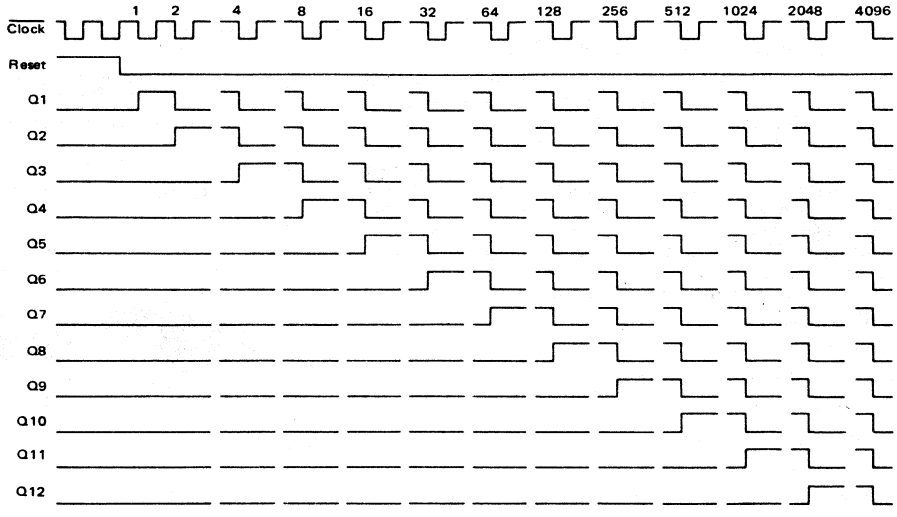


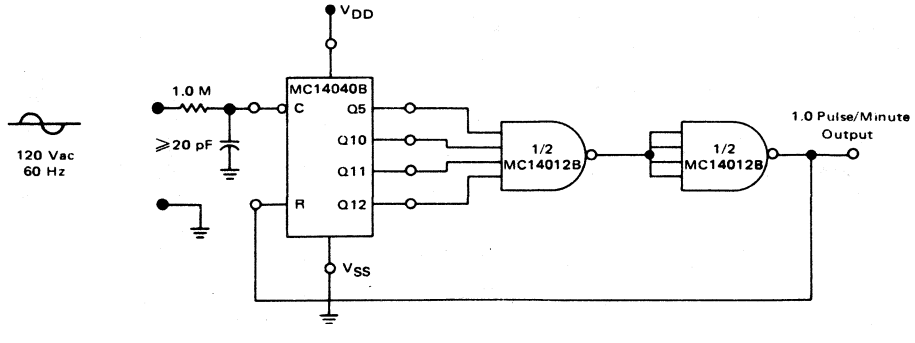
FIGURE 3 – TIMING DIAGRAM



APPLICATIONS INFORMATION

TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040B. By selecting outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14012B decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

MOTOROLA

MC14042B

QUAD TRANSPARENT LATCH

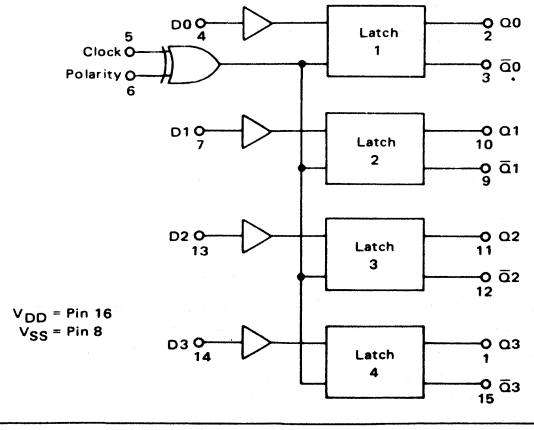
The MC14042B Quad Transparent Latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe data through the latches can be reversed using the polarity input. Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the clock level which is determined by the polarity input. When the polarity input is in the logic "0" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level.

- Buffered Data Inputs
- Common Clock
- Positive or Negative Edge Clocked
- Q and $\overline{Q}$ Outputs
- Double Diode Input Protection
- No Limit on Clock Rise or Fall Times
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

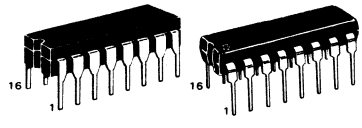
LOGIC DIAGRAM



CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD
TRANSPARENT LATCH



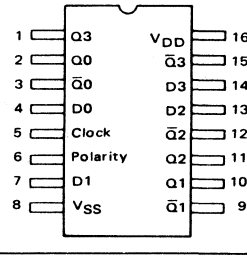
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



TRUTH TABLE

CLOCK	POLARITY	Q
0	0	Data
⌐	0	Latch
1	1	Data
¬	1	Latch

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# D Inputs "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Input Voltage C,P Inputs "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.75	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.25	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.0 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.0 μA/kHz) f + I_{DD}							
		15	I_T = (3.0 μA/kHz) f + I_{DD}							

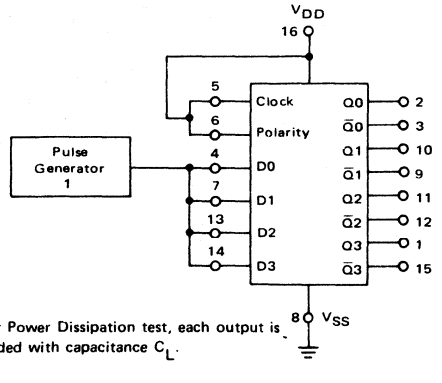
*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time, D to Q, Q	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns	t_{PHL}	5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Propagation Delay Time, Clock to Q, Q	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns	t_{PHL}	5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		25	–	60	120	
Clock Pulse Width	t_{WH}					ns
		5.0	300	150	–	
		10	100	50	–	
		15	80	40	–	
Clock Rise Time	t_{TLH}					–
		5.0	No Limit			
		10				
		15				
Hold Time	t_h					ns
		5.0	100	50	–	
		10	50	25	–	
		15	40	20	–	
Setup Time	t_{su}					ns
		5.0	50	0	–	
		10	30	0	–	
		15	25	0	–	

*The formulae given are for the typical characteristics only.

FIGURE 1 – AC AND POWER DISSIPATION TEST CIRCUIT AND TIMING DIAGRAM
(Data to Output)



For Power Dissipation test, each output is loaded with capacitance C_L.

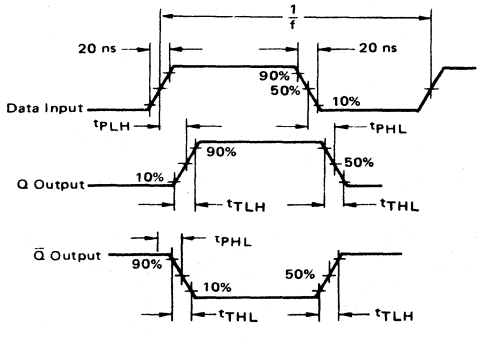
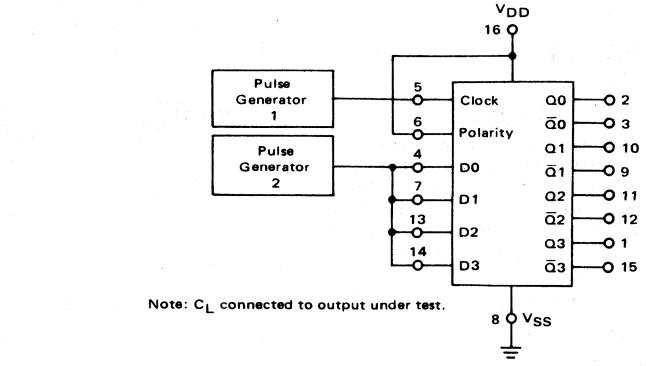
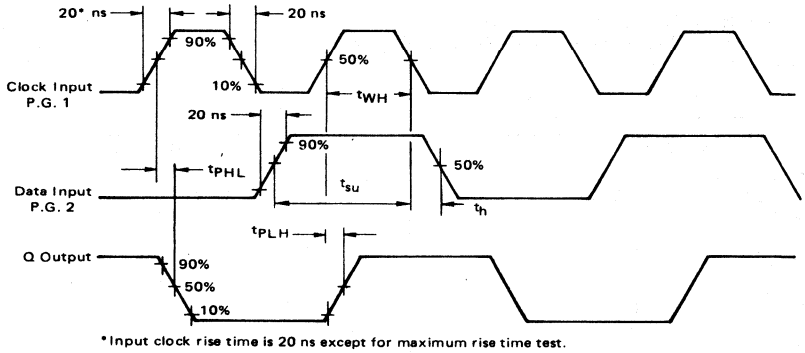


FIGURE 2 – AC TEST CIRCUIT AND TIMING DIAGRAM
(Clock to Output)



Note: C_L connected to output under test.



*Input clock rise time is 20 ns except for maximum rise time test.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

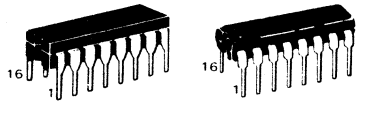
MC14043B
QUAD "NOR" R-S LATCH

MC14044B
QUAD "NAND" R-S LATCH

CMOS MSI
QUAD R-S LATCHES

The MC14043B and MC14044B quad R-S latches are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three-state buffers having a common enable input. The outputs are enabled with a logical "1" or high on the enable input; a logical "0" or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

- Quiescent Current = 4.0 nA/pkg typical @ 10 Vdc
- Double Diode Input Protection
- Three-State Outputs with Common Enable
- Outputs Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load, or Two HTL Loads Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc



L SUFFIX
CERAMIC PACKAGE
CASE 620

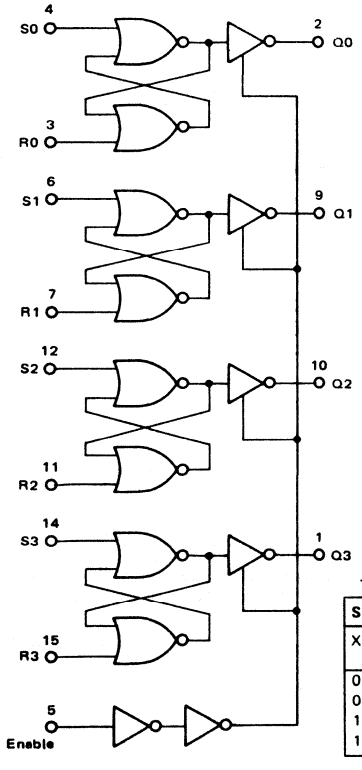
P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

3

MC14043B



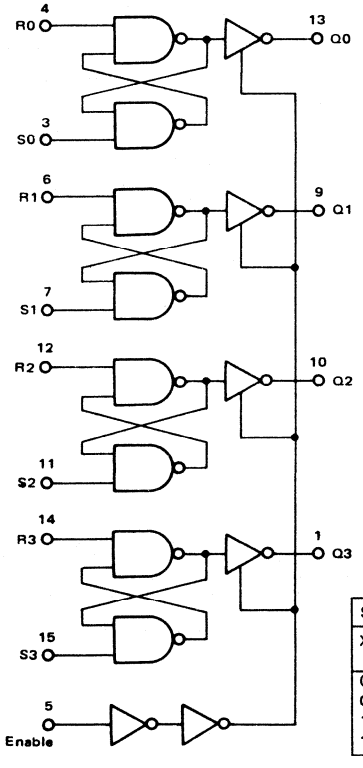
V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	No Change
0	1	1	0
1	0	1	1
1	1	1	1

X = Don't Care

MC14044B



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	No Change

X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all outputs switching)	I_T	5.0	I_T = (0.58 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.15 µA/kHz) f + I_{DD}							
		15	I_T = (1.73 µA/kHz) f + I_{DD}							
Three-State Output Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	µAdc
Three-State Output Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.0001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

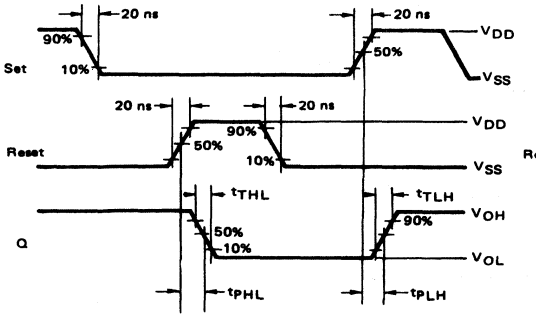
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 32.5 ns		5.0	–	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 32.5 ns		5.0	–	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.90 ns/pF) C_L + 130 ns		5.0	–	175	350	
t_{PLH} = (0.36 ns/pF) C_L + 57 ns		10	–	75	175	
t_{PLH} = (0.26 ns/pF) C_L + 47 ns		15	–	60	120	
t_{PHL} = (0.90 ns/pF) C_L + 130 ns	t_{PHL}	5.0	–	175	350	ns
t_{PHL} = (0.90 ns/pF) C_L + 57 ns		10	–	75	175	
t_{PHL} = (0.26 ns/pF) C_L + 47 ns		15	–	60	120	
Set Pulse Width	t_{WH}	5.0	200	80	–	ns
		10	100	40	–	
		15	70	30	–	
Reset Pulse Width	t_{WH}	5.0	200	80	–	ns
		10	100	40	–	
		15	70	30	–	
Three-State Enable/Disable Delay	t_{PLZ}, t_{PHZ}	5.0	–	150	300	ns
		10	–	80	160	
		15	–	55	110	

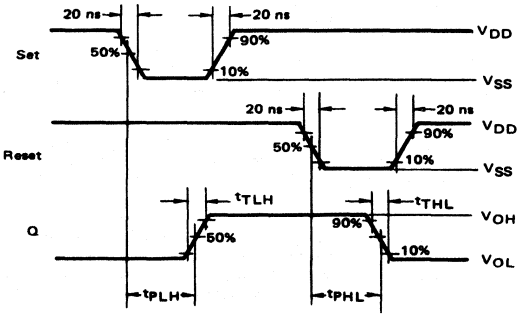
*The formulae given are for the typical characteristics only.

AC WAVEFORMS

MC14043B



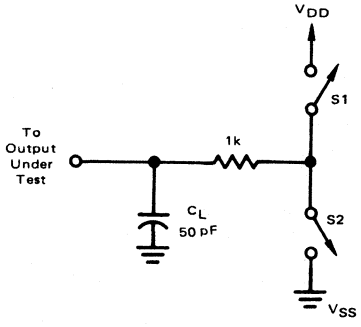
MC14044B

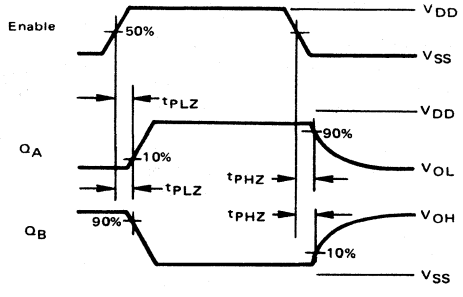


THREE-STATE ENABLE/DISABLE DELAYS

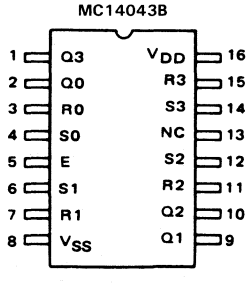
Set, Reset, and Switch Conditions for 3-State Tests.

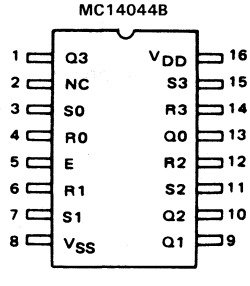
TEST	S	R	MC14043B			MC14044B		
			S1	S2	Q	S1	S2	Q
t_{PLZ}	V_{DD}	V_{SS}	Open	Closed	A	Closed	Open	B
t_{PLZ}	V_{SS}	V_{DD}	Closed	Open	B	Open	Closed	A
t_{PHZ}	V_{DD}	V_{SS}	Open	Closed	A	Closed	Open	B
t_{PHZ}	V_{SS}	V_{DD}	Closed	Open	B	Open	Closed	A





PIN ASSIGNMENT





NC = No Connection

MOTOROLA

MC14046B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PHASE-LOCKED LOOP

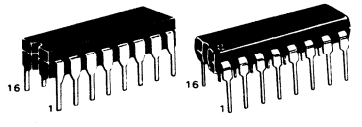
3

PHASE-LOCKED LOOP

The MC14046B phase-locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs. PCA_{in} and PCB_{in}. Input PCA_{in} can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal $PC1_{out}$, and maintains 90° phase shift at the center frequency between PCA_{in} and PCB_{in} signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals $PC2_{out}$ and PCP_{out}, and maintains a 0° phase shift between PCA_{in} and PCB_{in} signals (duty cycle is immaterial). The linear VCO produces an output signal VCO_{out} whose frequency is determined by the voltage of input VCO_{in} and the capacitor and resistors connected to pins $C1_A$, $C1_B$, R1, and R2. The source-follower output SF_{out} with an external resistor is used where the VCO_{in} signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

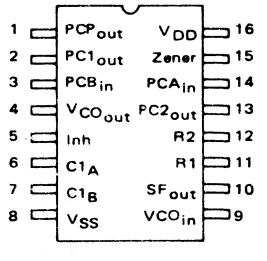
- VCO Frequency = 1.4 MHz Typical @ V_{DD} = 10 Vdc
- VCO Frequency Drift with Temperature = 0.04%/°C Typical @ V_{DD} = 10 Vdc
- VCO Linearity = 1% Typical
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Dynamic Power Dissipation — 70 μW Typical @ f_0 = 10 kHz, V_{DD} = 5.0 Vdc, R1 = 1.0 MΩ, R2 = ∞, R_{SF} = ∞
- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 Vdc
- Pin-for-Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive Or Gate and is Duty Cycle Limited
- Phase Comparator 2 switches on Rising Edges and is not Duty Cycle Limited



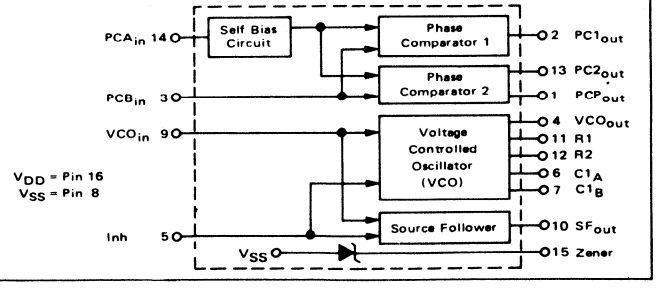
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Pins 6, 7, 10, 11, 12, and 15 if unused must be left open.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}, Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
(Inh = "1" and PCA = "1")		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
(Inh = "1" and PCA = "1")		15	–	80	–	0.015	80	–	600	
Total Supply Current †	I_T	5.0	I_T = (1.46 µA/kHz) f + I_{DD}							µAdc
(Inh = "0", f_o = 10 kHz, C_L = 50 pF,		10	I_T = (2.91 µA/kHz) f + I_{DD}							
R1 = 1 MΩ, R2 = ∞, R_{SF} = ∞, and		15	I_T = (4.37 µA/kHz) f + I_{DD}							
50% Duty Cycle)										

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†**To Calculate Total Current in General:**

$$I_T \approx 2.2 \times V_{DD}\left(\frac{VCO_{in} - 1.65}{R1} + \frac{V_{DD} - 1.35}{R2}\right)^{3/4} + 1.6 \times \left(\frac{VCO_{in} - 1.65}{R_{SF}}\right)^{3/4} + 1 \times 10^{-3}(C_L + 9)\, V_{DD}\, f +$$
$$1 \times 10^{-1}\, V_{DD}^2 \left(\frac{100 - \%\ \text{Duty Cycle of PCA}_{in}}{100}\right) + I_Q$$

where: I_T in µA, C_L in pF, VCO_{in}, V_{DD} in Vdc, f in KHz, and R1, R2, R_{SF} in MΩ, C_L on VCO_{out}.

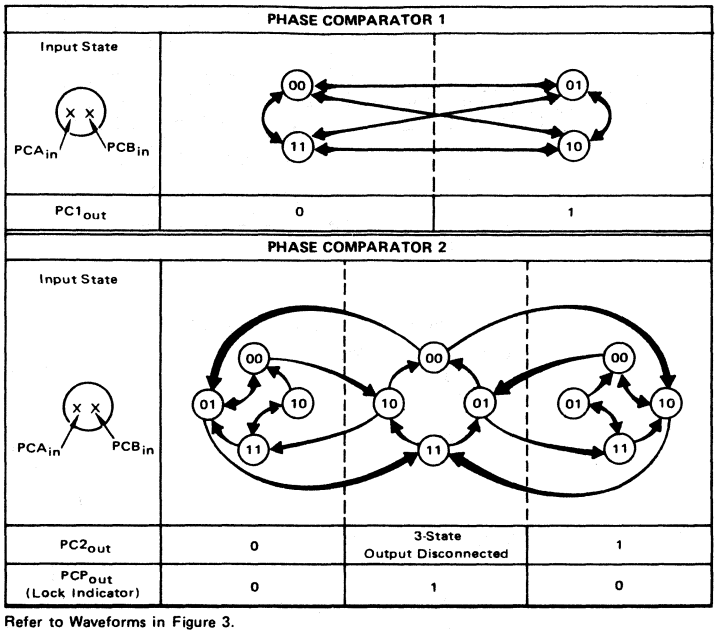
3

ELECTRICAL CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Minimum AL Device	Minimum CL/CP Device	Typical All Types	Maximum AL Device	Maximum CL/CP Device	Units
Output Rise Time	t_{TLH}							ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	–	180	350	400	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	–	90	150	200	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	–	65	110	160	
Output Fall Time	t_{THL}							ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	–	100	175	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	–	50	75	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	–	37	55	80	
PHASE COMPARATORS 1 and 2								
Input Resistance – PCA_{in}	R_{in}	5.0	1.0	1.0	2.0	–	–	MΩ
		10	0.2	0.2	0.4	–	–	
		15	0.1	0.1	0.2	–	–	
– PCB_{in}	R_{in}	15	150	15	1500	–	–	MΩ
Minimum Input Sensitivity	V_{in}	5.0	–	–	200	300	400	mV p-p
AC Coupled – PCA_{in}		10	–	–	400	600	800	
C series = 1000 pF, f = 50 kHz		15	–	–	700	1050	1400	
DC Coupled – PCA_{in}, PCB_{in}	–	5 to 15	See Noise Immunity					
VOLTAGE CONTROLLED OSCILLATOR (VCO)								
Maximum Frequency	f_{max}	5.0	0.50	0.35	0.70	–	–	MHz
(VCO_{in} = V_{DD}, C1 = 50 pF,		10	1.0	0.7	1.4	–	–	
R1 = 5 kΩ, and R2 = ∞)		15	1.4	1.0	1.9	–	–	
Temperature – Frequency Stability	–	5.0	–	–	0.12	–	–	%/°C
(R2 = ∞)		10	–	–	0.04	–	–	
		15	–	–	0.015	–	–	
Linearity (R2 = ∞)	–							%
(VCO_{in} = 2.50 V ± 0.30 V, R1 ≥ 10 kΩ)		5.0	–	–	1	–	–	
(VCO_{in} = 5.00 V ± 2.50 V, R1 ≥ 400 kΩ)		10	–	–	1	–	–	
(VCO_{in} = 7.50 V ± 5.00 V, R1 ≥ 1000 kΩ)		15	–	–	1	–	–	
Output Duty Cycle	–	5 to 15	–	–	50	–	–	%
Input Resistance – VCO_{in}	R_{in}	15	150	50	1500	–		MΩ
SOURCE-FOLLOWER								
Offset Voltage	–	5.0	–	–	1.65	2.2	2.5	Vdc
(VCO_{in} minus SF_{out}, R_{SF} > 500 kΩ)		10	–	–	1.65	2.2	2.5	
		15	–	–	1.65	2.2	2.5	
Linearity	–							%
(VCO_{in} = 2.50 V ± 0.30 V, R_{SF} > 50 kΩ)		5.0	–	–	0.1	–	–	
(VCO_{in} = 5.00 V ± 2.50 V, R_{SF} > 50 kΩ)		10	–	–	0.6	–	–	
(VCO_{in} = 7.50 V ± 5.00 V, R_{SF} > 50 kΩ)		15	–	–	0.8	–	–	
ZENER DIODE								
Zener Voltage (I_Z = 50 μA)	V_Z	–	6.7	6.3	7.0	7.3	7.7	Vdc
Dynamic Resistance (I_Z = 1 mA)	R_Z	–	–	–	100	–	–	Ω

* The formulae given are for the typical characteristics only.

FIGURE 1 – PHASE COMPARATORS STATE DIAGRAMS

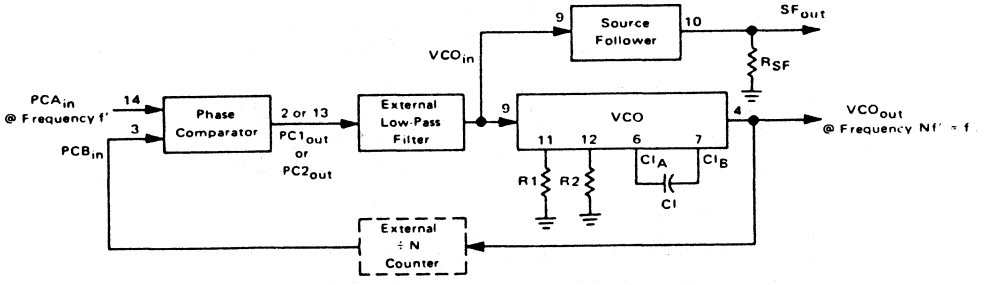


Refer to Waveforms in Figure 3.

FIGURE 2 – DESIGN INFORMATION

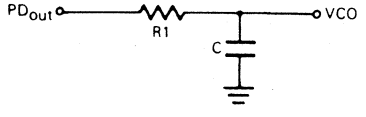
Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA$_{in}$.	VCO in PLL system adjusts to center frequency (f_0).	VCO in PLL system adjusts to minimum frequency (f_{min}).
Phase angle between PCA$_{in}$ and PCB$_{in}$.	90° at center frequency (f_0), approaching 0° and 180° at ends of lock range ($2f_L$).	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range ($2f_L$).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock. $2f_L$ = full VCO frequency range = $f_{max} - f_{min}$.	
Capture frequency range ($2f_C$).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (see Figure 3). $f_C < f_L$	$f_C = f_L$
Center frequency (f_0).	The frequency of VCO$_{out}$, when VCO$_{in}$ = 1/2 V_{DD}	
VCO output frequency (f). Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is less than ±20%.	$f_{min} = \frac{1}{R_2(C_1 + 32\,pF)}$ (V_{CO} input = V_{SS}) $f_{max} = \frac{1}{R_1(C_1 + 32\,pF)} + f_{min}$ (V_{CO} input = V_{DD}) Where: 10K < R_1 < 1M 10K < R_2 < 1M 100pF < C_1 < .01 μF	

FIGURE 3 – GENERAL PHASE-LOCKED LOOP CONNECTIONS AND WAVEFORMS



PHASE LOCKED LOOP – LOW PASS FILTER DESIGN

A)

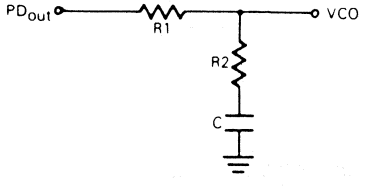


$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NR1C}}$$

$$\zeta = \frac{N\omega_N}{2K\phi\, K_{VCO}}$$

$$F(s) = \frac{1}{R1CS + 1}$$

B)



$$\omega_N = \sqrt{\frac{K_\phi K_{VCO}}{NC(R1 + R2)}}$$

$$\zeta = 0.5\omega_N \left(R2C + \frac{N}{K\phi K_{VCO}}\right)$$

$$F(s) = \frac{R2CS + 1}{S(R1C + R2C) + 1}$$

NOTE: Sometimes R1 is split into two series resistors each R1 + 2. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value for C_C should be such that the corner frequency of this network does not significantly affect ω_N.

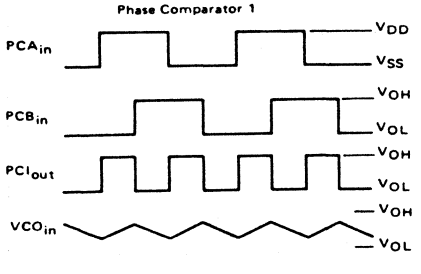
DEFINITIONS: N = Total Division Ratio in feedback loop
$K\phi = V_{DD}/\pi$ for Phase Comparator 1
$K\phi = V_{DD}/4\pi$ for Phase Comparator 2

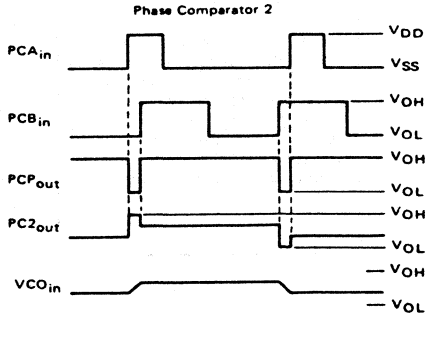
$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

for a typical design $\omega_N \cong \frac{2\pi fr}{10}$ (at phase detector input)

$\zeta \cong 0.707$

Waveforms





MOTOROLA

MC14049UB
MC14050B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX BUFFERS

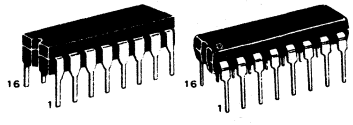
Inverting – MC14049UB
Noninverting – MC14050B

3

HEX BUFFERS

The MC14049UB hex inverter/buffer and MC14050B non-inverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{DD}. The input-signal high level (V_{IH}) can exceed the V_{DD} supply voltage for logic-level conversions. Two TTL/DTL Loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (V_{DD} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA). Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

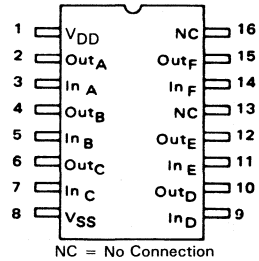
- High Source and Sink Currents
- High-to-Low Level Converter
- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Meets JEDEC UB Specifications—MC14049UB
  Meets JEDEC B Specification—MC14050B
- V_{IN} can exceed V_{DD}



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



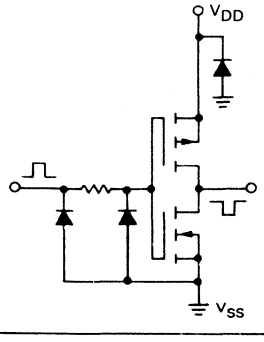
NC = No Connection

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

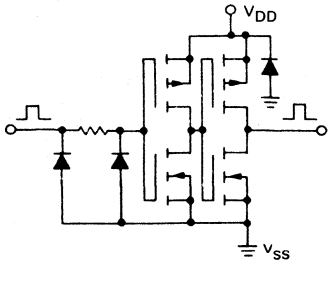
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to +30	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	45	mAdc
Operating Temperature Range AL Device	T_A	−55 to +125	°C
CL/CP Device		−40 to +85	
Storage Temperature Range	T_{stg}	−65 to +150	°C

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)

MC14049UB

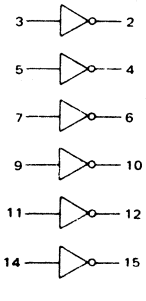


MC14050B



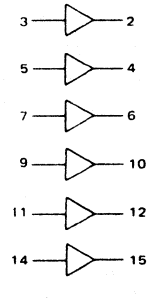
LOGIC DIAGRAMS

MC14049UB



NC = Pin 13, 16
V_{SS} = Pin 8
V_{DD} = Pin 1

MC14050B



NC = Pin 13, 16
V_{SS} = Pin 8
V_{DD} = Pin 1

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD}	T_{low}*		25°C			T_{high}*		Unit
			Vdc	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage #MC14049UB	"0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)			5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)			10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)			15	–	2.5	–	6.75	2.5	–	2.5	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 Vdc)			5.0	4.0	–	4.0	2.75	–	4.0	–	
(V_O = 1.0 Vdc)			10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 Vdc)			15	12.5	–	12.5	8.25	–	12.5	–	
Input Voltage #MC14050B	"0" Level	V_{IL}									Vdc
(V_O = 0.5 Vdc)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 1.0 Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 1.5 Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									Vdc
(V_O = 4.5 Vdc)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 9.0 Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 13.5 Vdc)			15	11	–	11	8.25	–	11	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-1.6	–	-1.25	−2.5	–	-0.9	–	
(V_{OH} = 9.5 Vdc)			10	-1.6	–	-1.3	−2.6	–	-0.9	–	
(V_{OH} = 13.5 Vdc)			15	-4.7	–	-3.75	−10	–	-2.7	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	3.75	–	3.2	6.0	–	2.1	–	mAdc
(V_{OL} = 0.5 Vdc)			10	10	–	8.0	16	–	5.6	–	
(V_{OL} = 1.5 Vdc)			15	30	–	24	40	–	16.8	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-1.5	–	−1.25	−2.5	–	-1.0	–	
(V_{OH} = 9.5 Vdc)			10	-1.5	–	−1.3	−2.6	–	-1.0	–	
(V_{OH} = 13.5 Vdc)			15	-4.5	–	−3.75	−10	–	-3.0	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	3.6	–	3.2	6.0	–	2.6	–	mAdc
(V_{OL} = 0.5 Vdc)			10	9.6	–	8.0	16	–	6.6	–	
(V_{OL} = 1.5 Vdc)			15	28	–	24	40	–	19	–	
Input Current (AL Device)		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)		I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	10	20	–	–	pF
Quiescent Current (AL Device)		I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
(Per Package)			10	–	2.0	–	0.004	2.0	–	60	
			15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)		I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
(Per Package)			10	–	8.0	–	0.004	8.0	–	60	
			15	–	16	–	0.006	16	–	120	
Total Supply Current**†		I_T	5.0	I_T = (1.8 μA/kHz)f + I_{DD}							μAdc
(Dynamic plus Quiescent, Per Package)			10	I_T = (3.5 μA/kHz)f + I_{DD}							
(C_L 50 pF on all outputs, all buffers switching)			15	I_T = (5.3 μA/kHz)f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

†To Calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3}(C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

#Noise immunity specified for worst-case input combination
B Suffix Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
UB Suffix Noise Margin for both "1" and "0" level =
0.5 Vdc min @ V_{DD} = 5.0 Vdc
1.0 Vdc min @ V_{DD} = 10 Vdc
1.0 Vdc min @ V_{DD} = 15 Vdc

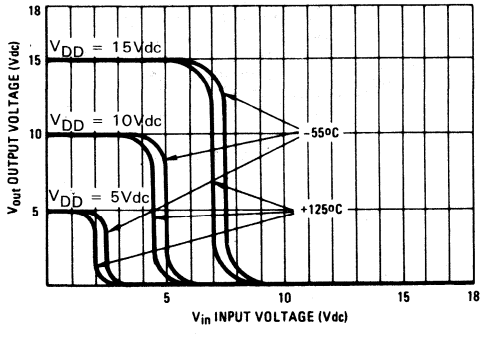
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
MC14049UB						
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.8 ns/pF) C_L + 60 ns		5.0	–	100	160	
t_{TLH} = (0.3 ns/pF) C_L + 35 ns		10	–	50	100	
t_{TLH} = (0.27 ns/pF) C_L + 26.5 ns		15	–	40	60	
Output Fall Time	t_{THL}					ns
t_{THL} = (0.3 ns/pF) C_L + 25 ns		5.0	–	40	60	
t_{THL} = (0.12 ns/pF) C_L + 14 ns		10	–	20	40	
t_{THL} = (0.1 ns/pF) C_L + 10 ns		15	–	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.38 ns/pF) C_L + 61 ns		5.0	–	80	120	
t_{PLH} = (0.20 ns/pF) C_L + 30 ns		10	–	40	65	
t_{PLH} = (0.11 ns/pF) C_L + 24.5 ns		15	–	30	50	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.38 ns/pF) C_L + 11 ns		5.0	–	30	60	
t_{PHL} = (0.12 ns/pF) C_L + 9 ns		10	–	15	30	
t_{PHL} = (0.11 ns/pF) C_L + 4.5 ns		15	–	10	20	
MC14050B						
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.7 ns/pF) C_L + 65 ns		5.0	–	100	160	
t_{TLH} = (0.25 ns/pF) C_L + 37.5 ns		10	–	50	80	
t_{TLH} = (0.2 ns/pF) C_L + 30 ns		15	–	40	60	
Output Fall Time	t_{THL}					ns
t_{THL} = (0.2 ns/pF) C_L + 30 ns		5.0	–	40	60	
t_{THL} = (0.06 ns/pF) C_L +17 ns		10	–	20	40	
t_{THL} = (0.04 ns/pF) C_L + 13 ns		15	–	15	30	
Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.33 ns/pF) C_L + 63.5 ns		5.0	–	80	140	
t_{PLH} = (0.19 ns/pF) C_L + 30.5 ns		10	–	40	80	
t_{PLH} = (0.06 ns/pF) C_L + 27 ns		15	–	30	60	
Propagation Delay Time	t_{PHL}					ns
t_{PHL} = (0.2 ns/pF) C_L + 30 ns		5.0	–	40	80	
t_{PHL} = (0.1 ns/pF) C_L + 15 ns		10	–	20	40	
t_{PHL} = (0.05 ns/pF) C_L + 12.5 ns		15	–	15	30	

*The formulae given are for the typical characteristics only.

FIGURE 1 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

MC14049UB



MC14050B

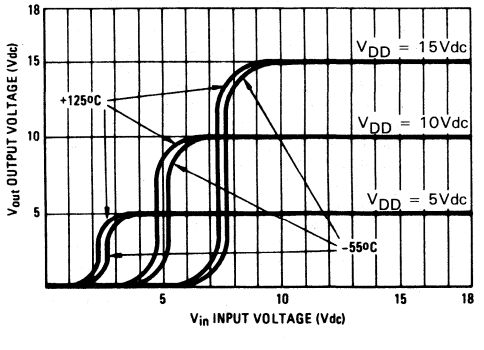


FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

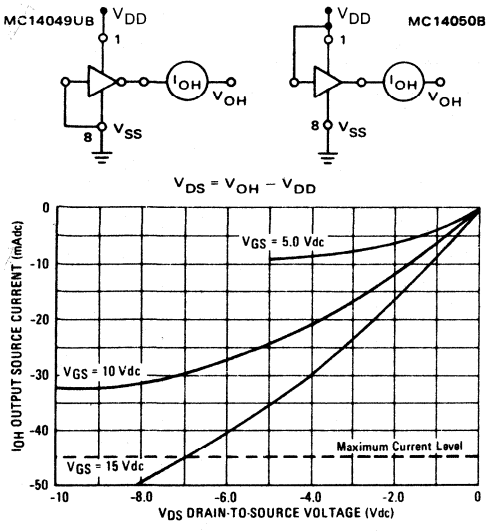


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS

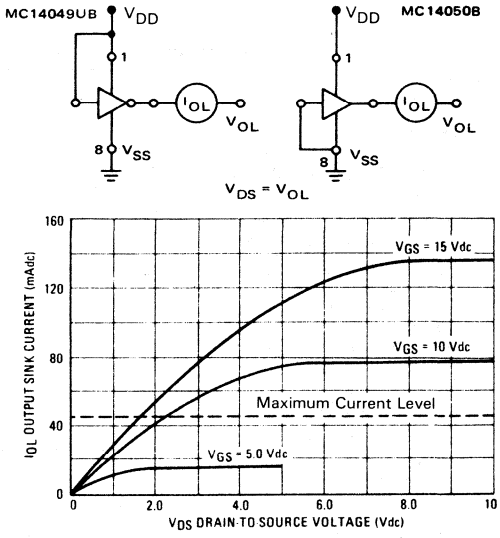


FIGURE 4 – AMBIENT TEMPERATURE POWER DERATING

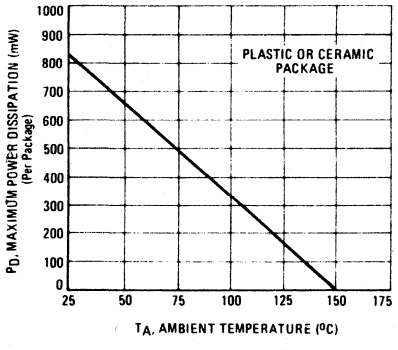
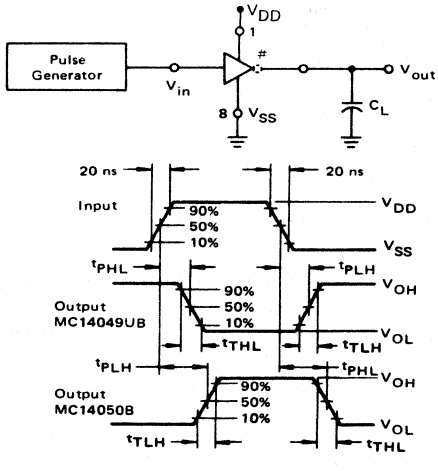


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



#Invert on MC14049UB only

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{out} be constrained to the range $V_{SS} \leq V_{out} \leq V_{DD}$ and that V_{in} be constrained to the range $V_{SS} \leq V_{in} \leq 30$ volts.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14051B
MC14052B
MC14053B

ANALOG MULTIPLEXERS/DEMULTIPLEXERS

The MC14051B, MC14052B, and MC14053B, analog multiplexers are digitally controlled analog switches. The MC14051B effectively implements an 8PST electronic switch, the MC14052B a 4PDT or 2P4T, and the MC14053B a DP3T or 3P2T. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

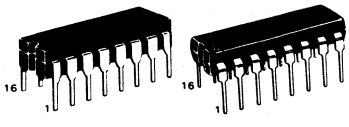
- High On/Off Output Voltage Ratio – 65 dB typical
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches – 80 dB typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range (V_{DD}-V_{EE}) = 3 to 18 V
  Note: V_{EE} must be $\leq V_{SS}$
- Transmits Frequencies Up to 65 MHz
- Linearized Transfer Characteristics, ΔR_{ON} <60 Ω for $V_{in} = V_{DD}$ to V_{EE} @ 15 Vdc
- Low Noise – 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/ DEMULTIPLEXERS

3



CASE 620
L SUFFIX
CERAMIC PACKAGE

CASE 648
P SUFFIX
PLASTIC PACKAGE

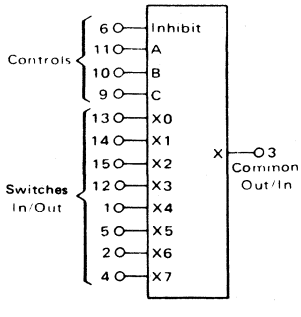
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS

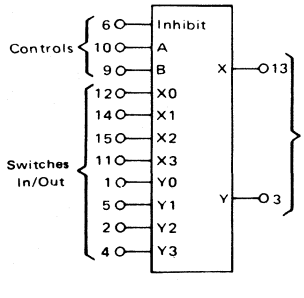
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{EE}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
Through Current	I	25	mAdc
Operating Temperature Range — AL Device	T_A	-55 to +125	°C
CL/CP Device		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	°C

MC14051B
8-Channel Analog Multiplexer/Demultiplexer



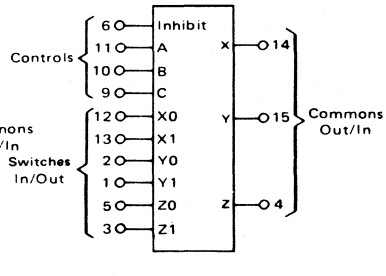
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

MC14052B
Dual 4-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

MC14053B
Triple 2-Channel Analog Multiplexer/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

Note: Control Inputs referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be $\leq V_{SS}$.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}-V_{EE} Vdc	T_{low}*' Min	T_{low}*' Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.005	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or V_{SS}		10	–	0.05	–	0	0.05	–	0.05	
V_{SS} = V_{EE}		15	–	0.05	–	0	0.05		0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage (Control) # "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.25	–	11.0	8.25	–	11.0	–	
Input Current (AL Device) (Control Inhibit)	i_{in}	15	–	±0.1	–	± 0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device) (Control, Inhibit)	I_{in}	15	–	±0.3	–	± 0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}									pF
Control, Inhibit		–	–	–	–	5.0	7.5	–	–	
Switch Inputs (Inhibit = 1)		–	–	–	–	10	21.0	–	–	
Output Capacitance MC14051B	C_{out}	10	–	–	–	96	–	–	–	pf
MC14052B		10	–	–	–	48	–	–	–	
MC14053B		10	–	–	–	24	–	–	–	
Feedthrough Capacitance MC14051B	C_{in-out}	10	–	–	–	0.18	–	–	–	pf
MC14052B		10	–	–	–	0.12	–	–	–	
MC14053B		10	–	–	–	0.10	–	–	–	
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package)	I_T	5.0	I_T = (0.07 µA/kHz) f + I_Q							µADC
		10	I_T = (0.20 µA/kHz) f + I_Q							
		15	I_T = (0.36 µA/kHz) f + I_Q							
ON Resistance (AL Device)	R_{ON}	5.0	–	800	–	250	1050	–	1300	Ω
		10	–	400	–	120	500	–	550	
		15	–	220	–	80	280	–	320	
ON Resistance (CL/CP Device)	R_{ON}	5.0	–	880	–	250	1050	–	1200	Ω
		10	–	450	–	120	500	–	520	
		15	–	250	–	80	280	–	300	
Δ ON Resistance Between Any Two Channels	Δ R_{ON}	5.0	–	–	–	25	–	–	–	Ω
		10	–	–	–	10	–	–	–	
		15	–	–	–	5.0	–	–	–	
OFF Channel Leakage Current	–									nAdc
Any Channel (AL Device) All Channels OFF:		15	–	±100	–	±0.01	±100	–	±1000	
MC14051B		15	–	±100	–	±0.08	±100	–	±1000	
MC14052B		15	–	±100	–	±0.04	±100	–	±1000	
MC14053B		15	–	±100	–	±0.02	±100	–	±1000	
OFF Channel Leakage Current	–									nAdc
Any Channel (CL/CP Device)		15	–	±300	–	±0.01	±300	–	±1000	
All Channels OFF: MC14051B		15	–	±300	–	±0.08	±300	–	±1000	
MC14052B		15	–	±300	–	±0.04	±300	–	±1000	
MC14053B		15	–	±300	–	±0.02	±300	–	±1000	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for Al Device, +85°C for CL/CP Device.

Noise immunity is defined as the control input voltage coincident with the specified change, ΔV_{out}, at an output in the OFF State.

** The formulas given are for the typical characteristics only at 25°C.

† Total Supply Current, I_T, is the current drawn at device terminals V_{DD} and V_{SS} for total current through the device. The channel component, $(V_{in}-V_{out})/R_{ON}$, should not be included.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

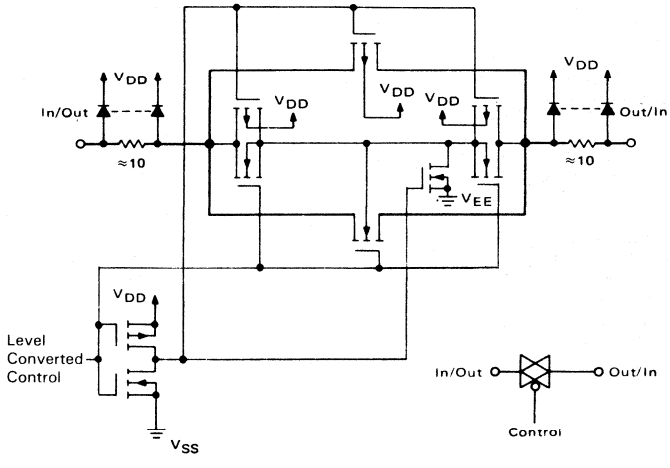
Characteristic	Symbol	V_{DD}-V_{EE} Vdc	Typ All Types	Max	Unit
Propagation Delay Times	t_{PLH}, t_{PHL}				ns
Switch Input to Switch Output (R_L = 10 kΩ)					
MC14051					
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns		5.0	35	90	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 11 ns		10	15	40	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns		15	12	30	
MC14052					
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 21.5 ns		5.0	30	75	ns
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 8.0 ns		10	12	30	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 7.0 ns		15	10	25	
MC14053					
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 16.5 ns		5.0	25	65	ns
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 4.0 ns		10	8.0	20	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 3.0 ns		15	6.0	15	
Inhibit to Output (R_L = 10 kΩ):					
Output "1" or "0" to High Impedance, or	t_{PHZ}, t_{PLZ},				ns
High Impedance to "1" or "0" Level	t_{PZH}, t_{PZL}				
MC14051B		5.0	350	700	
		10	170	340	
		15	140	280	
MC14052B		5.0	300	600	ns
		10	155	310	
		15	125	250	
MC14053B		5.0	275	550	ns
		10	140	280	
		15	110	220	
Control Input to Output (R_L = 10 kΩ)	t_{PLH}, t_{PHL}				ns
MC14051B		5.0	360	720	
		10	160	320	
		15	120	240	
MC14052B		5.0	325	650	ns
		10	130	260	
		15	90	180	
MC14053B		5.0	300	600	ns
		10	120	240	
		15	80	160	
Sine Wave Distortion (R_L = 1 kΩ, f = 1 kHz)	–	10	0.04	–	%
Bandwidth (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}-V_{EE}) p-p, 20 Log $\frac{V_{out}}{V_{in}}$ = −3 dB)	BW				MHz
MC14051B		10	20	–	
MC14052B		10	30	–	
MC14053B		10	55	–	
Feedthrough Attenuation, Input to Output (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}-V_{EE}) p-p, 20 Log $\frac{V_{out}}{V_{in}}$ = −50 dB)	–				MHz
MC14051B		10	4.5	–	
MC14052B		10	30	–	
MC14053B		10	55	–	
Channel Separation (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}-V_{EE}) p-p, 20 Log $\frac{V_{out(B)}}{V_{in(A)}}$ = −50 dB)	–	10	3.0	–	MHz
Feedthrough Control, Input to Output (R_1 = 1 kΩ, R_L = 10 kΩ Control/Inhibit t_{TLH} = t_{THL} = 20 ns)	–	10	30	–	mV
Maximum Control Frequency (R_L = 1 kΩ, V_{out} = 1/2 V_{in})	–	10	2	–	MHz

* The formulas given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC



TRUTH TABLE

Control Inputs				ON Switches					
	Select								
Inhibit	C*	B	A	MC14051B	MC14052B		MC14053B		
0	0	0	0	X0	Y0	X0	Z0	Y0	X0
0	0	0	1	X1	Y1	X1	Z0	Y0	X1
0	0	1	0	X2	Y2	X2	Z0	Y1	X0
0	0	1	1	X3	Y3	X3	Z0	Y1	X1
0	1	0	0	X4			Z1	Y0	X0
0	1	0	1	X5			Z1	Y0	X1
0	1	1	0	X6			Z1	Y1	X0
0	1	1	1	X7			Z1	Y1	X1
1	x	x	x	None	None		None		

*Not applicable for MC14052
x = Don't Care

FIGURE 2 – MC14051B FUNCTIONAL DIAGRAM

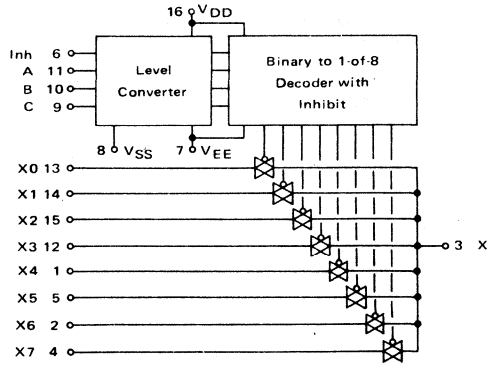


FIGURE 3 – MC14052B FUNCTIONAL DIAGRAM

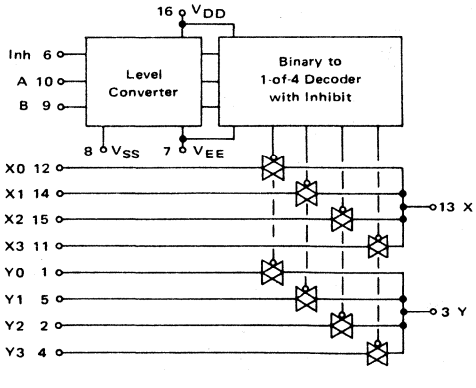
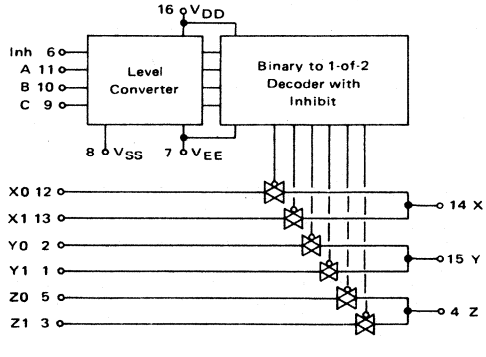


FIGURE 4 – MC14053B FUNCTIONAL DIAGRAM



TEST CIRCUITS

FIGURE 5 – INPUT VOLTAGE

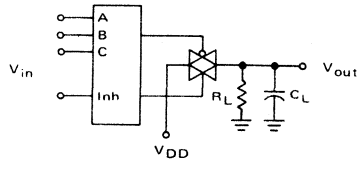


FIGURE 6 – PROPAGATION DELAY TIMES, CONTROL AND INHIBIT TO OUTPUT

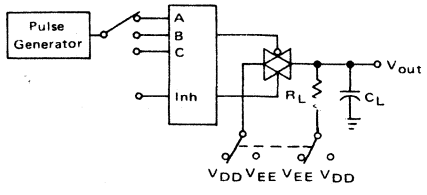


FIGURE 7 – BANDWIDTH AND FEEDTHROUGH ATTENUATION

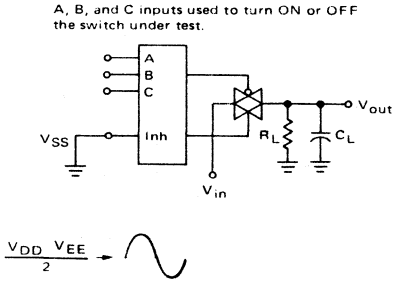


FIGURE 8 – CROSSTALK BETWEEN ANY TWO SWITCHES

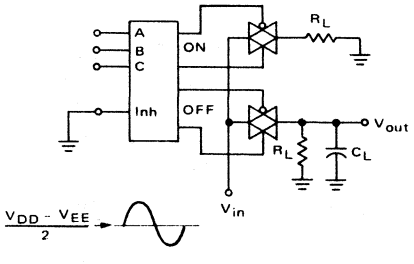


FIGURE 9 – FEEDTHROUGH, CONTROL TO SIGNAL OUTPUT

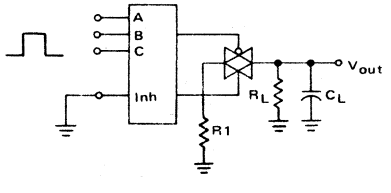


FIGURE 10 – MAXIMUM CONTROL FREQUENCY

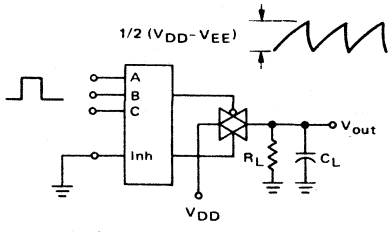
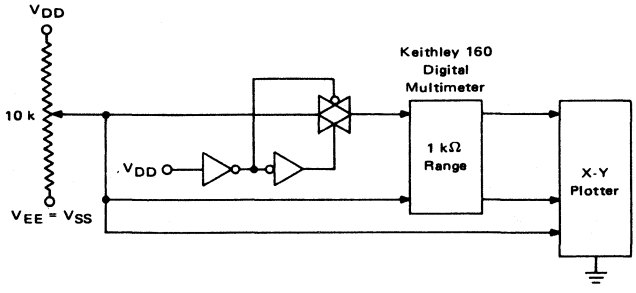


FIGURE 11 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

3

FIGURE 12 – V_{DD} = 7.5 V, V_{EE} = -7.5 V

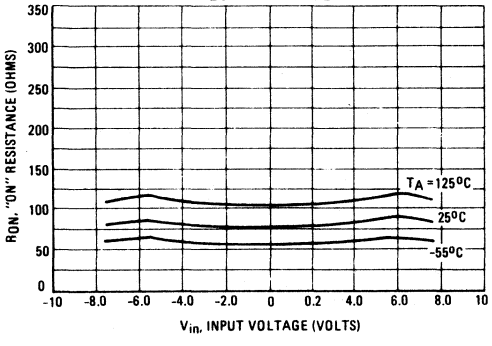


FIGURE 13 – V_{DD} = 5.0 V, V_{EE} = -5.0 V

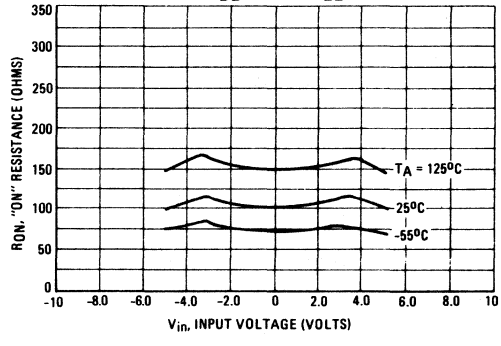


FIGURE 14 – V_{DD} = 2.5 V, V_{EE} = -2.5 V

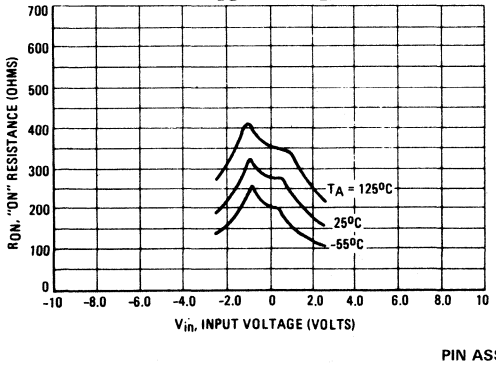
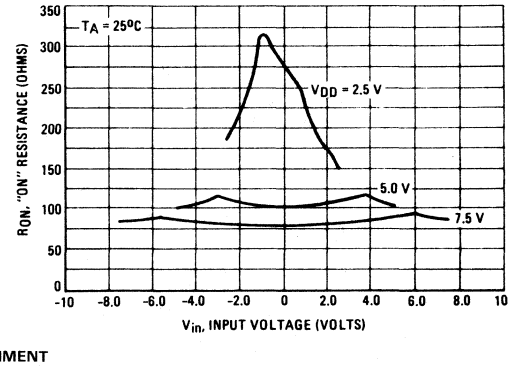
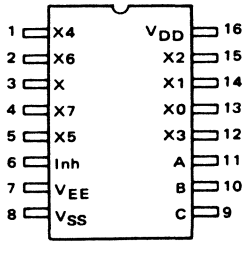


FIGURE 15 – COMPARISON AT 25°C, V_{DD} = -V_{EE}

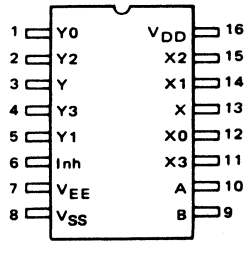


PIN ASSIGNMENT

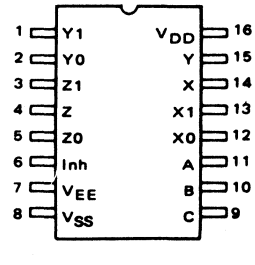
MC14051B



MC14052B



MC14053B



MOTOROLA

MC14060B

Advance Information

CMOS MSI

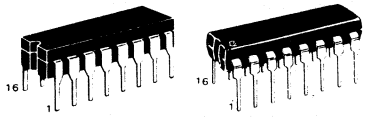
(LOW POWER COMPLEMENTARY MOS)

14-BIT BINARY COUNTER AND OSCILLATOR

14-BIT BINARY COUNTER AND OSCILLATOR

The MC14060B is a 14-stage binary ripple counter with an on-chip oscillator buffer. The oscillator configuration allows design of either RC or crystal oscillator circuits. Also included on the chip is a reset function which places all outputs into the zero state and disables the oscillator. A negative transition on $Clock_{in}$ will advance the counter to the next state. Schmitt trigger action on the input line permits very slow input rise and fall times. Applications include time delay circuits, counter controls, and frequency dividing circuits.

- Fully Static Operation
- Quiescent Current = 5.0 nA/Package Typical @ 5 V
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Low Input Capacitance = 5.0 pF Typical
- Buffered Outputs Available from Stages 4 Through 10 and 12 Through 14
- Common Reset Line
- 17 MHz Typical Counting Rate @ V_{DD} = 15 V
- Pin-for-Pin Replacement for CD4060B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

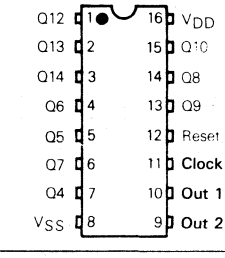
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

TRUTH TABLE

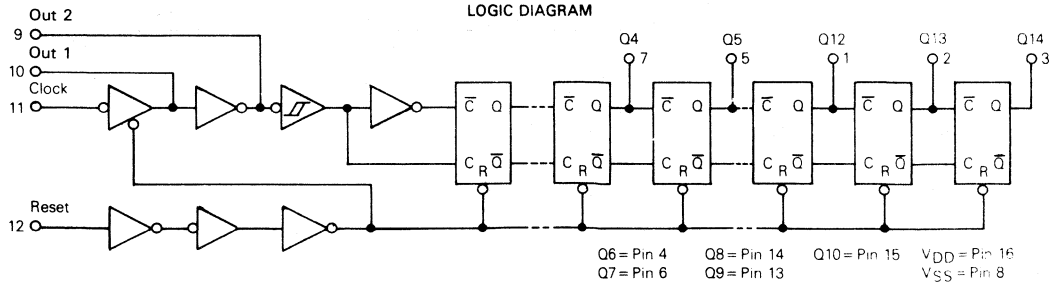
$Clock_{in}$	RESET	Output State
⌐¯	L	No Change
¯⌐	L	Advance to next state
X	H	All Outputs are low

X = Don't Care

PIN ASSIGNMENT



LOGIC DIAGRAM



This is advance information and specifications are subject to change without notice.

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ADI-822

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range − AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} V	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	V
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	V
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage # "0" Level (V_O = 4.5 or 0.5 V)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level (V_O = 0.5 or 4.5 V)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
(V_O = 1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)†										
(V_{OH} = 2.5 V) Source	I_{OH}	5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	mA
(V_{OH} = 4.6 V)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 V)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 V)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mA
(V_{OL} = 0.5 V)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 V)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)†										
(V_{OH} = 2.5 V) Source	I_{OH}	5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	mA
(V_{OH} = 4.6 V)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 V)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 V)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mA
(V_{OL} = 0.5 V)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 V)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μA
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μA
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	

* T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, 85°C for CL/CP Device.

\# Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
2.0 V min @ V_{DD} = 10 V
2.5 V min @ V_{DD} = 15 V

† Data not applicable to pins 9 and 10.

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time (Counter Outputs)	t_{TLH}	5.0 10 15	– – –	40 25 20	200 100 80	ns
Output Fall Time (Counter Outputs)	t_{THL}	5.0 10 15	– – –	50 30 20	200 100 80	ns
Propagation Delay Time $Clock_{in}$ to Q4	t_{PLH} t_{PHL}	5.0 10 15	– – –	415 175 125	740 300 200	ns
$Clock_{in}$ to Q14		5.0 10 15	– – –	1.5 0.7 0.4	2.7 1.3 1.0	μs
Clock Pulse Width	t_{WH}	5.0 10 15	100 40 30	65 30 20	– – –	ns
Clock Pulse Frequency	f_ϕ	5.0 10 15	– – –	5 14 17	3.5 8 12	MHz
Clock Rise and Fall Time	t_{TLH} t_{THL}	5.0 10 15	No Limit			–
Reset Pulse Width	t_W	5.0 10 15	120 60 40	40 15 10	– – –	ns
Propagation Delay Time Reset to Qn	t_{PHL}	5.0 10 15	– – –	170 80 60	360 160 100	ns

FIGURE 1 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

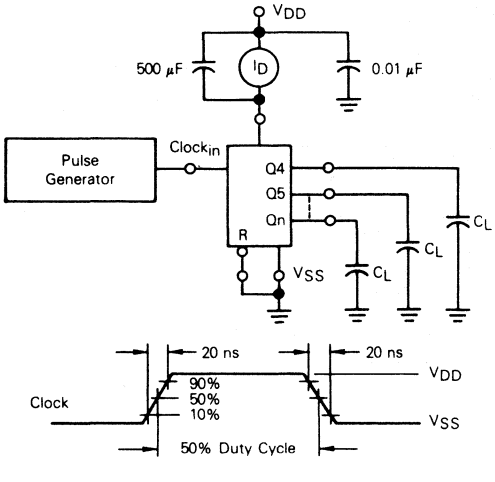


FIGURE 2 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

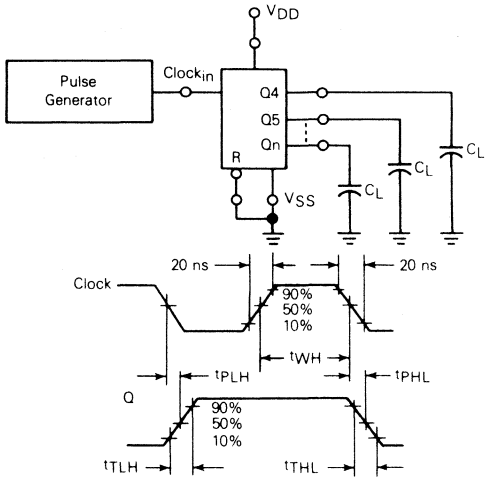
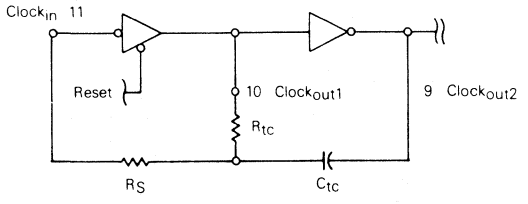


FIGURE 3 – OSCILLATOR CIRCUIT USING RC CONFIGURATION



$$f \approx \frac{1}{2.3\,R_{tc}C_{tc}}$$

if 1kHz ≤ f ≤ 100 kHz
and $R_S \approx 2\,R_{tc}$
(f in Hz, R in ohms, C in farads)

TYPICAL RC OSCILLATOR CHARACTERISTICS

FIGURE 4 – RC OSCILLATOR STABILITY

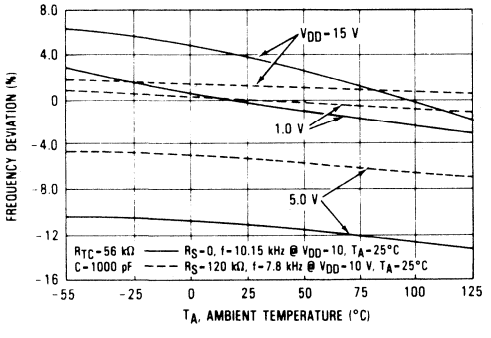


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C

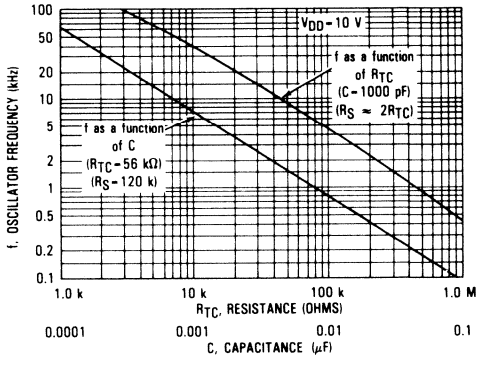


FIGURE 6 – TYPICAL CRYSTAL OSCILLATOR CIRCUIT

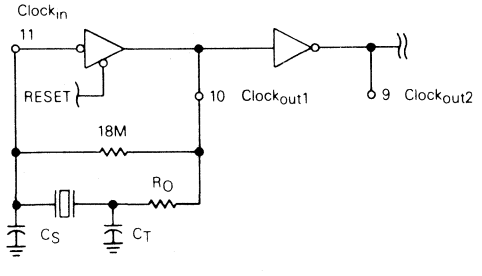


FIGURE 7 – TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

Characteristic	500 kHz Circuit	32 kHz Circuit	Unit
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Equivalent Resistance, R_S	1.0	6.2	kΩ
External Resistor/Capacitor Values			
R_O	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Changes as a Function of V_{DD} (T_A = 25°C)			
V_{DD} Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V_{DD} Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature (V_{DD} = 10 V)			
T_A Change from −55°C to +25°C Complete Oscillator*	+100	+120	ppm
T_A Change from +25°C to +125°C Complete Oscillator*	−160	−560	ppm

*Complete oscillator includes crystal, capacitors, and resistors.

MOTOROLA

MC14066B

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

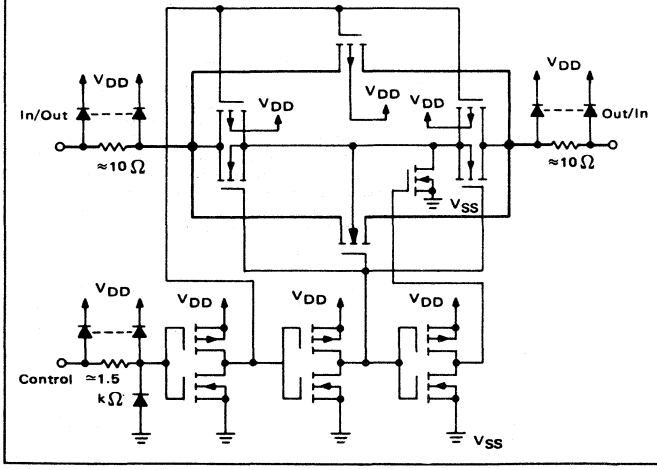
The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- High On/Off Output Voltage Ratio — 65 dB typical
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Low Crosstalk Between Switches —50 dB typical @ 8 MHz
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Transmits Frequencies Up to 65 MHz @ 10 Vdc
- Linearized Transfer Characteristics, $\Delta R_{ON} < 60\ \Omega$ for $V_{in} = V_{DD}$ to V_{SS} (at 15V)
- Low Noise — 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4016, CD4066, MC14016

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
Through Current	I	25	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

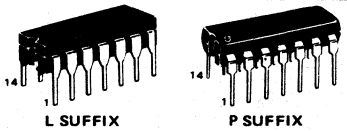
CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)



CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH
QUAD MULTIPLEXER

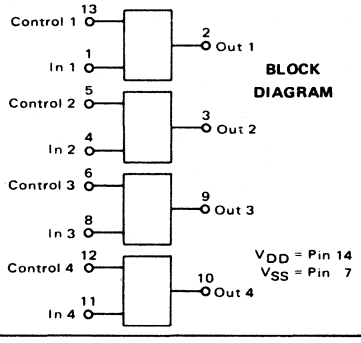


L SUFFIX
CERAMIC PACKAGE
CASE 632

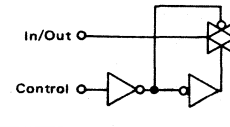
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range



LOGIC DIAGRAM AND TRUTH TABLE
(1/4 OF DEVICE SHOWN)



Control	Switch
0	OFF
1	ON

Logic Diagram Restrictions
$V_{SS} \leq V_{in} \leq V_{DD}$
$V_{SS} \leq V_{out} \leq V_{DD}$

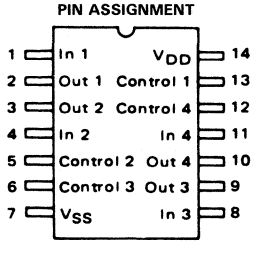
$V_{control}$	V_{in} to V_{out} Resistance
V_{SS}	$>10^9$ Ohms typ
V_{DD}	3×10^2 Ohms typ

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Voltage (Control) "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.75	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.25	–	11.25	8.25	–	11.25	–	
Input Current (AL Device) Control	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device) Control	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}									pF
Control Input			–	–	–	5.0	7.5	–	–	
Switch Inputs		10	–	–	–	8.0	15	–	–	
Output Capacitance	C_{out}	10	–	–	–	13.0	–	–	–	pF
Feedthrough Capacitance	C_{in-out}	10	–	–	–	0.5	–	–	–	pF
Quiescent Current (AL Device)	I_O	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_Q	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
ON Resistance (AL Device)	R_{ON}	5.0	–	800	–	250	1050	–	1200	Ω
		10	–	400	–	120	500	–	520	
		15	–	220	–	80	280	–	300	
ON Resistance (CL/CP Device)	R_{ON}	5.0	–	880	–	250	1050	–	1300	Ω
		10	–	450	–	120	500	–	550	
		15	–	250	–	80	280	–	320	
ΔON Resistance Between Any Two of Four Switches	ΔR_{ON}	5.0	–	–	–	25	–	–	–	Ω
		10	–	–	–	10	–	–	–	
		15	–	–	–	5.0	–	–	–	
Input/Output Leakage Current Switch OFF (AL Device)	–	15	–	±100	–	±0.01	±100	–	±1000	nAdc
Input/Output Leakage Current Switch OFF (CL/CP Device)	–	15	–	±300	–	±0.01	±300	–	±1000	nAdc

*T_{low} = 55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Propagation Delay Times V_{SS} = 0 Vdc						
Input to Output (R_L = 10 kΩ)	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 15.5 ns		5.0	–	20	40	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 6.0 ns		10	–	10	20	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 4.0 ns		15	–	7.0	15	
Control to Output (R_L = 1 kΩ)						
Output "1" to High Impedance	t_{PHZ}	5.0	–	40	80	ns
		10	–	35	70	
		15	–	30	60	
Output "0" to High Impedance	t_{PLZ}	5.0	–	40	80	ns
		10	–	35	70	
		15	–	30	60	
High Impedance to Output "1"	t_{PZH}	5.0	–	60	120	ns
		10	–	20	40	
		15	–	15	30	
High Impedance to Output "0"	t_{PZL}	5.0	–	60	120	ns
		10	–	20	40	
		15	–	15	30	
Sine Wave Distortion V_{SS} = -5 Vdc (V_{in} = 1.77 Vdc, RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	–	5.0	–	0.1	–	%
Frequency Response (Switch ON) V_{SS} = -5 Vdc (R_L = 1 kΩ, $20 \log_{10} \frac{V_{out}}{V_{in}}$ = -3 dB)	–	5.0	–	65	–	MHz
Feedthrough Attenuation (Switch OFF) V_{SS} = -5 Vdc (R_L = 1 kΩ, $20 \log_{10} \frac{V_{out}}{V_{in}}$ = -50 dB)	–	5.0	–	1.0	–	MHz
Crosstalk Between Any Two Switches V_{SS} = -5 Vdc (R_L = 1 kΩ, $20 \log_{10} \frac{V_{out(B)}}{V_{in(A)}}$ = -50 dB, (Switch A ON, Switch B OFF)	–	5.0	–	8.0	–	MHz
Crosstalk, Control Input to Signal Output V_{SS} = -5 Vdc	–	5.0	–	300	–	p-p mV
Maximum Control Input Frequency V_{SS} = 0 Vdc	–	5.0	–	6.0	–	MHz
($20 \log_{10} \frac{V_{out}}{V_{in}}$ = -6 dB)		10	–	8.0	–	
		15	–	8.5	–	

*The formulas given are for the typical characteristics only.

TEST CIRCUITS

FIGURE 1 – INPUT VOLTAGE

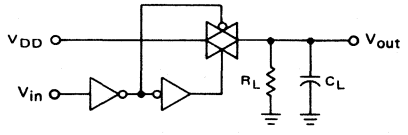


FIGURE 2 – PROPAGATION DELAY TIME, CONTROL TO OUTPUT

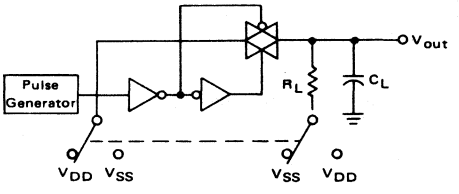


FIGURE 3 – BANDWIDTH AND FEEDTHROUGH ATTENUATION

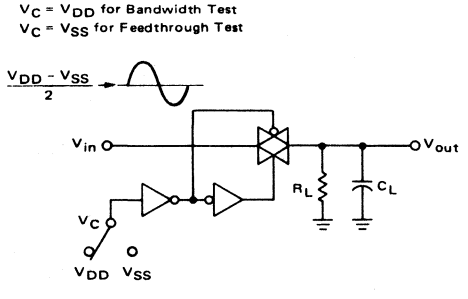


FIGURE 4 – CROSSTALK BETWEEN ANY TWO SWITCHES

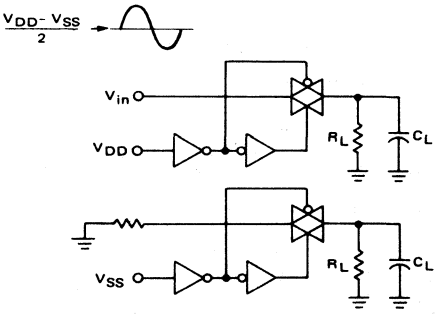


FIGURE 5 – CROSSTALK, CONTROL TO OUTPUT

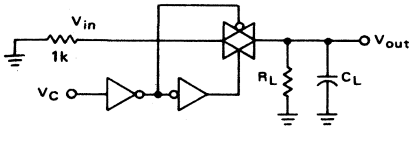


FIGURE 6 – MAXIMUM CONTROL FREQUENCY

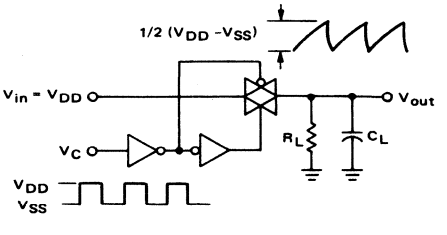
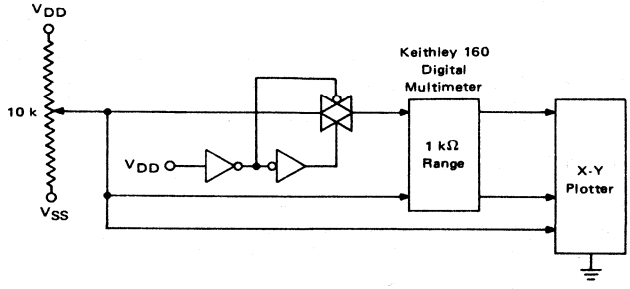


FIGURE 7 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 8 – V_{DD} = 7.5 V, V_{SS} = -7.5 V

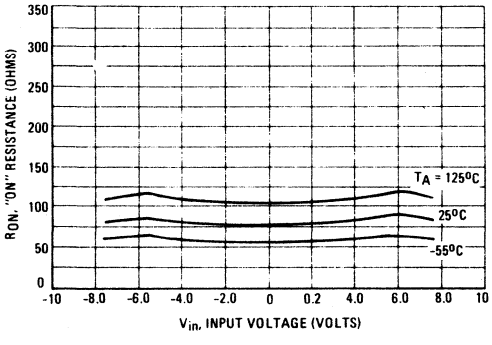


FIGURE 9 – V_{DD} = 5.0 V, V_{SS} = -5.0 V

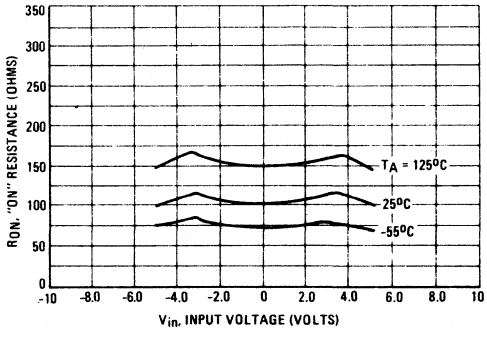


FIGURE 10 – V_{DD} = 2.5 V, V_{SS} = -2.5 V

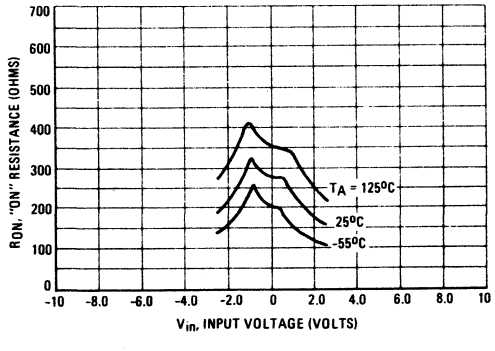
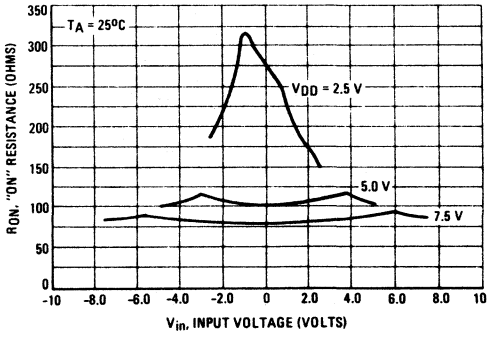


FIGURE 11 – COMPARISON AT 25°C, V_{DD} = -V_{SS}



MOTOROLA

MC14067B
MC14097B

Advance Information

CMOS
(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/
DEMULTIPLEXERS

3

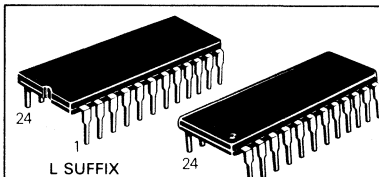
ANALOG MULTIPLEXERS/DEMULTIPLEXERS

The MC14067 and MC14097 multiplexers/demultiplexers are digitally controlled transmission gates featuring low ON resistance and very low leakage current. These devices can be used in either digital or analog applications.

The MC14067 is a 16-channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C and D. These control inputs select 1-of-16 channels by turning ON the appropriate transmission gate (see MC14067 truth table).

The MC14097 is a differential 8-channel multiplexer/demultiplexer with an inhibit and three binary control inputs A, B and C. These control inputs select 1 of 8 pairs of channels by turning ON the appropriate transmission gates (see MC14097 truth table).

- Low ON Resistance: 80 Ω @ $V_{DD} - V_{SS} = 15$ V
- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Transmits Frequencies Up to 65 MHz @10 V
- Low Noise
- Pin for Pin Replacement for CD4067B and CD4097B



L SUFFIX
CERAMIC PACKAGE
CASE 623

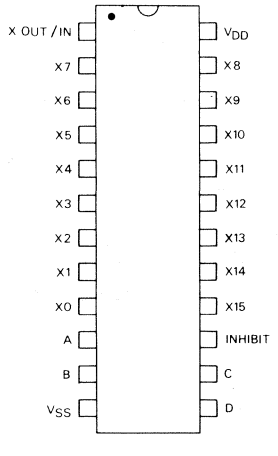
P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

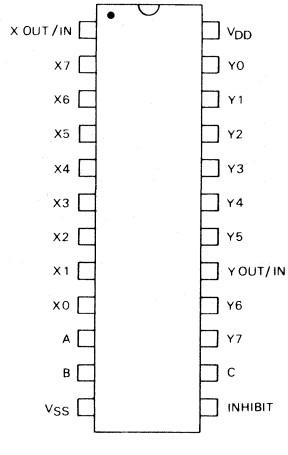
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENTS

MC14067B



MC14097B



ADI 919

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	V
Through Current	I	25	mA
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

MC14067 TRUTH TABLE

Control Inputs					Selected
A	B	C	D	Inh	Channel
X	X	X	X	1	None
0	0	0	0	0	X0
1	0	0	0	0	X1
0	1	0	0	0	X2
1	1	0	0	0	X3
0	0	1	0	0	X4
1	0	1	0	0	X5
0	1	1	0	0	X6
1	1	1	0	0	X7
0	0	0	1	0	X8
1	0	0	1	0	X9
0	1	0	1	0	X0
1	1	0	1	0	X1
0	0	1	1	0	X2
1	0	1	1	0	X3
0	1	1	1	0	X4
1	1	1	1	0	X5

MC14097 TRUTH TABLE

Control Inputs				Selected
A	B	C	Inh	Channels
X	X	X	1	None
0	0	0	0	X0 Y0
1	0	0	0	X1 Y1
0	1	0	0	X2 Y2
1	1	0	0	X3 Y3
0	0	1	0	X4 Y4
1	0	1	0	X5 Y5
0	1	1	0	X6 Y6
1	1	1	0	X7 Y7

X = Don't Care

FIGURE 1 — MC14067 FUNCTIONAL DIAGRAM

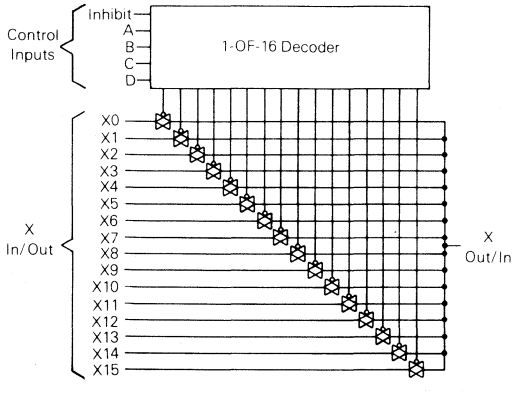
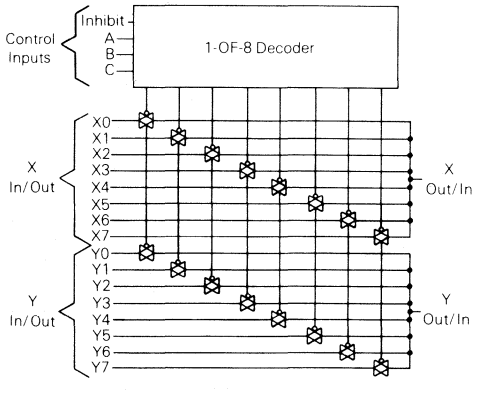


FIGURE 2 — MC14097 FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} V	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Channel Inputs (V_{in}) and Outputs (V_{out})										
Output Voltage "0" Level V_{in} = 0 V	V_{OL}	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	V
"1" Level V_{in} = V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	V
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0 10 15	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	μA
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0 10 15	– – –	20 40 80	– – –	0.005 0.010 0.015	20 40 80	– – –	150 300 600	μA
Total Supply Current**† (Dynamic plus Quiescent, Per Package)	I_T	5.0 10 15	I_T = (0.07 μA/kHz) f + I_{DD} I_T = (0.20 μA/kHz) f + I_{DD} I_T = (0.36 μA/kHz) f + I_{DD}							μA
ON Resistance (AL Device) (Figure 9)	R_{ON}	5.0 10 15	– – –	880 400 220	– – –	250 120 80	1050 500 280	– – –	1200 550 320	Ω
ON Resistance (CL/CP Device) (Figure 9)	R_{ON}	5.0 10 15	– – –	880 450 250	– – –	250 120 80	1050 500 280	– – –	1200 520 300	Ω
ON Resistance Between Any Two Channels	$\triangle R_{ON}$	5.0 10 15	– – –	– – –	– – –	25 10 5.0	– – –	– – –	– – –	Ω
OFF Channel Leakage Current Any Channel (AL Device) All Channels OFF: MC14067B MC14097B	–	25 15 15	– – –	100 100 100	– – –	±0.01 ±0.08 ±0.04	100 100 100	– – –	– – –	nA
OFF Channel Leakage Current Any Channel (CL/CP Device) All Channels OFF: MC14067B MC14097B	–	15 15 15	– – –	1000 1000 1000	– – –	±0.01 ±0.08 ±0.04	1000 1000 1000	– – –	– – –	nA
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Output Capacitance MC14067B MC14097B	C_{out}	10 10	– –	– –	– –	60 32	– –	– –	– –	pF
Feedthrough Capacitance MC14069B MC14067B	C_{in-out}	10 10	– –	– –	– –	0.18 0.12	– –	– –	– –	pF
Control Inputs (Inhibit, A, B, C, D)										
Input Voltage# "0" Level V_{in} = V_{DD} (Figure 5)	V_{IL}	5.0 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	V
"1" Level	V_{IH}	5.0 10 15	3.5 7.0 11.0	– – –	3.5 7.0 11.0	2.75 5.50 8.25	– – –	3.5 7.0 11.0	– – –	V
Input Current	I_{in}	–	–	–	–	10	–	–	–	pA
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity is defined as the control input voltage coincident with the specified change, $\triangle V_{out}$, at an output in the OFF state.
**The formulas given are for the typical characteristics only at 25°C.
†Total Supply Current, I_T, is the current drawn at device terminals V_{DD} and V_{SS} for total current through the device. The channel component, $(V_{in} - V_{out})/R_{ON}$, should not be included.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}-V_{SS} Vdc	Typ All Types	Max AL Device	Max CL/CP Device	Unit
Propagation Delay Times	t_{PLH}, t_{PHL}					ns
Channel Input-to-Channel Output (R_L = 200 kΩ)						
MC14067B	(Figure 3)	5.0	35	55	90	
		10	15	25	40	
		15	12	18	30	
MC14097B		5.0	25	40	65	ns
		10	10	20	25	
		15	7	15	18	
Control Input-to-Channel Output						
Channel Turn-On Time (R_L = 10 kΩ)	t_{PZH}, t_{PZL}					ns
MC14067B/097B	(Figure 4)	5.0	240	260	600	
		10	115	175	290	
		15	75	115	190	
Channel Turn-Off Time (R_L = 300 Ω)						
MC14067B/097B	t_{PHZ}, t_{PLZ}	5.0	250	375	625	ns
	(Figure 4)	10	120	180	300	
		15	75	115	190	
Any Pair of Address Inputs to Output						ns
MC14067B	t_{PLH}, t_{PHL}	5.0	280	420	700	
		10	115	175	290	
		15	85	130	215	
MC14097B		5.0	250	375	625	ns
	(Figure 10)	10	100	150	250	
		15	75	115	190	
Sine Wave Distortion (R_L = 1 kΩ, f = 1 kHz)	–	10	0.3	–	–	%
ON Channel Bandwidth	BW					MHz
[R_L = 1 kΩ, V_{in} = ½ (V_{DD} – V_{SS}) p-p(sine-wave)]						
$20 \log_{10} \frac{V_{out}}{V_{in}}$ = –3 dB MC14067B	(Figure 5)	10	15	–	–	
MC14097B		10	25	–	–	
OFF Channel Isolation	–					MHz
[R_L = 1 kΩ, V_{in} = ½ (V_{DD} V_{SS}) p-p(sine-wave)]						
$20 \log_{10} \frac{V_{out}}{V_{in}}$ = –40 dB MC14067B	(Figure 5)	10	20	–	–	
MC14097B		10	12	–	–	
Crosstalk, Channel to Channel	–	10	20	–	–	MHz
[R_L = 1 kΩ, V_{in} = ½ (V_{DD} – V_{SS}) p-p(sine-wave)]						
$20 \log_{10} \frac{V_{out(B)}}{V_{in(A)}}$ = –40 dB)	(Figure 6)					
Crosstalk, Control Inputs-to-Channel Output	–	10	30	–	–	mV
(R1 = 1 kΩ, R_L = 10 kΩ, Control/Inhibit						
t_r = t_f = 20 ns)	(Figure 7)					
Maximum Control Frequency	–	10	5	–	–	MHz
(R_L = 1 kΩ, V_{out} = ½ V_{in})	(Figure 8)					

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 3 — PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS V_{in} to V_{out}

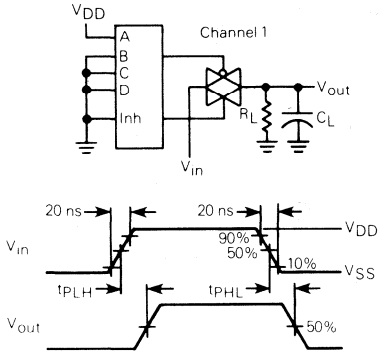


FIGURE 4 — TURN-ON AND DELAY TURN-OFF TEST CIRCUIT AND WAVEFORMS

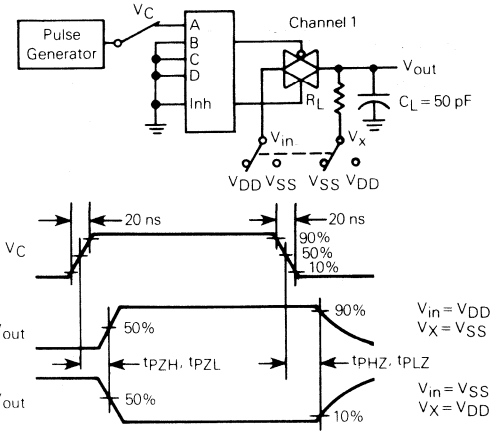


FIGURE 5 — BANDWIDTH AND OFF-CHANNEL ISOLATION TEST CIRCUIT

A, B, and C inputs used to turn ON or OFF the switch under test.

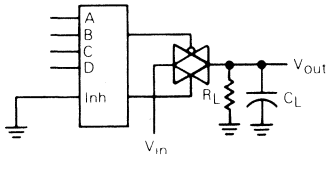


FIGURE 6 — CROSSTALK BETWEEN ANY TWO CHANNELS

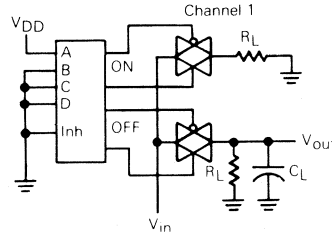


FIGURE 7 — CROSSTALK, CONTROL TO CHANNEL OUTPUT

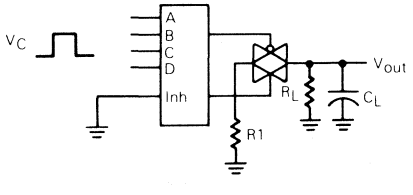


FIGURE 8 — MAXIMUM CONTROL FREQUENCY

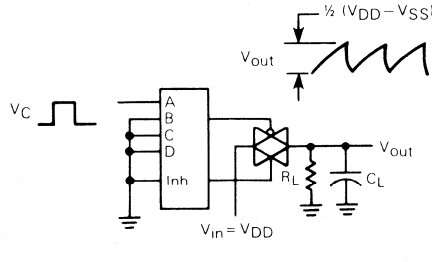


FIGURE 9 — CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT

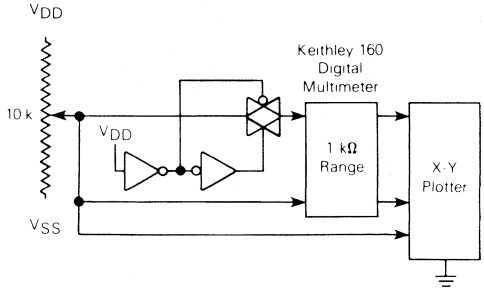
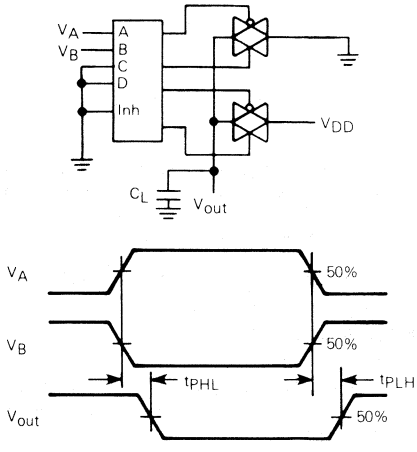


FIGURE 10 — PROPAGATION DELAY, ANY PAIR OF ADDRESS INPUTS to OUTPUT



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 11 — V_{DD} = 7.5 V, V_{SS} = −7.5 V

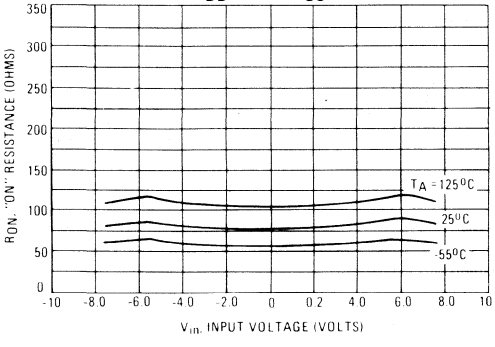


FIGURE 12 — V_{DD} = 5.0 V, V_{SS} = −5.0 V

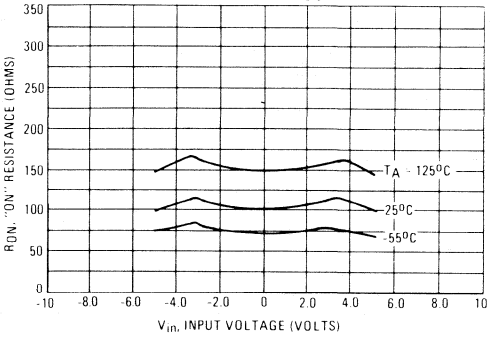


FIGURE 13 — V_{DD} = 2.5 V, V_{SS} = −2.5 V

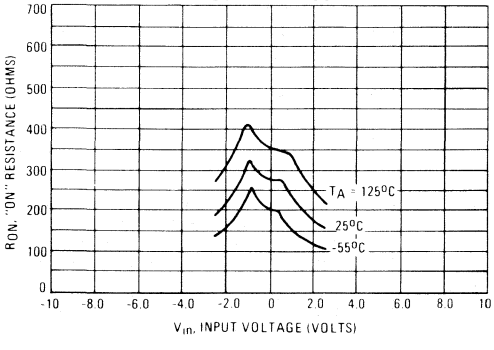
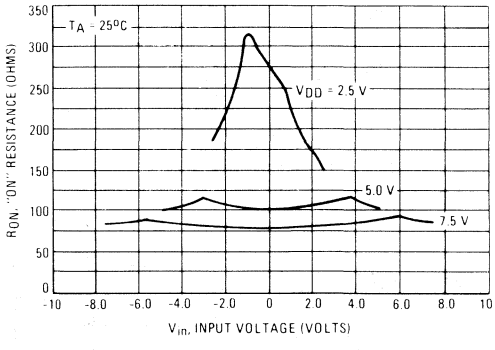


FIGURE 14 — COMPARISON AT 25°C, V_{DD} = −V_{SS}



MOTOROLA

MC14068B

CMOS SSI

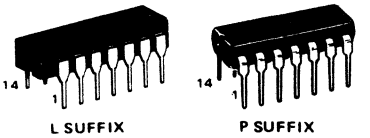
(LOW-POWER COMPLEMENTARY MOS)

8-INPUT "NAND" GATE

8 – INPUT "NAND" GATE

The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

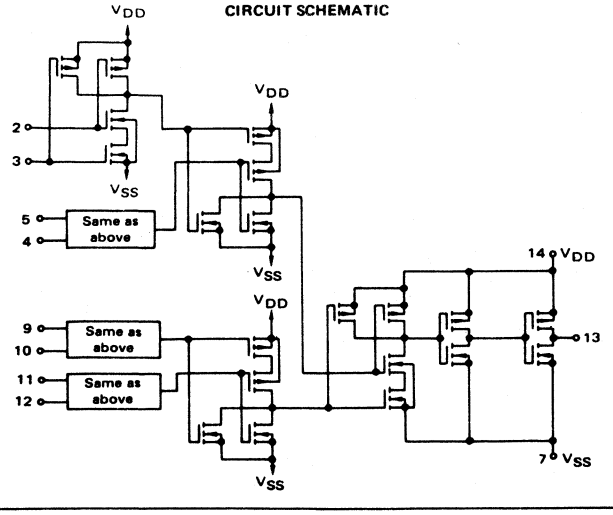
MC14XXXB — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

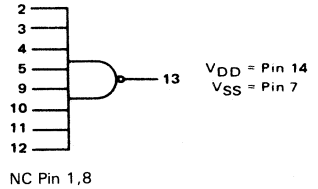
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



NC Pin 1,8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14069UB

HEX INVERTER

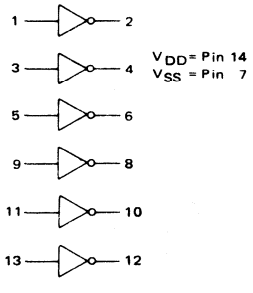
The MC14069UB hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications

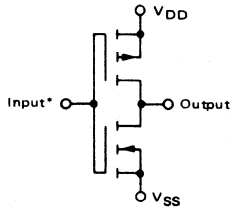
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)

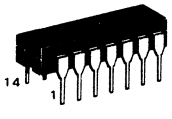


*Double diode protection on all inputs not shown.

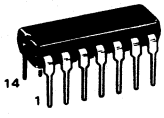
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXUB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT

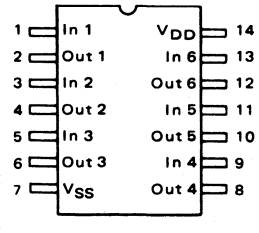
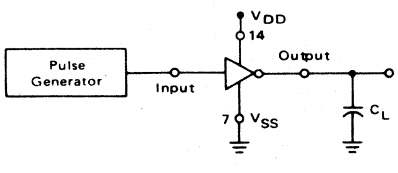
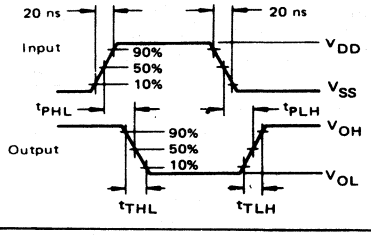


FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





3

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5 Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0 Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–			–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)	I_T	5.0	$I_T = (0.3\ \mu A/kHz)\ f + I_{DD}/6$							µAdc
		10	$I_T = (0.6\ \mu A/kHz)\ f + I_{DD}/6$							
		15	$I_T = (0.9\ \mu A/kHz)\ f + I_{DD}/6$							
Output Rise and Fall Times** (C_L = 50 pF)	t_{TLH}, t_{THL}									ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	–	–	100	200	–	–	
t_{TLH}, t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	–	–	50	100	–	–	
t_{TLH}, t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	–	–	40	80	–	–	
Propagation Delay Times** (C_L = 50 pF)	t_{PLH}, t_{PHL}									ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 20 ns		5.0	–	–	–	65	125	–	–	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 22 ns		10	–	–	–	40	75	–	–	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 17 ns		15	–	–	–	30	55	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device

†To calculate total supply current at loads other than 50 pf:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3}(C_L - 50)V_{DD}f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
0.5 Vdc min @ V_{DD} = 5.0 Vdc
1.0 Vdc min @ V_{DD} = 10 Vdc
1.0 Vdc min @ V_{DD} = 15 Vdc

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

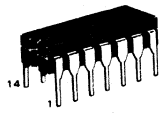
MC14070B
QUAD EXCLUSIVE "OR" GATE

MC14077B
QUAD EXCLUSIVE "NOR" GATE

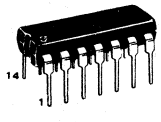
CMOS SSI
QUAD EXCLUSIVE "OR" AND "NOR" GATES

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- MC14070B – Replacement for CD4030B, CD4070B, and MC14507 Types
- MC14077B – Replacement for CD4077B Type



CASE 632
L SUFFIX
CERAMIC PACKAGE



CASE 646
P SUFFIX
PLASTIC PACKAGE

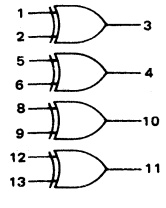
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

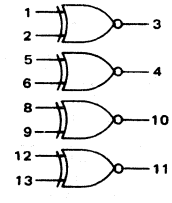
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

MC14070B
Quad Exclusive OR Gate

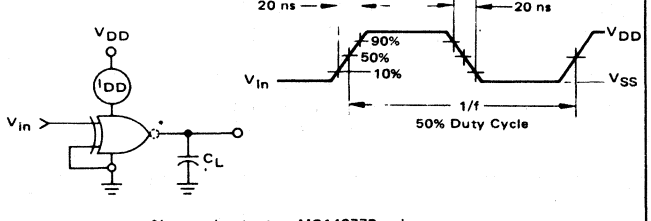


MC14077B
Quad Exclusive NOR Gate



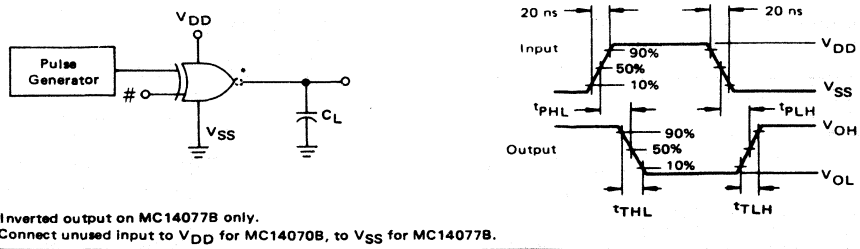
V_{DD} = Pin 14
V_{SS} = Pin 7
(Both Devices)

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



*Inverted output on MC14077B only.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



* Inverted output on MC14077B only.
#Connect unused input to V_{DD} for MC14070B, to V_{SS} for MC14077B.

ELECTRICAL CHARACTERISTICS

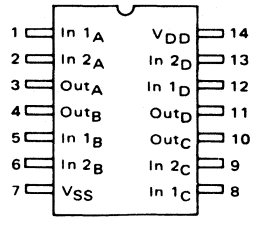
Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.3\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (0.6\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (0.9\ \mu A/kHz)\ f + I_{DD}$							
Output Rise and Fall Times** (C_L = 50 pF)	t_{TLH}, t_{THL}									ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	–	–	100	200	–	–	
t_{TLH}, t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	–	–	50	100	–	–	
t_{TLH}, t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	–	–	40	80	–	–	
Propagation Delay Times** (C_L = 50 pF)	t_{PLH}, t_{PHL}									ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 115 ns		5.0	–	–	–	175	350	–	–	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 47 ns		10	–	–	–	75	150	–	–	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 37 ns		15	–	–	–	50	100	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



MOTOROLA

MC14071B

QUAD 2-INPUT "OR" GATE

The MC14071 and MC14071B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14071B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4081B

MAXIMUM RATINGS (Voltages referenced to V_{SS})

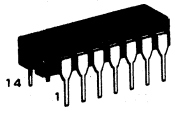
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics of this device.

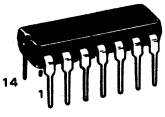
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



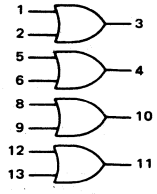
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

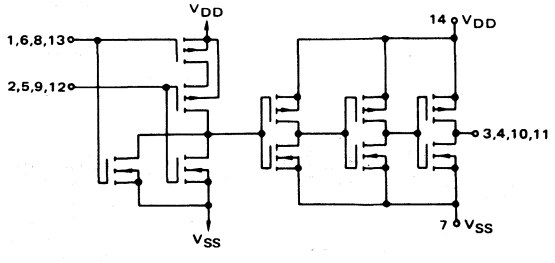
Delete for Non-B Device

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATICS
(1/4 of Device Shown)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14072B

DUAL 4 INPUT "OR" GATE

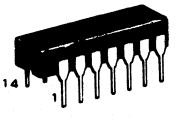
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4072B

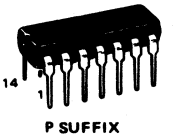
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

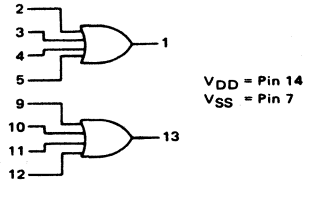
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

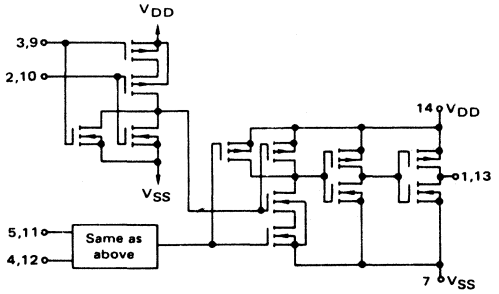
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

LOGIC DIAGRAM



CIRCUIT SCHEMATICS
(1/2 of Device Shown)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14073B

TRIPLE 3–INPUT "AND" GATE

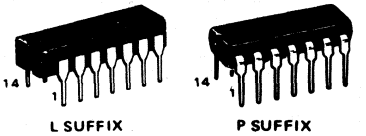
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4073B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "AND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

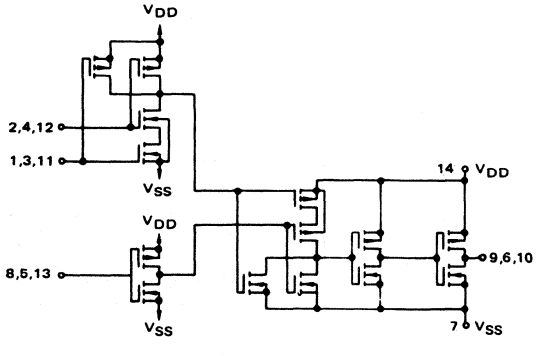
MC14XXXB — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

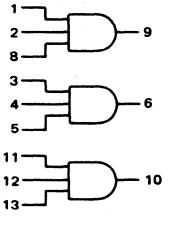
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATICS
(1/3 of Device Shown)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

3

MOTOROLA

MC14075B

TRIPLE 3–INPUT "OR" GATE

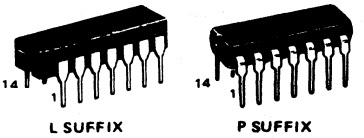
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4075B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE 3-INPUT "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

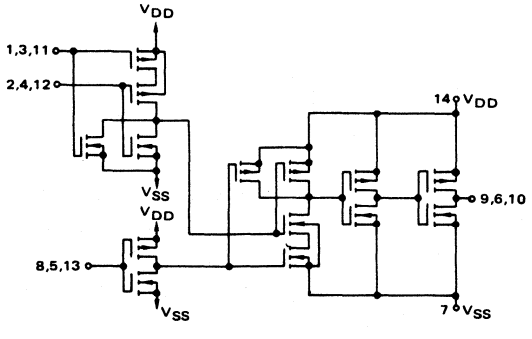
MC14XXXB — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

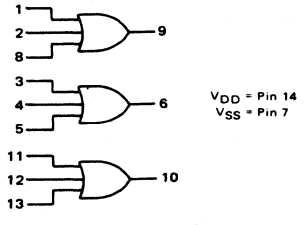
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATICS
(1/3 of Device Shown)



LOGIC DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14076B

4-BIT D-TYPE REGISTER with THREE-STATE OUTPUTS

The MC14076B 4-Bit Register consists of four D-type flip-flops operating synchronously from a common clock. OR gated output-disable inputs force the outputs into a high-impedance state for use in bus organized systems. OR gated data-disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master reset is provided to clear all four flip-flops simultaneously independent of the clock or disable inputs.

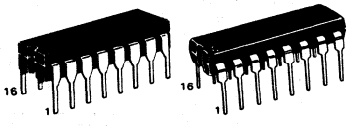
- Three-State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- For Bus Buffer Registers
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD D-TYPE REGISTER with THREE STATE OUTPUTS

3



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

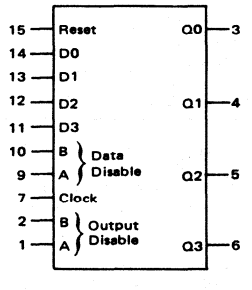
FUNCTION TABLE

INPUTS					OUTPUT
		Data Disable		Data	
Reset	Clock	A	B	D	Q
1	X	X	X	X	0
0	0	X	X	X	Q_n
0	⎍	1	X	X	Q_n
0	⎍	X	1	X	Q_n
0	⎍	0	0	0	0
0	⎍	0	0	1	1

When either output disable A or B (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

X = Don't Care.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

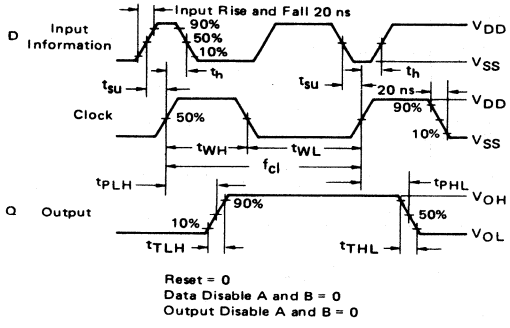
Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.75\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (1.50\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (2.25\ \mu A/kHz)\ f + I_{DD}$							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$$

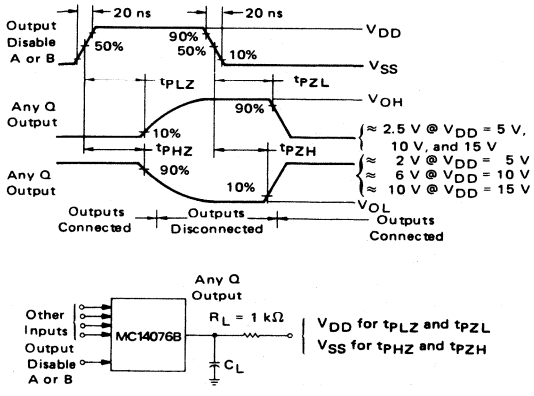
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

FIGURE 1 – TIMING DIAGRAM



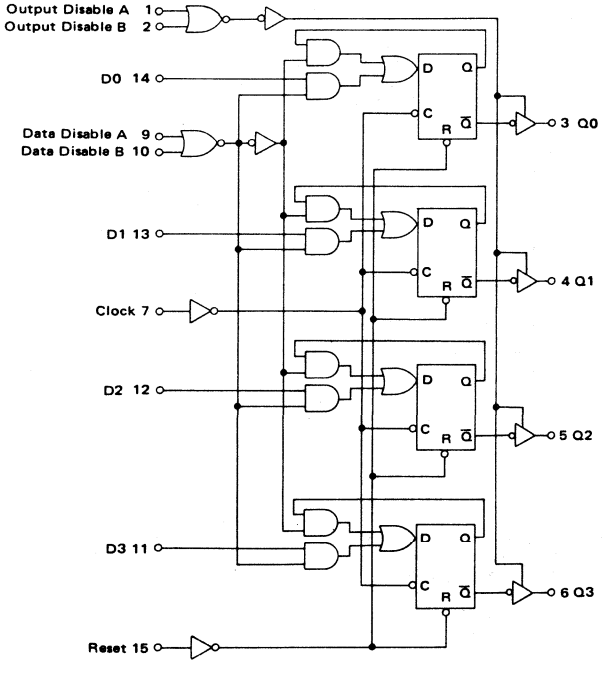
Reset = 0
Data Disable A and B = 0
Output Disable A and B = 0

FIGURE 2 – THREE-STATE PROPAGATION DELAY WAVESHAPE AND CIRCUIT

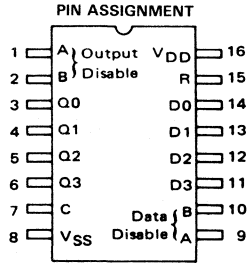


3

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time, All B-Series Gates	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time, All B-Series Gates	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	
Reset to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	
3-State Propagation Delay, Output "1" or "0" to High Impedance	t_{PHZ}, t_{PLZ}	5.0	–	150	300	ns
		10	–	60	120	
		15	–	45	90	
3-State Propagation Delay, High Impedance to "1" or "0" Level	t_{PZH}, t_{PZL}	5.0	–	200	400	ns
		10	–	80	160	
		15	–	60	120	
Clock Pulse Width	t_{WH}	5.0	260	130	–	ns
		10	110	55	–	
		15	80	40	–	
Reset Pulse Width	t_{WH}	5.0	370	185	–	ns
		10	150	75	–	
		15	110	55	–	
Data Setup Time	t_{su}	5.0	30	15	–	ns
		10	10	5	–	
		15	4	2	–	
Data Hold Time	t_h	5.0	130	65	–	ns
		10	60	30	–	
		15	50	25	–	
Data Disable Setup Time	t_{su}	5.0	220	110	–	ns
		10	80	40	–	
		15	50	25	–	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
Clock Pulse Frequency	f_{cl}	5.0	–	3.6	1.8	MHz
		10	–	9.0	4.5	
		15	–	12	6.0	

*The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14077B

QUAD EXCLUSIVE "NOR" GATE

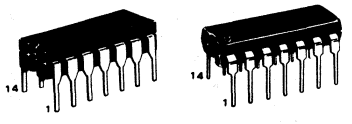
FOR COMPLETE DATA SEE MC14070B

CMOS SSI

QUAD EXCLUSIVE "OR" AND "NOR" GATES

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- **MC14070B** – Replacement for CD4030B, CD4070B, and MC14507 Types
- MC14077B – Replacement for CD4077B Type



CASE 632
L SUFFIX
CERAMIC PACKAGE

CASE 646
P SUFFIX
PLASTIC PACKAGE

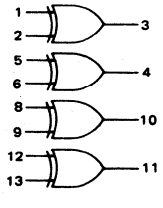
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

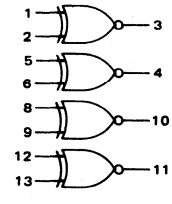
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

MC14070B
Quad Exclusive OR Gate

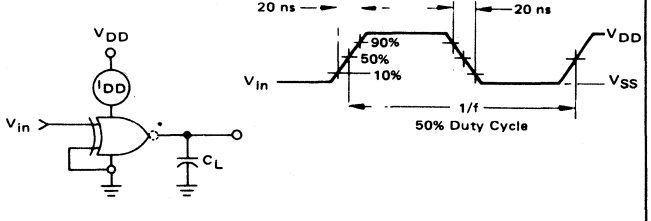


MC14077B
Quad Exclusive NOR Gate



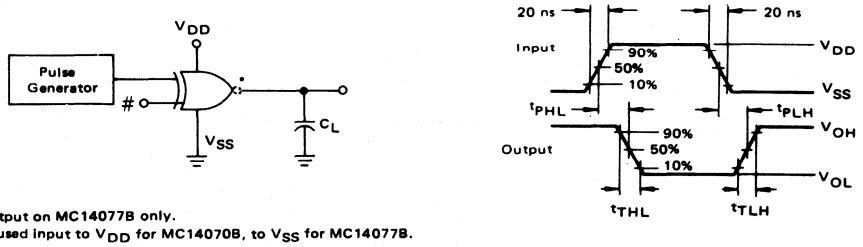
V_{DD} = Pin 14
V_{SS} = Pin 7
(Both Devices)

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



*Inverted output on MC14077B only.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



*Inverted output on MC14077B only.
#Connect unused input to V_{DD} for MC14070B, to V_{SS} for MC14077B.

MOTOROLA

MC14078B

8 – INPUT "NOR" GATE

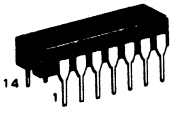
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs

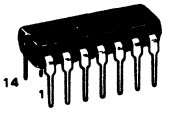
CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

8-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

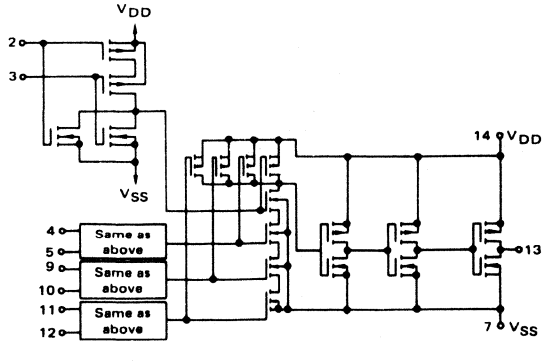
MC14XXXB — Suffix — Denotes
- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

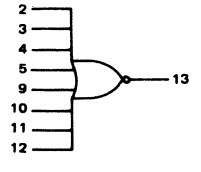
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

N.C. pins 1, 6, and 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14081B

QUAD 2-INPUT "AND" GATE

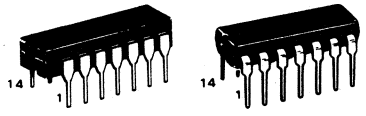
The MC14081 and MC14081B are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range. (MC14081B only)
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4081B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "AND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

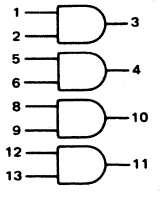
Delete for Non-B Device

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

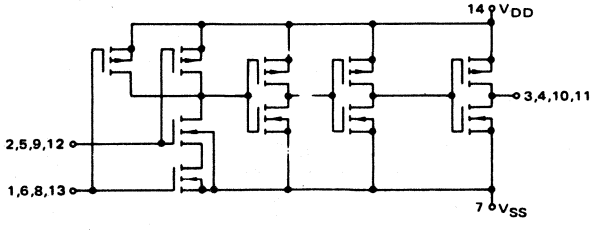
See the MC14001B data sheet for complete characteristics of this device.

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATICS
(1/4 of Device Shown)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14082B

DUAL 4-INPUT "AND" GATE

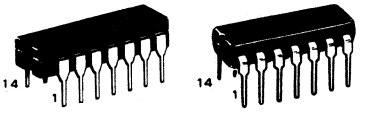
The B Series logic gates are constructed with P and N channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4082B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "AND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

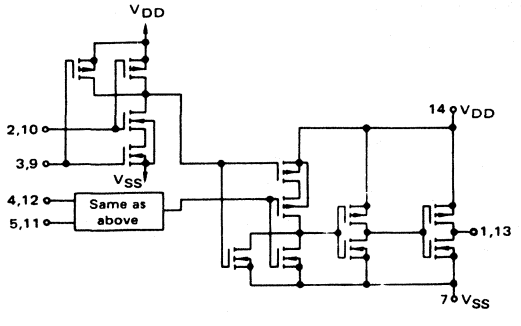
MC14XXXB — Suffix — Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

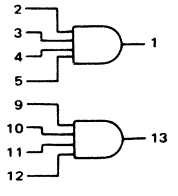
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See the MC14001B data sheet for complete characteristics for this device.

CIRCUIT SCHEMATICS
(1/2 of Device Shown)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14093B

Advance Information

CMOS SSI

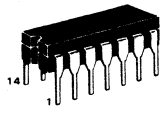
(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" SCHMITT TRIGGER

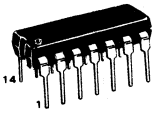
QUAD 2-INPUT "NAND" SCHMITT TRIGGER

The MC14093B Schmitt trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14093B may be used in place of the MC14011B quad 2-input NAND gate for enhanced noise immunity or to "square up" slowly changing waveforms.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Compatible with CD4093
- Can be Used to Replace MC14011B



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

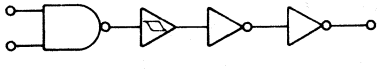
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

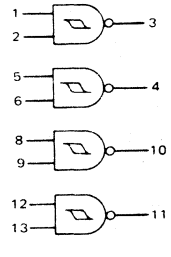
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

EQUIVALENT CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

3

3

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	–	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	–	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	–	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	–	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	–	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	–	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.2\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (2.4\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.6\ \mu A/kHz)\ f + I_{DD}$							
Hysteresis Voltage (Pins 1, 5, 8 and 12 held high or Pins 2, 6, 9 and 13 held high)	V_H‡	5.0	0.20	0.62	0.17	0.26	0.6	0.13	0.6	Vdc
		10	0.29	0.85	0.25	0.38	0.8	0.20	0.8	
		15	0.39	1.20	0.33	0.50	0.9	0.27	1.1	
Threshold Voltage (Pins 2, 5, 9, 12, held high) Positive-Going	V_{T+}	5.0	1.90	4.15	1.80	2.70	4.05	1.70	4.05	Vdc
		10	3.05	6.75	2.95	4.43	6.65	2.85	6.65	
		15	4.12	9.15	4.02	6.03	9.05	3.92	9.05	
Negative-Going	V_{T-}	5.0	1.63	3.76	1.63	2.44	3.66	1.53	3.66	Vdc
		10	2.70	6.18	2.70	4.05	6.08	2.60	6.08	
		15	3.59	8.40	3.69	5.53	8.30	3.70	8.30	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

‡$V_H = V_{T+} - V_{T-}$ (But maximum variation of V_H is specified as less than V_{T+} max − V_{T-} min).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0	–	125	250	ns
		10	–	50	100	
		15	–	40	80	

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVE FORMS

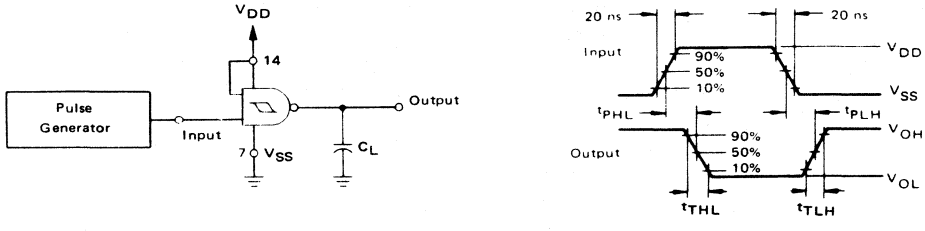
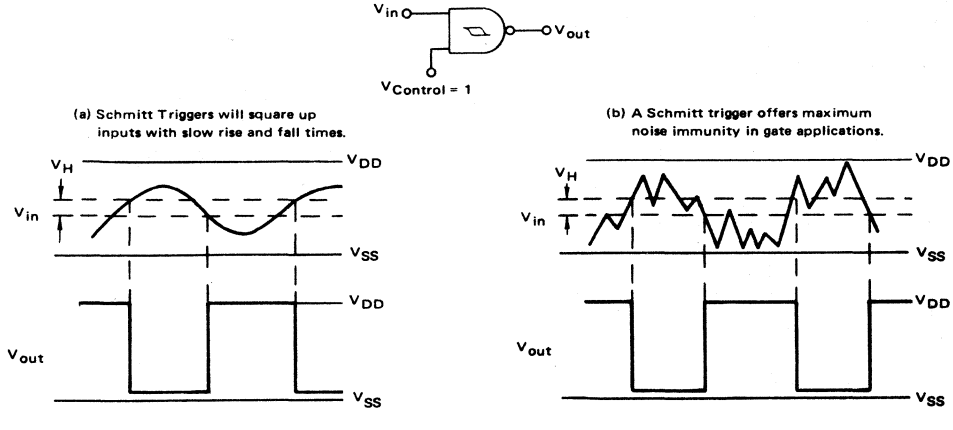
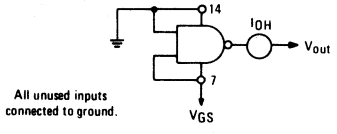


FIGURE 2 – TYPICAL SCHMITT TRIGGER APPLICATIONS



3

FIGURE 3 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT



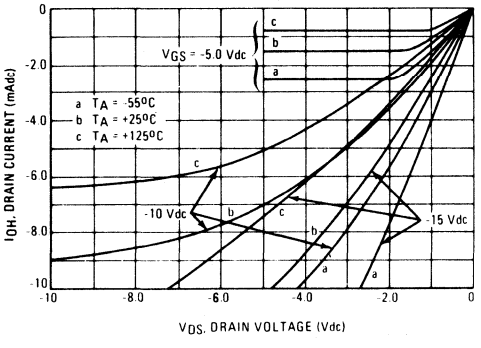
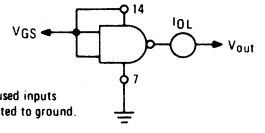


FIGURE 4 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



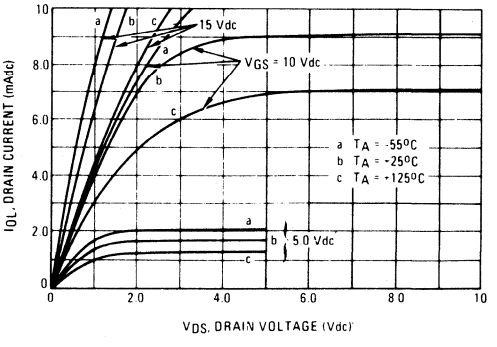
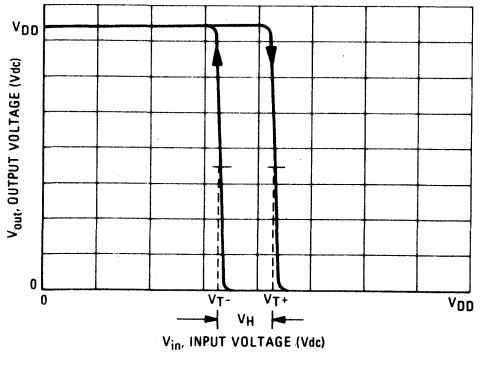
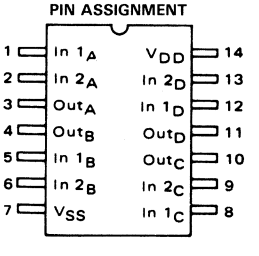


FIGURE 5 – TYPICAL TRANSFER CHARACTERISTICS



PIN ASSIGNMENT



MOTOROLA

MC14094B

8-STAGE SHIFT/STORE REGISTER WITH THREE-STATE OUTPUTS

The MC14094B combines an 8-stage shift register with a data latch for each stage and a three-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q_S output data is for use in high-speed cascaded systems. The Q'_S output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by three-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

- Three-State Outputs
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTTL Loads Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Three-State Bus Compatible
- Pin-for-Pin Compatible with CD4094B

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

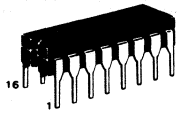
Clock	Output Enable	Strobe	Data	Parallel Outputs Q1	Parallel Outputs Q_N	Serial Outputs Q_S*	Serial Outputs Q'_S
↑	0	X	X	3S	3S	Q7	No Chg.
↓	0	X	X	3S	3S	No Chg.	Q7
↑	1	0	X	No Chg.	No Chg.	Q7	No Chg.
↑	1	1	0	0	Q_N-1	Q7	No Chg.
↑	1	1	1	1	Q_N-1	Q7	No Chg.
↓	1	1	1	No Chg.	No Chg.	No Chg.	Q7

3S = Three-State
X = Don't Care
*At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.

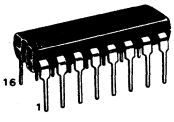
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-STAGE SHIFT/STORE REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

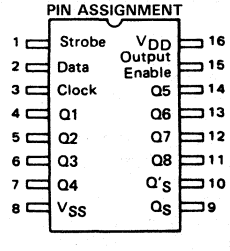


P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (4.1 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (14 µA/kHz) f + I_{DD}							
		15	I_T = (140 µA/kHz) f + I_{DD}							
3-State Output Leakage Current	I_{TL}	18	–	±0.4	–	±0.0001	±0.4	–	±12	µAdc

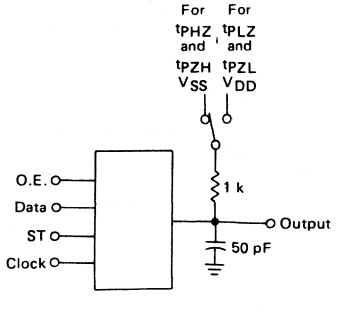
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

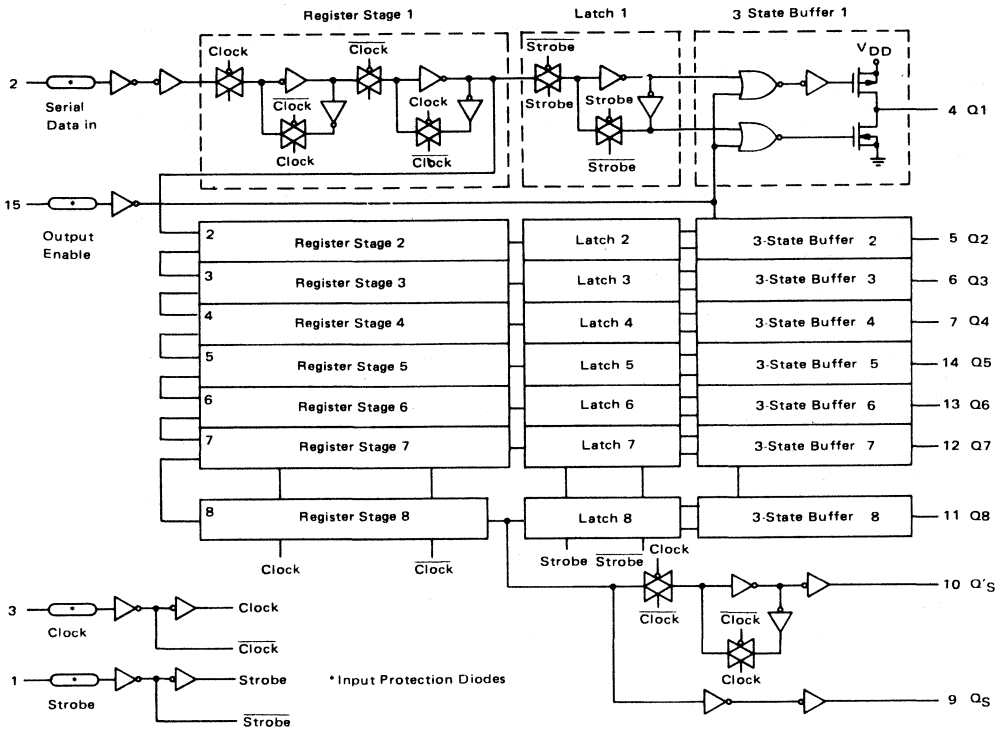
Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Serial out QS						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 305 ns		5.0	–	350	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 82 ns		15	–	95	190	
Clock to Serial out Q'S						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 350 ns		5.0	–	230	460	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 149 ns		10	–	110	220	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 62 ns		15	–	75	150	
Clock to Parallel out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 375 ns		5.0	–	420	840	
t_{PLH}, t_{PHL} = (0.35 ns/pF) C_L + 177 ns		10	–	195	390	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 122 ns		15	–	135	270	
Strobe to Parallel out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 245 ns		5.0	–	290	580	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 127 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	–	100	200	
Output Enable to Output						
t_{PHZ}, t_{PZL} = (0.90 ns/pF) C_L + 95 ns		5.0	–	140	280	
t_{PHZ}, t_{PZL} = (0.36 ns/pF) C_L + 57 ns		10	–	75	150	
t_{PHZ}, t_{PZL} = (0.26 ns/pF) C_L + 42 ns		15	–	55	110	
t_{PLZ}, t_{PZH} = (0.90 ns/pF) C_L + 180 ns		5.0	–	225	450	
t_{PLZ}, t_{PZH} = (0.36 ns/pF) C_L + 77 ns		10	–	95	190	
t_{PLZ}, t_{PZH} = (0.26 ns/pF) C_L + 57 ns		15	–	70	140	
Setup Time	t_{su}					ns
Data in to Clock		5.0	125	60	–	
		10	55	30	–	
		15	35	20	–	
Clock Pulse Width, High	t_{WH}	5.0	200	100	–	ns
		10	100	50	–	
		15	83	40	–	
Clock Rise Time	$t_{r(cl)}$	5	15	–	–	μs
		10	5.0	–	–	
		15	4.0	–	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.25	MHz
		10	–	5.0	2.5	
		15	–	6.0	3.0	
Strobe Pulse Width	t_{WL}	5.0	200	100	–	ns
		10	80	40	–	
		15	70	35	–	

* The formulae given are for the typical characteristics only.

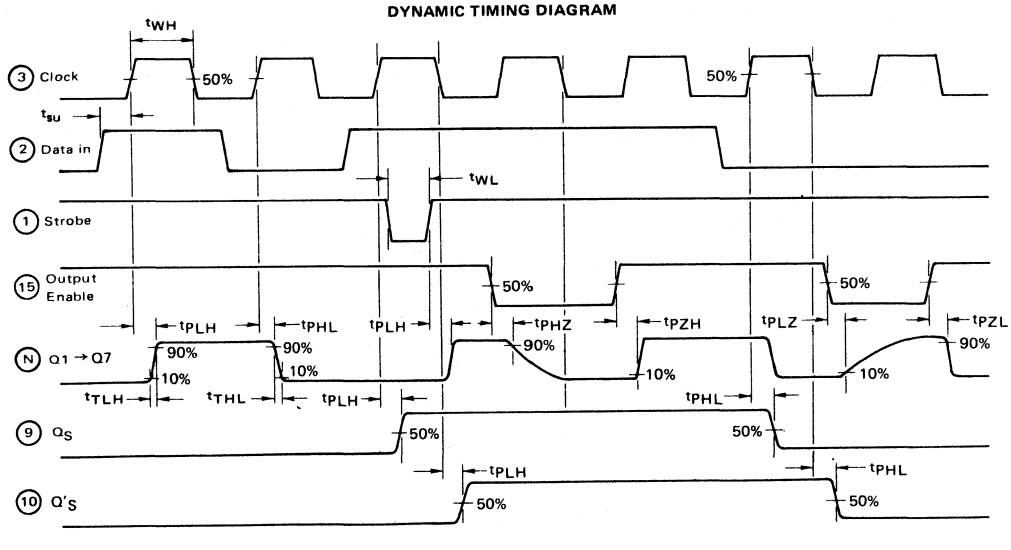
3-STATE TEST CIRCUIT



BLOCK DIAGRAM



DYNAMIC TIMING DIAGRAM



MOTOROLA

MC14097B

FOR COMPLETE DATA
SEE MC14067B

Advance Information

CMOS
(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/
DEMULTIPLEXERS

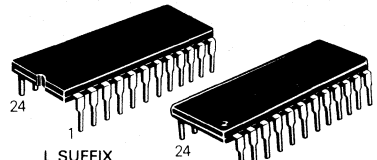
ANALOG MULTIPLEXERS/DEMULTIPLEXERS

The MC14067 and MC14097 multiplexers/demultiplexers are digitally controlled transmission gates featuring low ON resistance and very low leakage current. These devices can be used in either digital or analog applications.

The MC14067 is a 16-channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C and D. These control inputs select 1-of-16 channels by turning ON the appropriate transmission gate (see MC14067 truth table).

The MC14097 is a differential 8-channel multiplexer/demultiplexer with an inhibit and three binary control inputs A, B and C. These control inputs select 1 of 8 pairs of channels by turning ON the appropriate transmission gates (see MC14097 truth table).

- Low ON Resistance: 80 Ω @ $V_{DD} - V_{SS} = 15$ V
- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Transmits Frequencies Up to 65 MHz @10 V
- Low Noise
- Pin for Pin Replacement for CD4067B and CD4097B



L SUFFIX
CERAMIC PACKAGE
CASE 623

P SUFFIX
PLASTIC PACKAGE
CASE 709

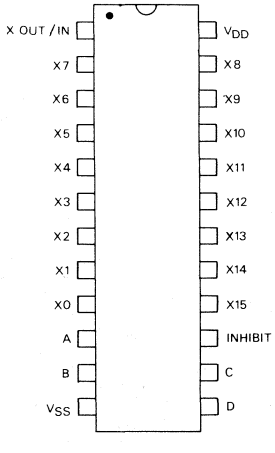
ORDERING INFORMATION

MC14XXXB — Suffix Denotes

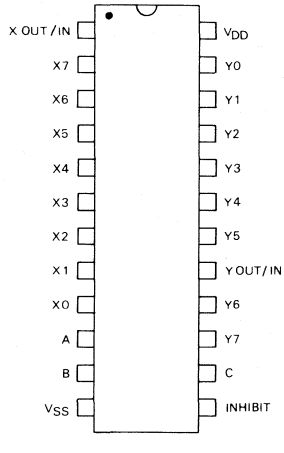
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENTS

MC14067B



MC14097B



ADI-919

MOTOROLA

MC14099B
MC14599B

8-BIT ADDRESSABLE LATCHES

The MC14099B and MC14599B are 8-bit addressable latches. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. Chip enable must be high for writing into MC14599B. For the MC14599B the data pin is a bidirectional data port and for the MC14099B the input is a unidirectional write only port. The Write/$\overline{\text{Read}}$ line controls this port in the MC14599B.

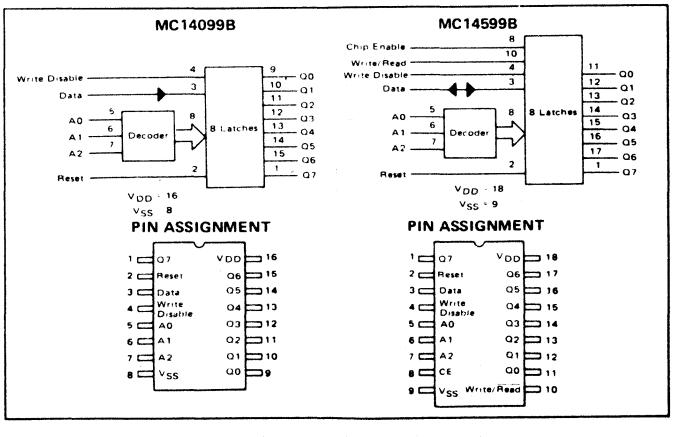
The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/$\overline{\text{Read}}$ or Chip Enable.

A Master Reset capability is available on both parts.

- Serial Data Input
- Parallel Output
- Low Input Capacitance – 5.0 pF typical
- Master Reset
- Noise Immunity – 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B
- Pin for pin compatible with Fairchild 4724.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



PIN ASSIGNMENT

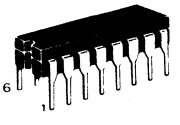
PIN ASSIGNMENT

CMOS MSI

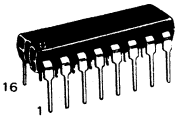
(LOW-POWER COMPLEMENTARY MOS)

8-BIT ADDRESSABLE LATCH

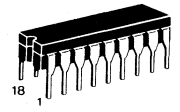
MC14599B WITH BIDIRECTIONAL PORT



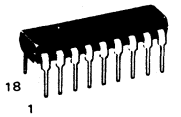
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 726



P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Input Capacitance MC14599B – Data (pin 3) (V_{in} = 0)	C_{in}	–	–	–	–	15.0	22.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.5 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.0 μA/kHz) f + I_{DD}							
		15	I_T = (4.5 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

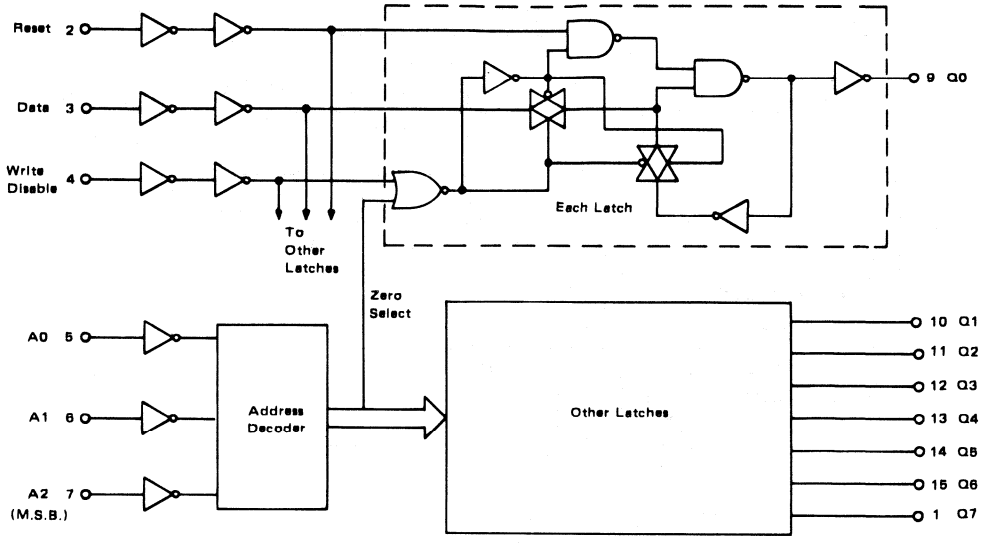
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L +32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L +20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L +20 ns		15	–	40	80	
Propagation Delay Time	t_{PHL}, t_{PLH}					ns
Data to Output		5.0	–	200	400	
		10	–	75	150	
		15	–	50	100	
Write Disable to Output		5.0	–	200	400	ns
		10	–	80	160	
		15	–	60	120	
Reset to Output		5.0	–	175	350	ns
		10	–	80	160	
		15	–	65	130	
Address to Output CE to Output (MC14599B only)		5.0	–	225	450	ns
		10	–	100	200	
		15	–	75	150	
Propagation Delay Time, MC14599B only	t_{PHL}, t_{PLH}					ns
Chip Enable, Write/$\overline{\text{Read}}$ to Data		5.0	–	200	400	
		10	–	80	160	
		15	–	65	130	
Address to Data		5.0	–	200	400	ns
		10	–	90	180	
		15	–	75	150	
Pulse Widths	t_{WH}, t_{WL}					ns
Data		5.0	200	100	–	
		10	100	50	–	
		15	80	40	–	
Address		5.0	400	200	–	ns
		10	200	100	–	
		15	125	65	–	
Reset		5.0	150	75	–	ns
		10	75	40	–	
		15	50	25	–	
Write Disable		5.0	320	160	–	ns
		10	160	80	–	
		15	120	60	–	
Set Up Time	t_{su}					ns
Data		5.0	100	50	–	
		10	50	25	–	
		15	35	20	–	
Hold Time	t_h					ns
Data		5.0	150	75	–	
		10	75	40	–	
		15	50	25	–	

* The formulae given are for the typical characteristics only.

MC14099B
FUNCTION DIAGRAM

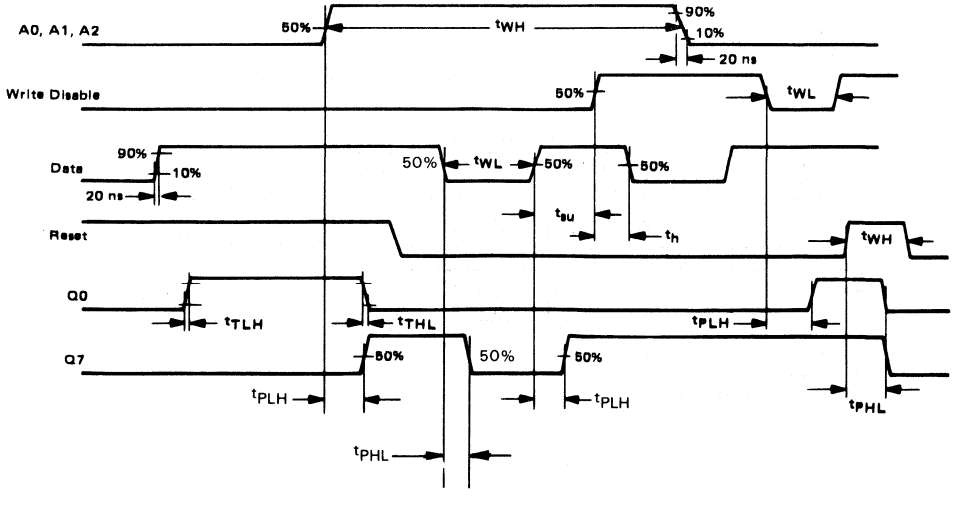


TRUTH TABLE

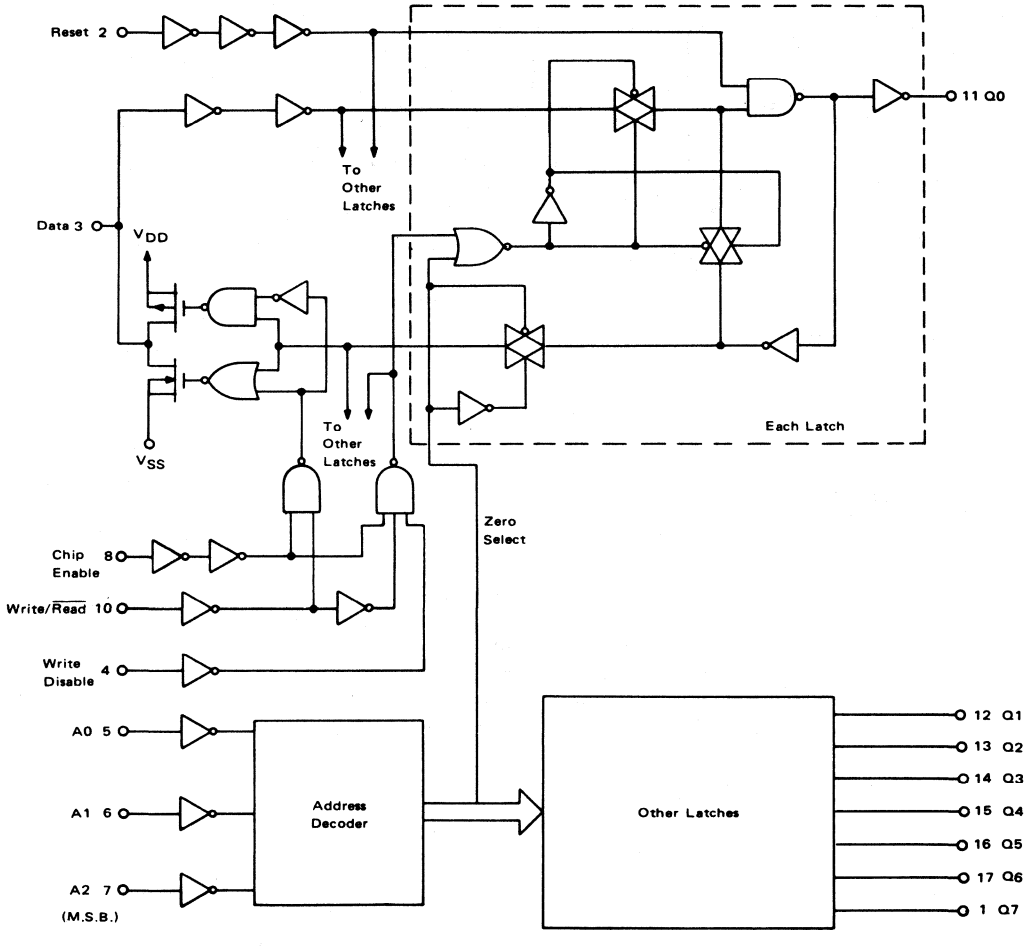
Write Disable	Reset	Addressed Latch	Unaddressed Latch
0	0	Data	Q_n*
0	1	Data	Reset†
1	0	Q_n*	Q_n*
1	1	Reset	Reset

* Q_n is previous state of latch.
† Reset to zero state.

TIMING DIAGRAM



MC14599B
FUNCTION DIAGRAM

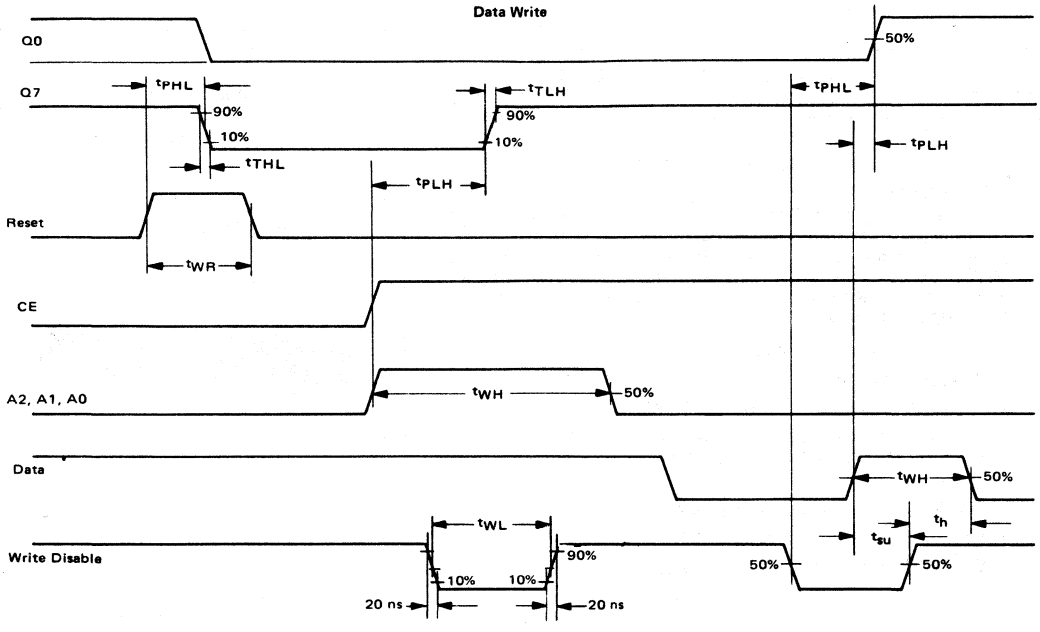


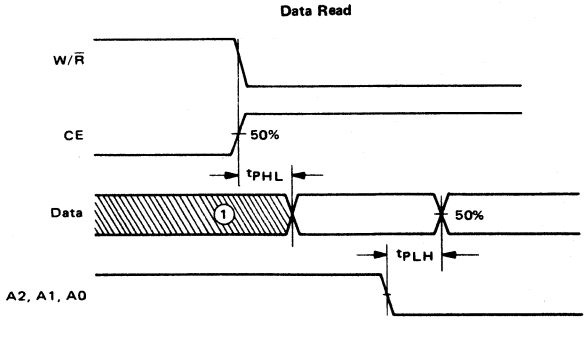
TRUTH TABLE

Chip Enable	Write/$\overline{\text{Read}}$	Write Disable	Reset	Addressed Latch	Other Latches	Data Pin
0	X	X	0	*	*	Z
1	1	0	0	Data	*	Input
1	1	1	0	*	*	Z
1	0	X	0	*	*	Q_n
X	X	X	1	0	0	Z/0

X = Don't care.
* = No change in state of latch.
Z = High impedance.
Q_n = State of addressed latch.

MC14599B
TIMING DIAGRAMS





NOTE: 1. Invalid Data Output
2. Reset in LOW State

MOTOROLA

MC14106B

Product Preview

CMOS SSI

(LOW POWER COMPLEMENTARY MOS)

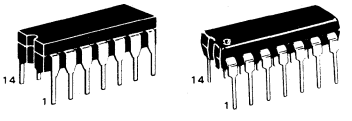
HEX
SCHMITT TRIGGER

3

HEX SCHMITT TRIGGER

The MC14106B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14106B may be used in place of the MC14069UB hex inverter for enhanced noise immunity or to "square up" slowly changing waveforms.

- Increased Hysteresis Voltage
- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD40106B and MM74C14
- Can Be Used to Replace MC14069UB



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

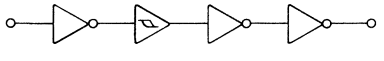
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

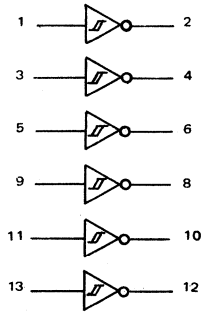
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

EQUIVALENT CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14160B
DECADE COUNTER
with Asynchronous Clear

MC14161B
4-BIT BINARY COUNTER
with Asynchronous Clear

MC14162B
DECADE COUNTER
with Synchronous Clear

MC14163B
4-BIT BINARY COUNTER
with Synchronous Clear

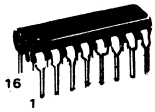
CMOS MSI

SYNCHRONOUS PROGRAMMABLE 4-BIT COUNTERS

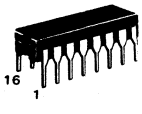
The MC14160B – MC14163B are synchronous programmable counters constructed with complementary MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These counters are functionally equivalent to the 74160–74163 TTL counters.

Two are synchronous programmable decade counters with asynchronous and synchronous clear inputs respectively (MC14160B, MC14162B. The other two are synchronous programmable 4-bit binary counters with the asynchronous and synchronous clear respectively (MC14161B, MC14163B).

- Internal Look-Ahead for Fast Counting
- Carry Output for N-Bit Cascading
- Synchronously Programmable
- Synchronous Counting
- Load Control Line
- Synchronous or Asynchronous Clear
- Positive Edge Clocked



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

ORDERING INFORMATION

MC14xxxB — Suffix — Denotes

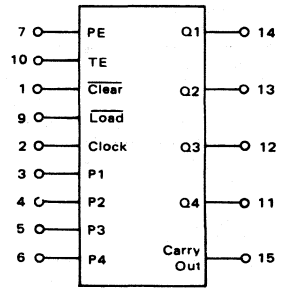
Suffix	Denotes
L	Ceramic Package
P	Plastic Package
A	Extended Operating Temperature Range
C	Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

3

3

ELECTRICAL CHARACTERISTICS

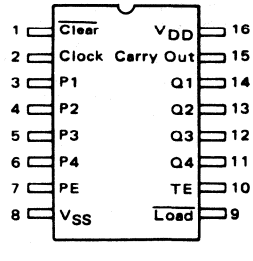
Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.56 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.1 μA/kHz) f + I_{DD}							
		15	I_T = (1.9 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT

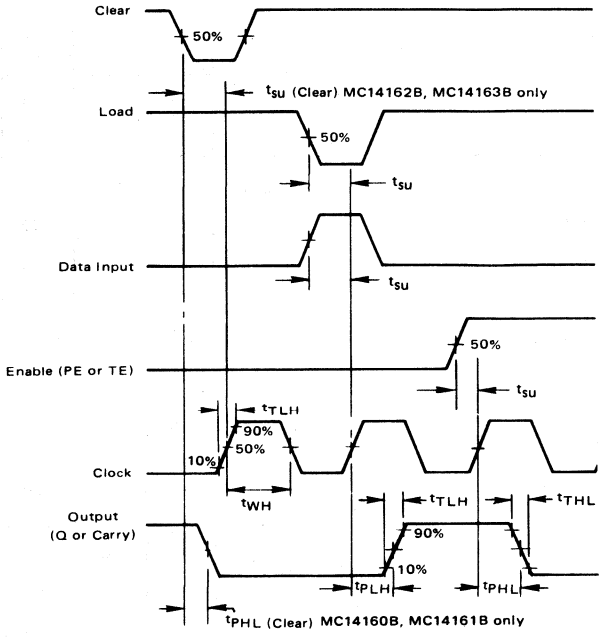


SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{TLH} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 305 ns		5.0	–	350	700	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns		15	–	100	200	
Clock to Carry Out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 395 ns		5.0	–	440	880	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 167 ns		10	–	185	370	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 112 ns		15	–	125	250	
TE to Carry Out						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 255 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 112 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 77 ns		15	–	90	180	
Clear to Q (MC14160B, MC14161B only)						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 110 ns		5.0	–	350	700	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 37 ns		10	–	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 22 ns		15	–	100	200	
Minimum Setup Time						
Data to Clock	t_{su}	5.0	320	160	–	ns
		10	130	65	–	
		15	90	45	–	
Load to Clock		5.0	600	300	–	
		10	260	130	–	
		15	180	90	–	
Enable to Clock (PE or TE)		5.0	420	210	–	
		10	170	85	–	
		15	120	60	–	
Clear to Clock (MC14162B, MC14163B only)		5.0	310	155	–	
		10	110	55	–	
		15	70	35	–	
Clock Pulse Width, High	t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	70	35	–	
Clock Rise Time	t_{TLH}	5	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
Clock Pulse Frequency	f_{cl}	5.0	–	2.0	1.0	MHz
		10	–	5.0	2.5	
		15	–	8.0	4.0	

*The formulae given are for the typical characteristics only.

SWITCHING WAVEFORMS

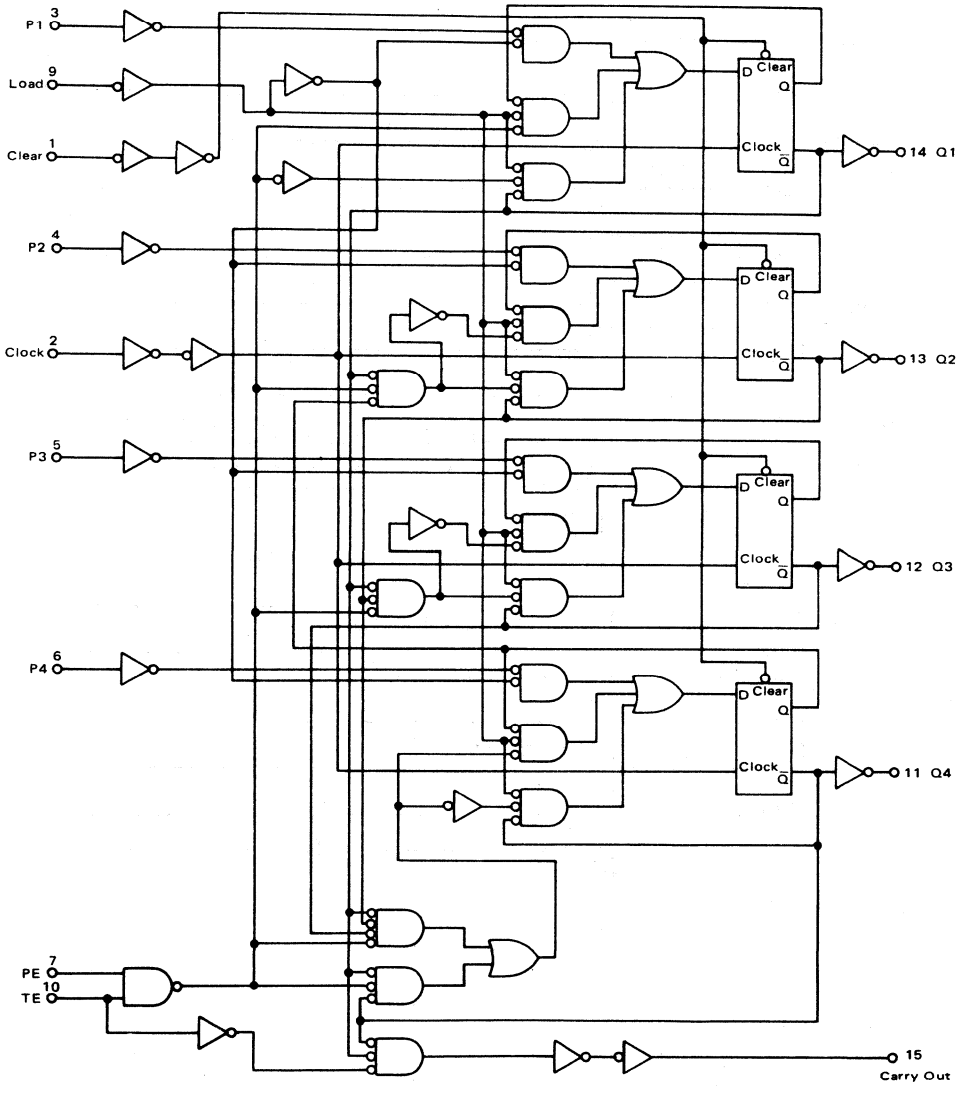


FUNCTIONAL DESCRIPTION

These counters are fully programmable; that is the outputs may be preset to either level. As presetting is synchronous, settling up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the MC14160B, MC14161B is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load or enable inputs. The clear function for the MC14162B and MC14163B is synchronous and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily; decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (PE, TE) must be high to count, and enable input TE fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages.

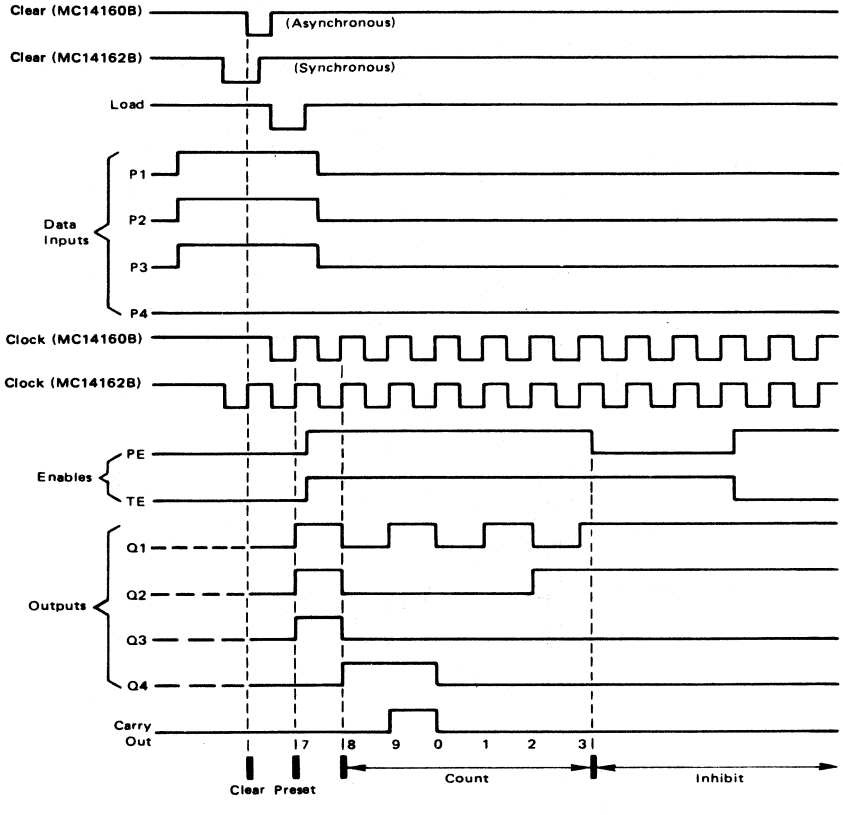
MC14160B, MC14162B LOGIC DIAGRAM
(Clear is synchronous for MC14162B)



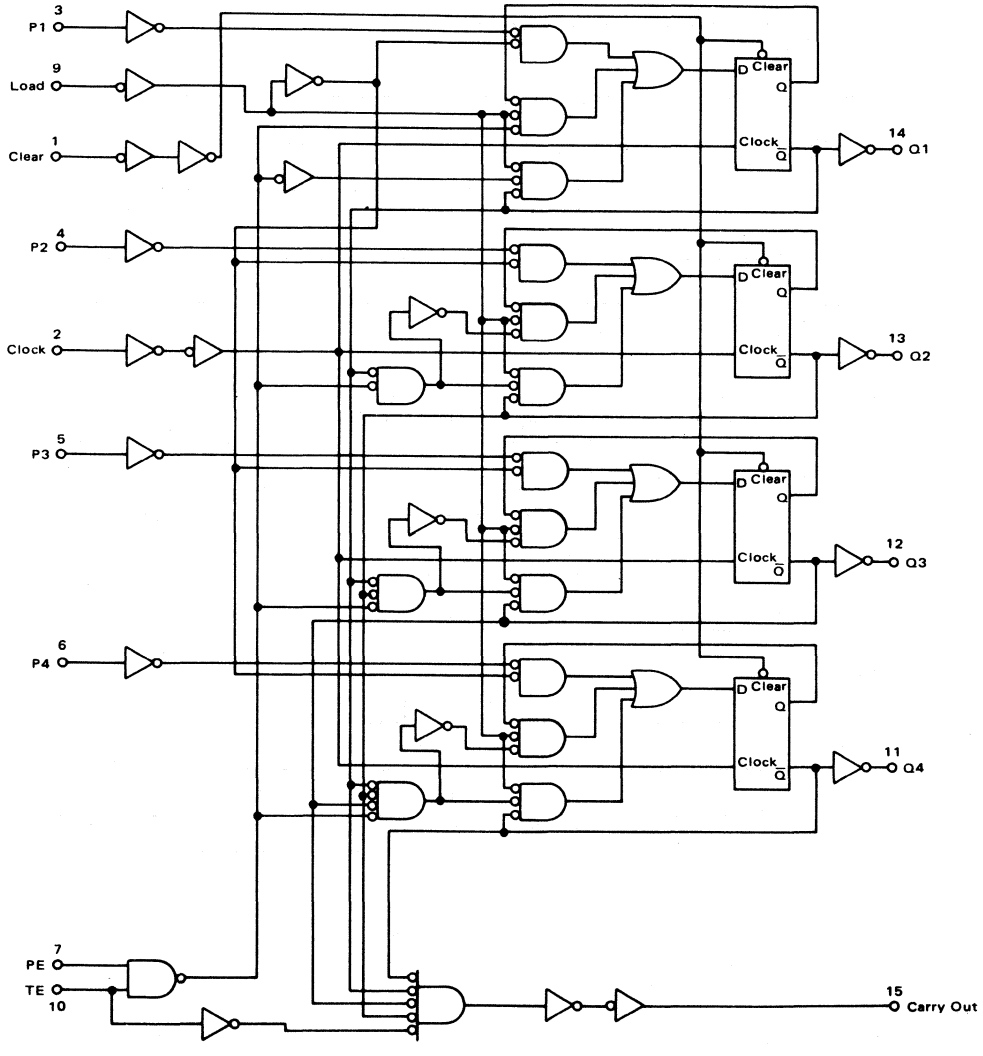
MC14160B, MC14162B TIMING DIAGRAM

Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit



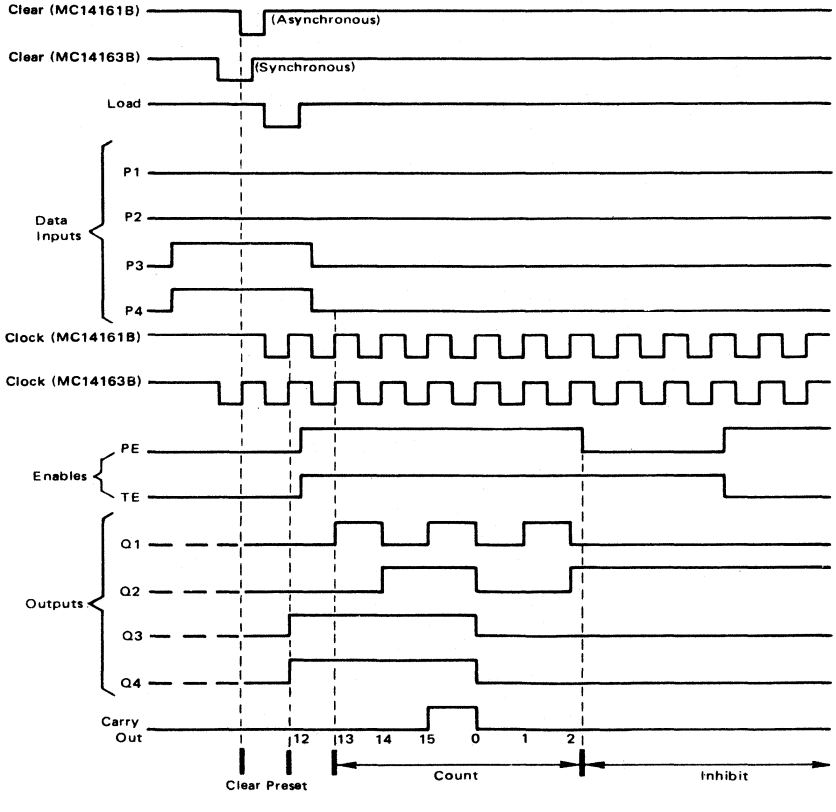
MC14161B, MC14163B LOGIC DIAGRAM
(Clear is Synchronous for MC14163B)



MC14161B, MC14163B TIMING DIAGRAM

Sequence illustrated in waveforms:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit



MOTOROLA

MC14174B

CMOS MSI

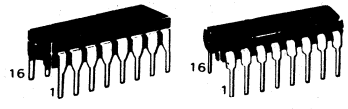
(LOW-POWER COMPLEMENTARY MOS)

HEX TYPE D FLIP-FLOP

HEX TYPE D FLIP-FLOP

The MC14174B hex type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data on the D inputs which meets the setup time requirements is transferred to the Q outputs on the positive edge of the clock pulse. All six flip-flops share common clock and reset inputs. The reset is active low, and independent of the clock.

- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Output Compatible with Two HTL Loads, Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74174

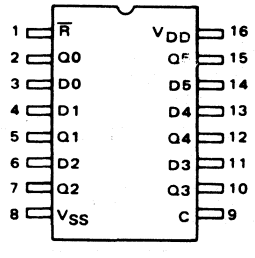


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

3

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

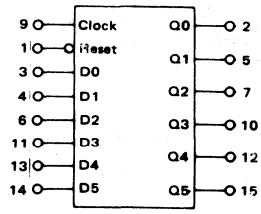
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE
(Postive Logic)

INPUTS			OUTPUT	
Clock	Data	Reset	Q	
↑	0	1	0	
↑	1	1	1	
↓	X	1	Q	No Change
X	X	0	0	

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.1 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.3 μA/kHz) f + I_{DD}							
		15	I_T = (3.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 3 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

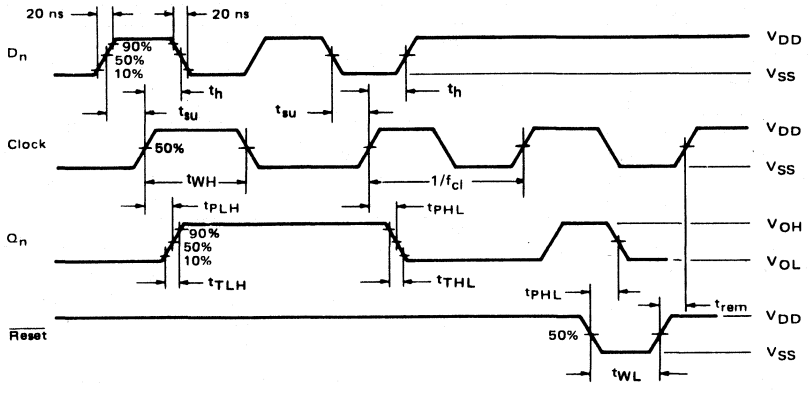
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time – Clock to Q	t_{PLH},					ns
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 165 ns	t_{PHL}	5.0	–	210	400	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 64 ns		10	–	85	160	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 52 ns		15	–	65	120	
Propagation Delay Time – $\overline{\text{Reset}}$ to Q	t_{PHL}					ns
t_{PHL} = (0.9 ns/pF) C_L + 205 ns		5.0	–	250	500	
t_{PHL} = (0.36 ns/pF) C_L + 79 ns		10	–	100	200	
t_{PHL} = (0.26 ns/pF) C_L + 62 ns		15	–	75	150	
Clock Pulse Width	t_{WH}	5.0	150	75	–	ns
		10	90	45	–	
		15	70	35	–	
$\overline{\text{Reset}}$ Pulse Width	t_{WL}	5.0	200	100	–	ns
		10	100	50	–	
		15	80	40	–	
Clock Pulse Frequency	f_{cl}	5.0	–	7.0	2.0	MHz
		10	–	12.0	5.0	
		15	–	15.5	6.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
Data Setup Time	t_{su}	5.0	40	20	–	ns
		10	20	10	–	
		15	15	0	–	
Data Hold Time	t_h	5.0	80	40	–	ns
		10	40	20	–	
		15	30	15	–	
$\overline{\text{Reset}}$ Removal Time**	t_{rem}	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	

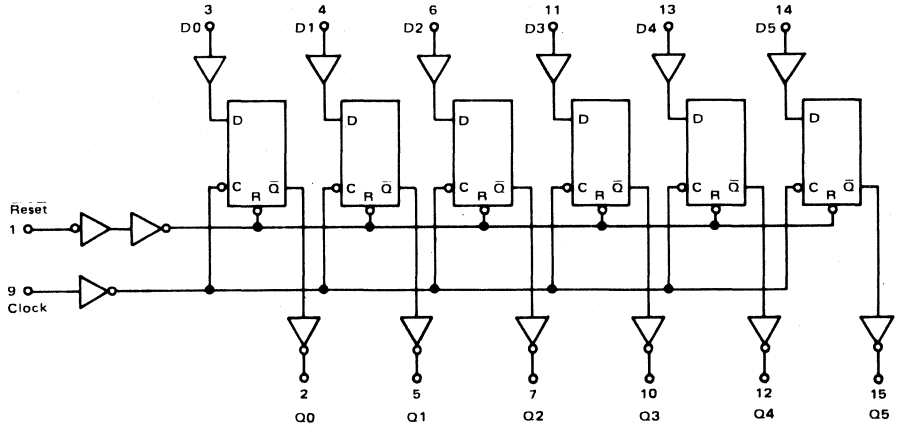
*The formulas given are for the typical characteristics only.
**The reset signal must be high prior to a positive-going transition of the clock.

3

TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



MOTOROLA

MC14175B

CMOS SSI

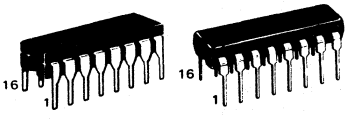
(LOW-POWER COMPLEMENTARY MOS)

QUAD TYPE D FLIP-FLOP

QUAD TYPE D FLIP-FLOP

The MC14175B quad type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each of the four flip-flops is positive-edge triggered by a common clock input (C). An active-low reset input ($\overline{R}$) asynchronously resets all flip-flops. Each flip-flop has independent Data (D) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

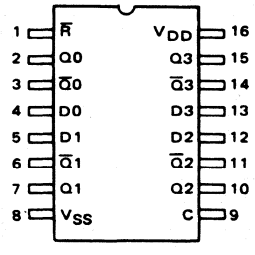
- Complementary Outputs
- Static Operation
- All Inputs and Outputs Buffered
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Output Compatible with Two HTL Loads, Two Low-Power TTL Loads or One Low-Power Schottky TTL Load
- Functional Equivalent to TTL 74175



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

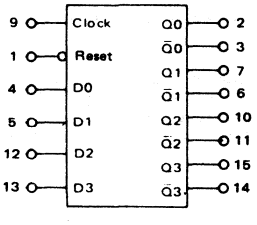
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE
(Postive Logic)

INPUTS			OUTPUTS		
Clock	Data	$\overline{Reset}$	Q	$\overline{Q}$	
↑	0	1	0	1	
↑	1	1	1	0	
↓	X	1	Q	$\overline{Q}$	No Change
X	X	0	0	1	

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.7\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (3.4\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (5.0\ \mu A/kHz)\ f + I_{DD}$							

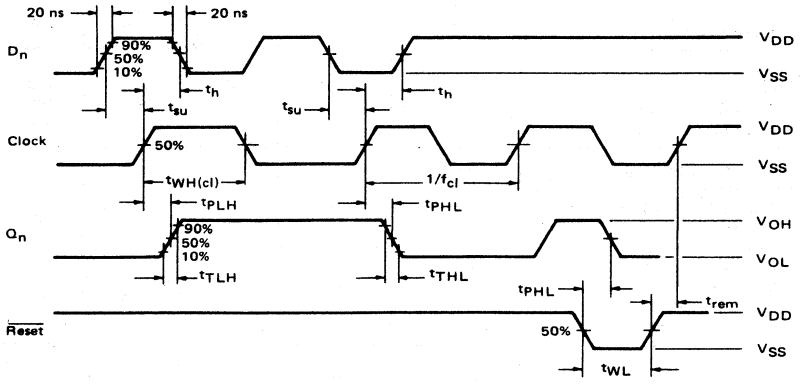
*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

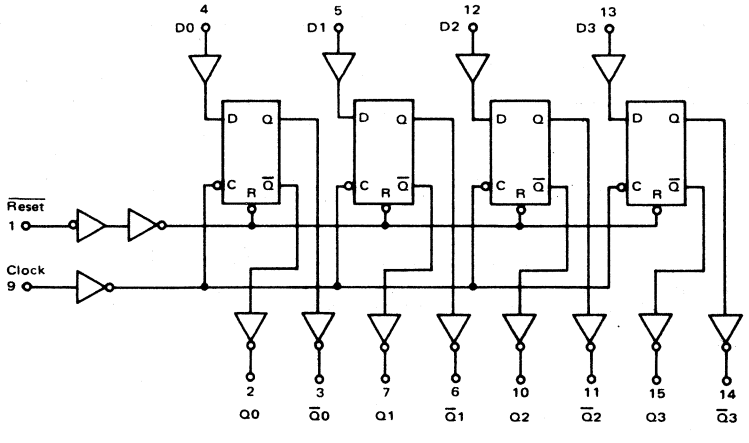
Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns t_{TLH}, t_{THL} = (0.6 ns/pF)C_L + 20 ns t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns	t_{TLH}, t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time – Clock to Q t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 175 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 72 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 57 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	220 90 70	400 160 120	ns
Propagation Delay Time – $\overline{\text{Reset}}$ to Q t_{PHL} = (0.9 ns/pF) C_L + 280 ns t_{PHL} = (0.36 ns/pF) C_L + 112 ns t_{PHL} = (0.26 ns/pF) C_L + 87 ns	t_{PHL}	5.0 10 15	– – –	325 130 100	500 200 150	ns
Clock Pulse Width	t_{WH}	5.0 10 15	250 100 75	110 45 35	– – –	ns
$\overline{\text{Reset}}$ Pulse Width	t_{WL}	5.0 10 15	200 80 60	100 40 30	– – –	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	– – –	4.5 11 14	2.0 5.0 6.5	MHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	– – –	– – –	15 5 4	μs
Data Setup Time	t_{su}	5.0 10 15	120 50 40	60 25 20	– – –	ns
Data Hold Time	t_h	5.0 10 15	80 40 30	40 20 15	– – –	ns
$\overline{\text{Reset}}$ Removal Time**	t_{rem}	5.0 10 15	250 100 80	125 50 40	– – –	ns

*The formulas given are for the typical characteristics only.
**The reset signal must be high prior to a positive-going transition of the clock.

TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



MOTOROLA

MC14194B

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

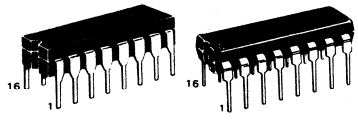
The MC14194B is a 4-bit static shift register capable of operating in the parallel load, serial shift left, serial shift right, or hold mode. The asynchronous $\overline{\text{Reset}}$ input, when at a low level, overrides all other inputs, resets all stages, and forces all outputs low. When $\overline{\text{Reset}}$ is at a logic 1 level, the two mode control inputs, S0 and S1, control the operating mode as shown in the truth table. Both serial and parallel operation are triggered on the positive-going transition of the Clock input. The Parallel Data, Data Shift, and mode control inputs must be stable for the specified setup and hold times before and after the positive-going Clock transition.

- Quiescent Current = 5.0 nA typ/pkg @ 5 Vdc
- Typical Shift Frequency = 9.0 MHz @ 10 Vdc
- Synchronous Right/Left Serial Operation
- Synchronous Parallel Load
- Asynchronous Hold (Do Nothing) Mode
- Functional Pin for Pin Equivalent of 74194

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

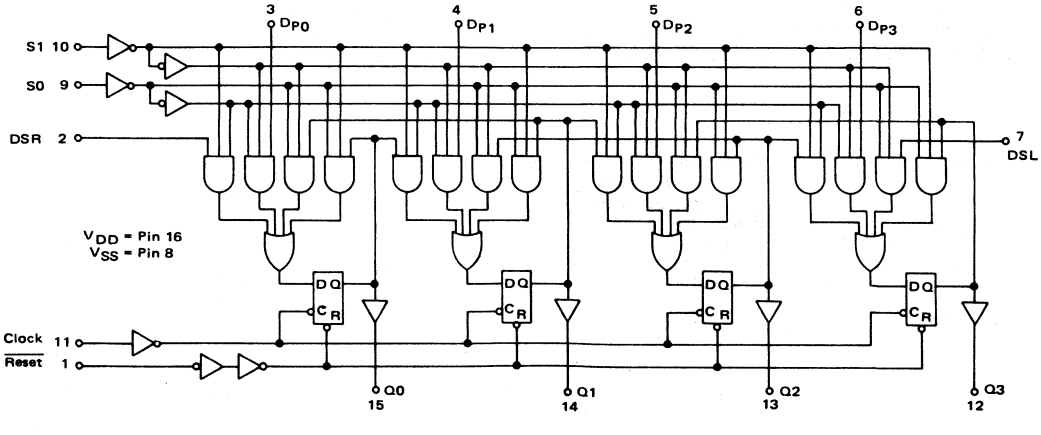
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

TRUTH TABLE

OPERATING MODE	INPUTS ($\overline{\text{Reset}}$ = 1)					OUTPUTS (@ t_{n+1})			
	S1	S0	DSR	DSL	D_{P0-3}	Q0	Q1	Q2	Q3
Hold	0	0	X	X	X	Q0	Q1	Q2	Q3
Shift Left	1	0	X	0	X	Q1	Q2	Q3	0
	1	0	X	1	X	Q1	Q2	Q3	1
Shift Right	0	1	0	X	X	0	Q0	Q1	Q2
	0	1	1	X	X	1	Q0	Q1	Q2
Parallel	1	1	X	X	0	0	0	0	0
	1	1	X	X	1	1	1	1	1

X = Don't Care
t_{n+1} = State after the next positive-going transition of the clock.

LOGIC DIAGRAM

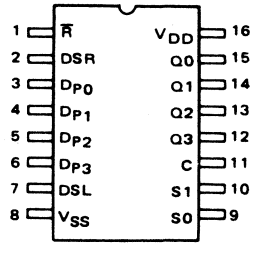


ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	12.0	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.95\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (1.9\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (2.9\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

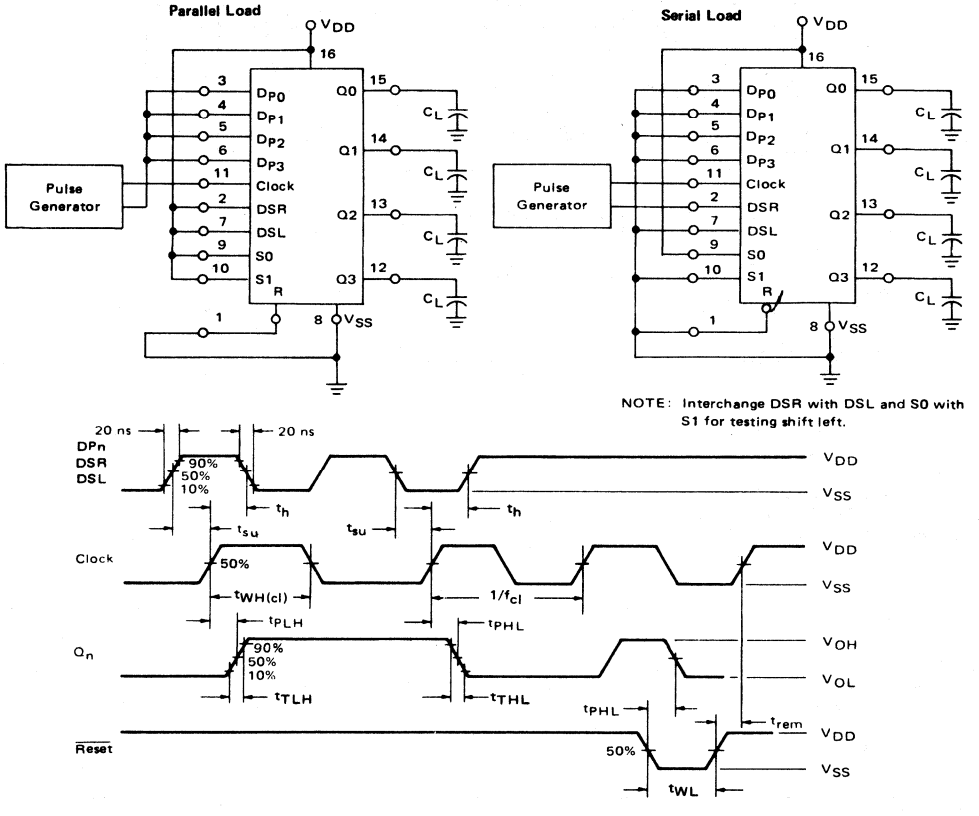
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},t_{PHL}					ns
Clock to Q						
t_{PLH},t_{PHL} = (0.9 ns/pF) C_L + 230 ns		5.0	–	275	550	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 92 ns		10	–	110	220	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 72 ns		15	–	85	170	
$\overline{\text{Reset}}$ to Q	t_{PHL}					ns
t_{PHL} = (0.9 ns/pF) C_L + 305 ns		5.0	–	350	700	
t_{PHL} = (0.36 ns/pF) C_L + 122 ns		10	–	140	280	
t_{PHL} = (0.26 ns/pF) C_L + 97 ns		15	–	110	220	
Clock Pulse Width	t_{WH}	5.0	280	140	–	ns
		10	110	55	–	
		15	85	40	–	
$\overline{\text{Reset}}$ Pulse Width	t_{WH}	5.0	180	90	–	ns
		10	70	35	–	
		15	50	26	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.6	1.8	MHz
(Shift Right or Left Mode)		10	–	9.0	4.5	
		15	–	12	6.0	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0			15	μs
		10			5	
		15			4	
Setup Time	t_{su}					ns
Data to Clock		5.0	10	-8.0	–	
		10	20	0	–	
		15	40	9.0	–	
Mode Control (S) to Clock		5.0	200	100	–	ns
		10	75	36	–	
		15	55	27	–	
Hold Time	t_h					ns
Data to Clock		5.0	180	90	–	
		10	50	25	–	
		15	35	10	–	
Mode Control (S) to Clock		5.0	0	-40	–	ns
		10	0	-27	–	
		15	0	-20	–	
$\overline{\text{Reset}}$ Removal Time**	t_{rem}	5.0	300	150	–	ns
		10	110	55	–	
		15	80	40	–	

*The formulas given are for the typical characteristics only.
**The reset signal must be high prior to a positive-going transition of the clock.

FIGURE 1 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



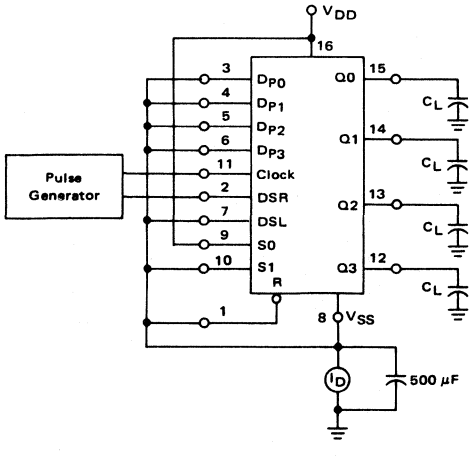
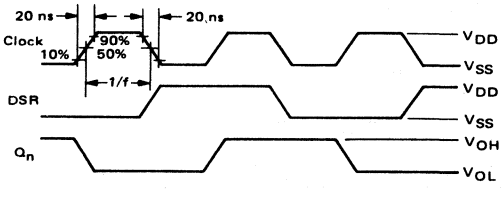


FIGURE 2 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



MOTOROLA

MC14415

QUAD PRECISION TIMER/DRIVER

The MC14415 quad timer/driver is constructed with complementary MOS enhancement mode devices. The output pulse width of each digital timer is a function of the input clock frequency. Once the proper input sequence is detected the output buffer is set (turned on), and after 100 clock pulses are counted, the output buffer is reset (turned off).

The MC14415 was designed specifically for application in high speed line printers to provide the critical timing of the hammer drivers, but may be used in many applications requiring precision pulse widths.

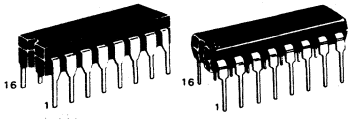
- Four Precision Digital Time Delays
- Schmitt Trigger Clock Conditioning
- NPN Bipolar Output Drivers
- Timing Disable Capability Using Inhibit Output
- Positive or Negative Edge Strobing on the Inputs
- Synchronous Polynomial Counters Used for Delay Counting
- Power Supply Operating Range
  = 3.0 Vdc to 18 Vdc (MC14415EFL/FL/FP)
  = 3.0 Vdc to 6.0 Vdc (MC14415EVL/VL/VP)

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD PRECISION TIMER/DRIVER

3



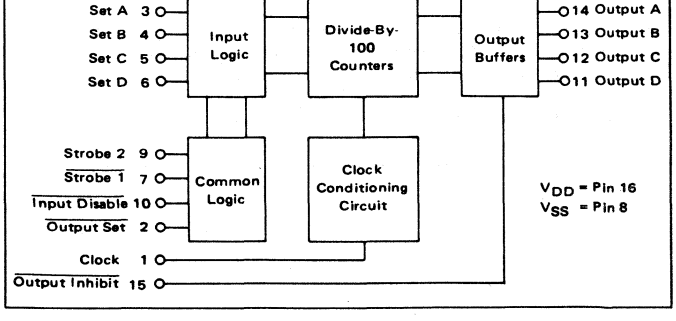
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

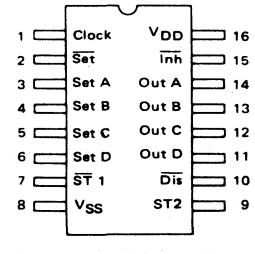
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage – MC14415EFL/FL/FP – MC14415EVL/VL/VP	V_{DD}	 +18 to -0.5 +6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} +0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Input Pin	I_{in}	10	mAdc
DC Current Drain per Output Pin	I_{out}	20	mAdc
Operating Temperature Range – MC14415EFL/EVL – MC14415FL/FP/VL/VP	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

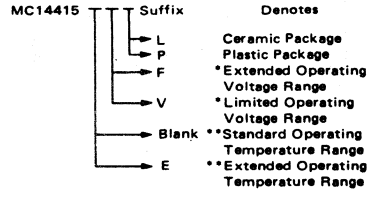
BLOCK DIAGRAM



PIN ASSIGNMENT



ORDERING INFORMATION



*See Features (above, left)
**See Maximum Ratings

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level (No Load)	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	
		15	–	–	–	–	–	–	–	
"1" Level		5.0	–	–	3.0	4.14	–	–	–	Vdc
		10	–	–	8.0	9.09	–	–	–	
		15	–	–	–	14.12	–	–	–	
Noise Immunity	V_{NL}									Vdc
($\Delta V_{out} \leq 1.5$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	
($\Delta V_{out} \leq 3.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	
($\Delta V_{out} \leq 4.5$ Vdc)		15	–	–	–	6.75	–	–	–	
($\Delta V_{out} \leq 1.5$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($\Delta V_{out} \leq 3.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	
($\Delta V_{out} \leq 4.5$ Vdc)		15	–	–	–	6.75	–	–	–	
Output Drive Voltage (NPN Driver)	V_{OH}									Vdc
(I_{OH} = 0 mA) Source		5.0	–	–	3.0	4.14	–	–	–	
(I_{OH} = 5.0 mA)			–	–	2.7	3.44	–	–	–	
(I_{OH} = 10 mA			–	–	2.5	3.30	–	–	–	
(I_{OH} = 15 mA)			–	–	2.2	3.08	–	–	–	
(I_{OH} = 0 mA)		10	–	–	8.0	9.09	–	–	–	Vdc
(I_{OH} = 5.0 mA)			–	–	7.7	8.45	–	–	–	
(I_{OH} = 10 mA)			–	–	7.5	8.30	–	–	–	
(I_{OH} = 15 mA)			–	–	7.1	8.14	–	–	–	
(I_{OH} = 0 mA)		15	–	–	–	14.12	–	–	–	Vdc
(I_{OH} = 5.0 mA)			–	–	–	13.81	–	–	–	
(I_{OH} = 10 mA)			–	–	–	13.70	–	–	–	
(I_{OH} = 15 mA)			–	–	–	13.61	–	–	–	
Output Drive Current	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	–	–	–	7.8	–	–	–	
Input Leakage Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	P_Q									mW
		5.0	–	0.25	–	0.00005	0.25	–	3.5	
		10	–	1.0	–	0.00022	1.0	–	14	
		15	–	–	–	0.00050	–	–	–	
Power Dissipation** (Dynamic plus Quiescent) (C_L = 15 pF)	P_D									mW
		5.0	$P_D = (56 \text{ mW/MHz}) f + P_Q$							
		10	$P_D = (225 \text{ mW/MHz}) f + P_Q$							
		15	$P_D = (510 \text{ mW/MHz}) f + P_Q$							

*T_{low} = -55°C for MC14415EFL, EVL; -40°C for MC14415FL,FP,VL,VP
T_{high} = +125°C for MC14415EFL,EVL; +85°C for MC14415FL,FP,VL,VP

** The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS (C_L = 15 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time*	t_{TLH}					ns
t_{TLH} = (2.0 ns/pF) C_L + 10 ns		5.0	–	40	85	
t_{TLH} = (1.25 ns/pF) C_L + 6 ns		10	–	25	60	
t_{TLH} = (1.10 ns/pF) C_L + 3 ns		15	–	20	–	
Output Fall Time*	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 47 ns		5.0	–	70	150	
t_{THL} = (0.75 ns/pF) C_L + 24 ns		10	–	35	80	
t_{THL} = (0.55 ns/pF) C_L + 17 ns		15	–	25	–	
Turn-Off Delay Time*	t_{PLH}					ns
t_{PLH} = (2.7 ns/pF) C_L + 560 ns		5.0	–	600	1200	
t_{PHL} = (1.2 ns/pF) C_L + 282 ns		10	–	300	600	
t_{PLH} = (0.91 ns/pF) C_L + 286 ns		15	–	150	–	
Turn-On Delay Time*	t_{PHL}					ns
t_{PHL} = (2.4 ns/pF) C_L + 564 ns		5.0	–	600	1200	
t_{PHL} = (1.0 ns/pF) C_L + 285 ns		10	–	300	600	
t_{PHL} = (0.75 ns/pF) C_L + 289 ns		15	–	150	–	
Turn-On Delay Time ($\overline{\text{Inhibit}}$ to Output)	t_{PHL}					ns
		5.0	–	300	550	
		10	–	225	425	
		15	–	110	–	
Turn-Off Delay Time ($\overline{\text{Inhibit}}$ to Output)	t_{PLH}					ns
		5.0	–	300	550	
		10	–	225	425	
		15	–	110	–	
Input Pulse Coincidence (Figure 3)	PC_{min}					ns
		5.0	500	450	–	
		10	450	350	–	
		15	–	–	–	
Input Pulse Width (Figure 1)	t_{WH}					ns
		5.0	500	450	–	
		10	450	350	–	
		15	–	–	–	
Input Clock Frequency	f_{cl}					MHz
		5.0	–	0.7	–	
		10	–	1.0	–	
		15	–	1.5	–	
Clock Input Rise and Fall Times (Figure 1)	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5.0	
		15	–	–	4.0	

*The formulae given are for the typical characteristics only.

FIGURE 1 – SWITCHING CHARACTERISTICS – WAVEFORM RELATIONSHIPS

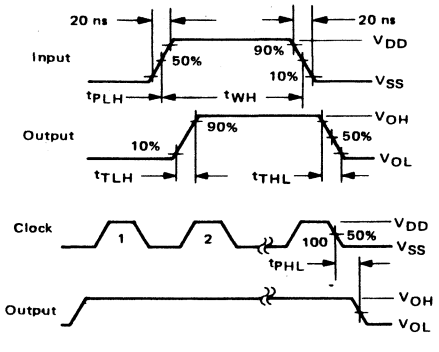


FIGURE 2 – AMBIENT TEMPERATURE POWER DERATING

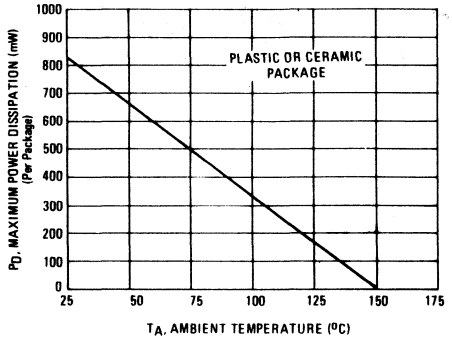
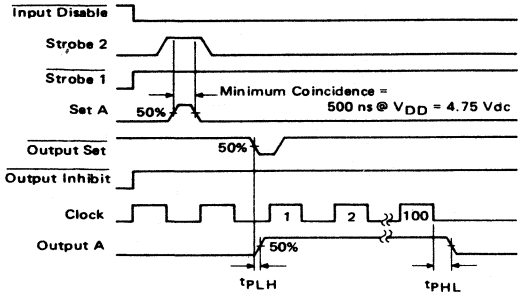
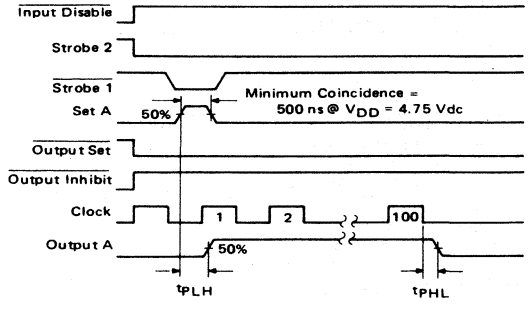


FIGURE 3 – TYPICAL OPERATION MODES AND FUNCTIONAL TIMING DIAGRAM

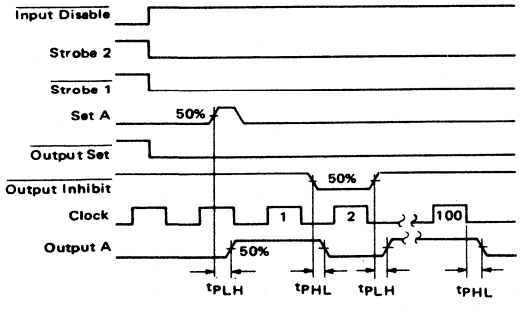
MODE 1 – $\overline{\text{OUTPUT SET}}$ INITIATES TIME DELAY



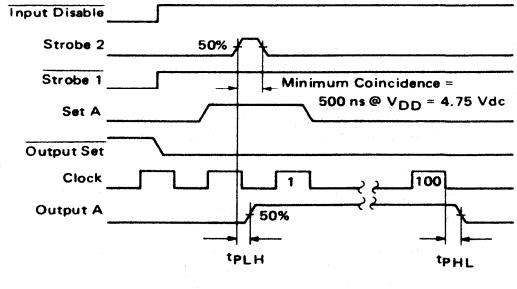
MODE 2 : SET A INITIATES TIME DELAY



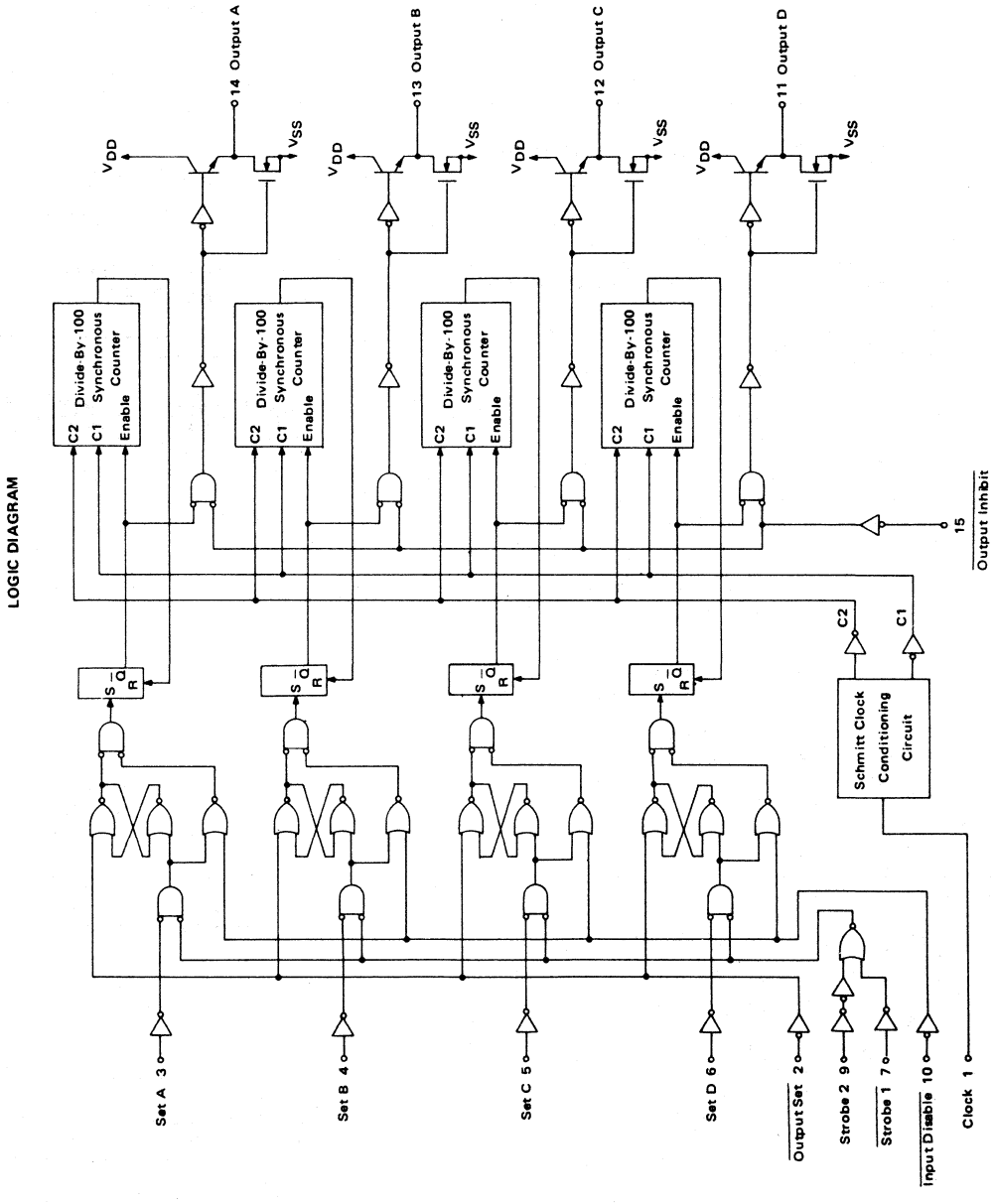
MODE 3: $\overline{\text{OUTPUT INHIBIT}}$ DISABLES TIME DELAY



MODE 4: POSITIVE-EDGE STROBE (ST2) INITIATES TIME DELAY



LOGIC DIAGRAM



MOTOROLA

MC14419

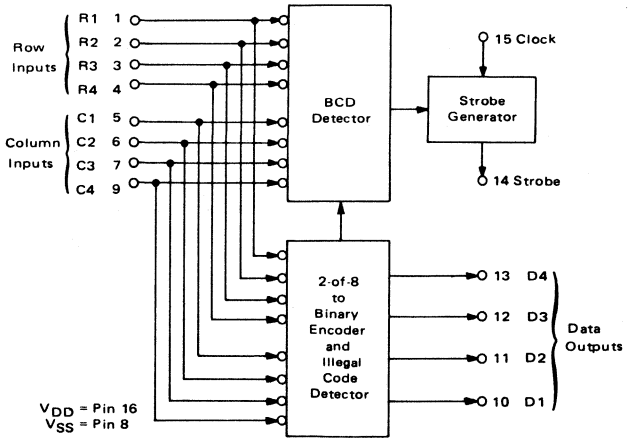
2-OF-8 KEYPAD-TO-BINARY ENCODER

The MC14419 is designed for phone dialer system applications, but finds many applications as a keypad-to-binary encoder. The device contains a 2-of-8 to binary encoder, a strobe generator, and an illegal state detector. The encoder has four row inputs and four column inputs, and is designed to accept inputs from 16 keyswitches arranged in a 4 x 4 matrix. For an output on the four data lines, one and only one row along with one and only one column input line must be activated. All other combinations are suppressed by the illegal state detector to eliminate false data output.

The strobe generator produces a strobe pulse when any of the 10 keys corresponding to numerals 0 through 9 are depressed. The strobe output can be used to eliminate erroneous data entry due to contact bounce. For a strobe output to occur, the key row and column input lines must remain stable for 80 clock pulses after activation. When the contact bounce has settled and 80 clock pulses have occurred, the output will be a single strobe pulse equal in width to that of the clock low state. The strobe generator will output one and only one pulse each time a numerical key is depressed. After the pulse has occurred, noise and bounce due to contact break will not cause another strobe pulse. With a 16 kHz input clock frequency, the pulse occurs 5 ms after the last bounce.

- Suppressed Output for Illegal Input Codes
- On-Chip Pullup Resistors for Row and Column Inputs
- Clock Input Conditioning Circuit
- Low Current Drain in Standby Mode
  5.0 μA Typical @ 5.0 Vdc
- Subsystem Complement to the MC14408/14409 Phone Pulse Converter
- One-Key Rollover Feature

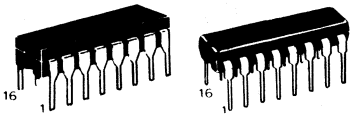
BLOCK DIAGRAM



CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

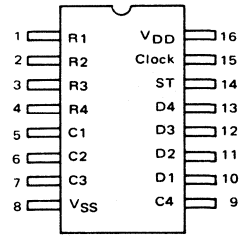
2-OF-8 KEYPAD-TO-BINARY ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



VDD = Pin 16
VSS = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{ss} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8.)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+6.0 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	-40°C Min	-40°C Max	25°C Min	25°C Typ	25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage Operating Range	V_{DD}	–	3.0	6.0	3.0	5.0	6.0	3.0	6.0	Vdc
Output Voltage "0" Level	V_{out}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	1.5	–	1.5	2.25	–	1.4	–	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.25	–	3.6	–	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.23	–	-0.20	-1.7	–	-0.16	–	mAdc
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.23	–	0.20	0.78	–	0.16	–	mAdc
Input Leakage Current (V_{in} = V_{DD})	I_{IH}	5.0	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Pullup Resistor Source Current (Row and Column Inputs) (V_{in} = V_{SS})	I_{IL}	5.0	265	460	190	250	330	125	215	μAdc
Input Capacitance (V_{in} = V_{SS})	C_{in}	–	–	–	–	5.0	–	–	–	pF
Standby Supply Current	I_{DDS}	3.0	–	3.0	–	1.0	3.0	–	6.0	μAdc
(f_{clock} = 16 kHz, No Keys Depressed)		5.0	–	15	–	5.0	15	–	30	
		6.0	–	60	–	20	60	–	120	
Standby Supply Current as a Function of Clock Frequency* (No Keys Depressed)	I_{DDS}	5.0	I_{DDS} = 0.09 μA/kHz + 3.0 μA							μAdc

*The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise and Fall Times, D1 thru D4 (Figure 1)	t_{TLH}, t_{THL}	5.0	–	300	–	ns
Propagation Delay Time, Row or Column Input to Data Output (Figure 1)	t_{PLH}, t_{PHL}	5.0	–	1000	–	ns
Clock Pulse Frequency Range	PRF	3.0 to 6.0	–	–	80	kHz

FIGURE 1 – SWITCHING TIME WAVEFORMS

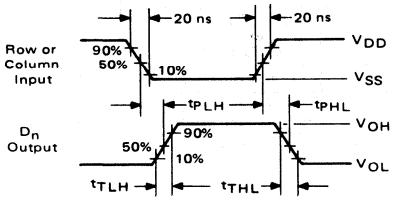


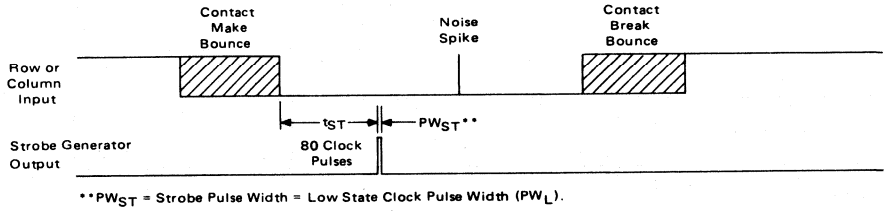
FIGURE 2 – TYPICAL STROBE PULSE DELAY TIMES

PRF Clock Frequency kHz	t_{ST}* Strobe Pulse Delay Time ms
4.0	20
8.0	10
16	5.0
32	2.5
80	1.0

*t_{ST} = (1/PRF) • 80, with PRF in kHz, t_{ST} in ms.

3

FIGURE 3 – STROBE GENERATOR TIMING DIAGRAM



**PW_{ST} = Strobe Pulse Width = Low State Clock Pulse Width (PW_L).

TRUTH TABLE

	Inputs								Outputs				
	Row				Column								
Key**	R4	R3	R2	R1	C4	C3	C2	C1	D4	D3	D2	D1	Strobe
1	1	1	1	0	1	1	1	0	0	0	0	1	⎍
2	1	1	1	0	1	1	0	1	0	0	1	0	⎍
3	1	1	1	0	1	0	1	1	0	0	1	1	⎍
A	1	1	1	0	0	1	1	1	1	1	0	0	0
4	1	1	0	1	1	1	1	0	0	1	0	0	⎍
5	1	1	0	1	1	1	0	1	0	1	0	1	⎍
6	1	1	0	1	1	0	1	1	0	1	1	0	⎍
B	1	1	0	1	0	1	1	1	1	1	0	1	0
7	1	0	1	1	1	1	1	0	0	1	1	1	⎍
8	1	0	1	1	1	1	0	1	1	0	0	0	⎍
9	1	0	1	1	1	0	1	1	1	0	0	1	⎍
C	1	0	1	1	0	1	1	1	1	1	1	0	0
*	0	1	1	1	1	1	1	0	1	0	1	0	0
0	0	1	1	1	1	1	0	1	0	0	0	0	⎍
#	0	1	1	1	1	0	1	1	1	0	1	1	0
D	0	1	1	1	0	1	1	1	1	1	1	1	0
	All Other Combinations								0	0	0	0	0

**See Figure 4 for keypad designation.

FIGURE 4 – TYPICAL KEYPAD INTERFACE APPLICATION

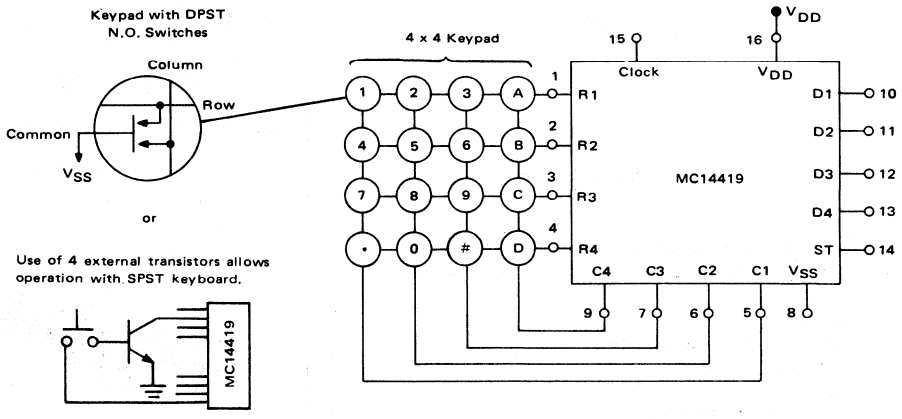
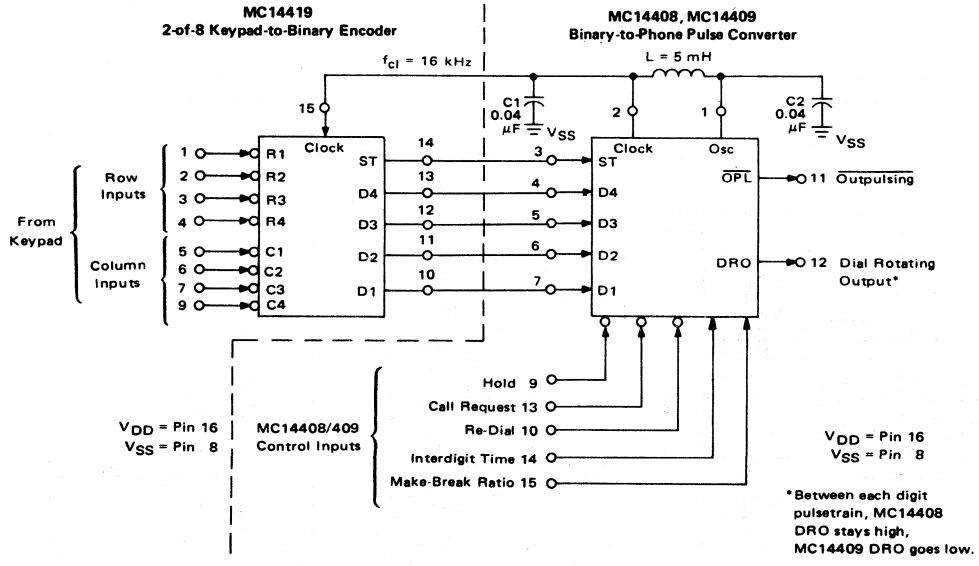


FIGURE 5 – PHONE DIALER SYSTEM



MOTOROLA

MC14430

CMOS MSI

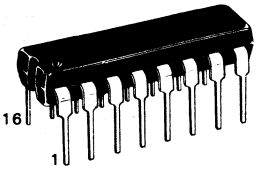
(LOW POWER COMPLEMENTARY MOS)

INPUT ADDRESS ENCODER

INPUT ADDRESS ENCODER

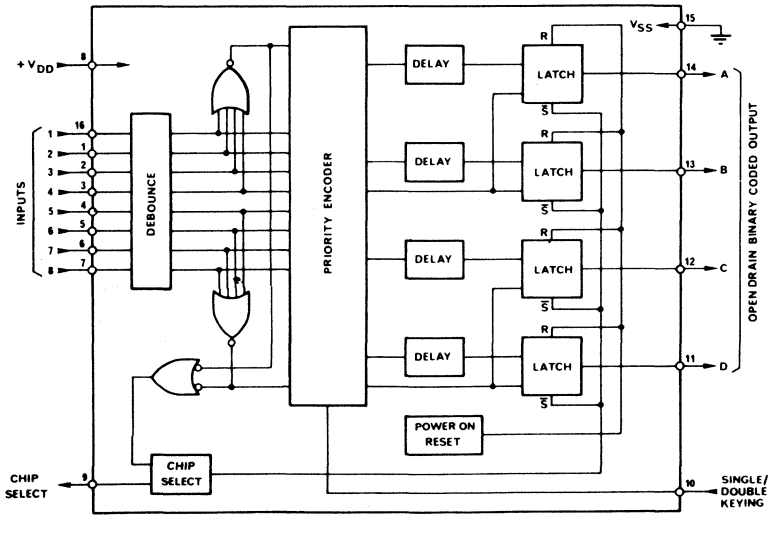
The MC14430 is an integrated circuit designed for program selection address in TV and radio receivers by means of push button switches.

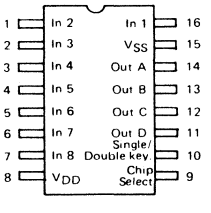
- 8 program inputs
- Binary coded open drain latched output
- Push button type keyboard allows for electrical isolation in live chassis applications
- Single or double keying operation possible
- Up to four circuits can be cascaded
- Normally closed or normally open switches can be used.



P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 – MC14430 BLOCK DIAGRAM & PIN-OUT





E-049 – May 1979

MAXIMUM RATINGS (T_A = 25 °C)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+10 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

3

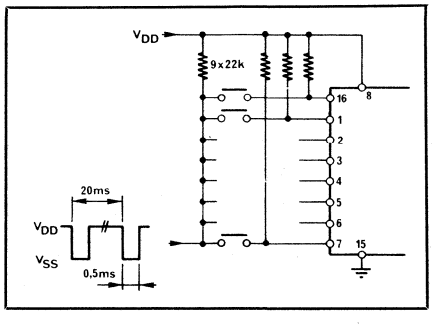
ELECTRICAL CHARACTERISTICS (T_A = 0 to 70 °C)

Characteristics		Symbol	Min.	Typ.	Max.	Unit
Operating Supply Voltage		V_{DD}	4	5.2	6	Vdc
Quiescent Current per Package (Pins 16,1,2, 3,4,5,6,7 open or grounded)	V_{DD} = 5 V	I_{DD}	–	0.068	10	μAdc
Input Voltage	"O" Level "I" Level	V_{IL} V_{IH}	– 3.5	2.25 2.75	1.5 –	Vdc
Input Current	V_{DD} = 5 V V_{in} = 1 V V_{in} = 2 V V_{in} = 5 V	I_{in}	 – – –	 2.1 2.6 2.6	 – – 6.0	μAdc
Output Drive Current (V_{OL} = 0.5 V)	V_{DD} = 5 V	I_{OL}	2.5	6.2	–	mAdc
Output Drive Current (V_{OL} = 0.5 V)	V_{DD} = 5 V	I_{OL}	0.9	2.25	–	mAdc

APPLICATION INFORMATION

Incorrect encoding of the selected program number can occur whenever the last bounce, on opening a normally open switch, is 40 to 60 μsec. wide. Should the type of switch used have a characteristic within this timing, the switch configuration opposite is recommended.
By pulsing the common switch line at a rate lower than the whole bounce period (15 msec. max.), chances of misfunction are reduced.
Pulsing can be provided by a unijunction transistor relaxation oscillator or by a switching transistor driven by the vertical deflection flyback signal or others. The pulse width can vary between few hundred μsec. and few milliseconds.

FIGURE 2 – BOUNCE IMMUNE APPLICATION



APPLICATION INFORMATION

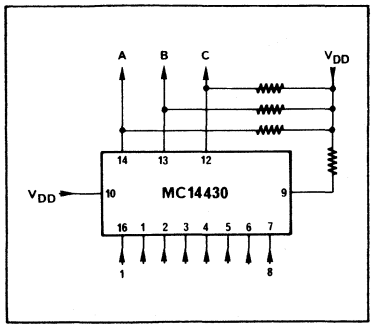


FIGURE 3 – 8 CHANNELS SINGLE KEYING

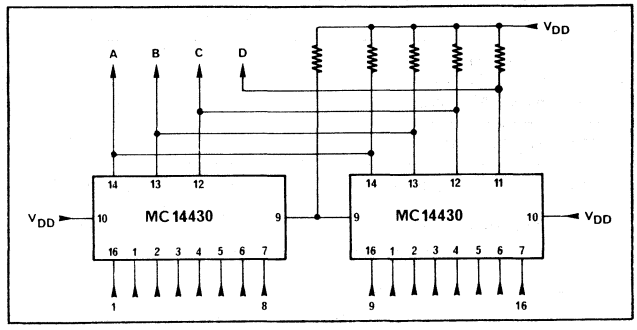


FIGURE 4 – 16 CHANNELS SINGLE KEYING

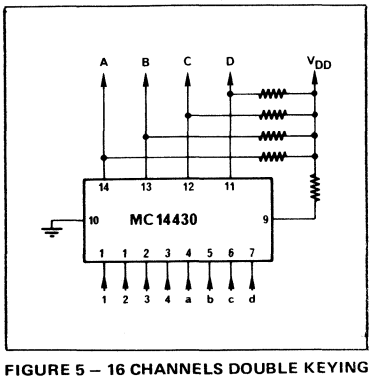


FIGURE 5 – 16 CHANNELS DOUBLE KEYING

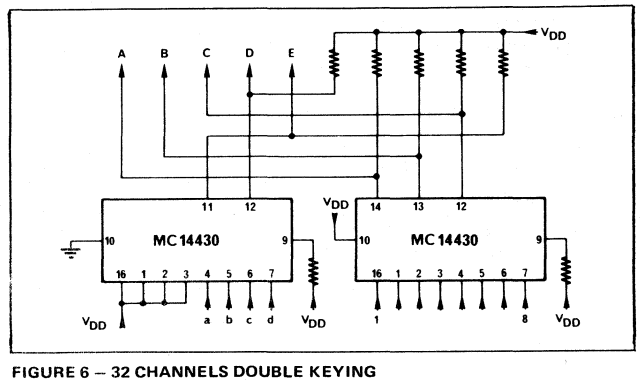


FIGURE 6 – 32 CHANNELS DOUBLE KEYING

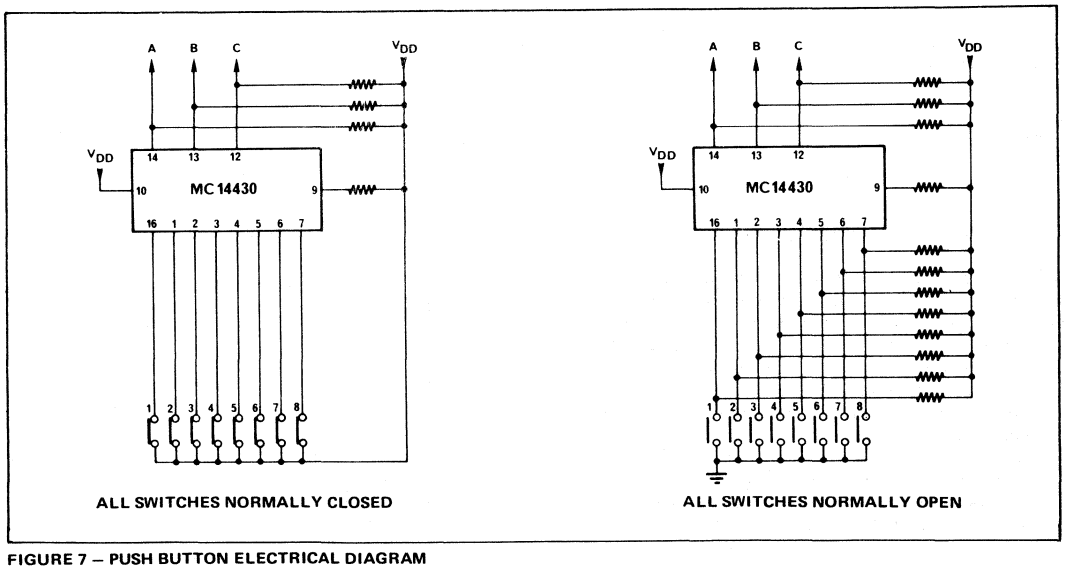


FIGURE 7 – PUSH BUTTON ELECTRICAL DIAGRAM

INPUT/OUTPUT FUNCTIONS

SINGLE/DOUBLE KEYING – Single Keying Mode (SKM) is selected by connecting pin 10 to V_{DD}. Double Keying Mode (DKM) is obtained by connecting pin 10 to ground.
In SKM, input pins: 16, 1, 2, 3, 4, 5, 6, 7 select programs 1 to 8 respectively. The corresponding binary coded output (000 for program 1) will appear on lines A, B, C. Output D (pin 11) is a chip select output and will remain activated (at V_{SS}) as long as the chip is selected. Refer to application information.
In DKM, keys are divided into two groups: keys 1, 2, 3, 4 (pin 16, 1, 2, 3) and keys a, b, c, d, (pin 4, 5, 6, 7) which affect output lines A, B, and C, D respectively (see application information).
Keying sequence is important since output lines A and B are reset every time a, b, c, d are actuated.
For example: program b3 is selected by keying b first, then 3. If key d is then actuated, program d1 is selected.

POWER ON RESET – When power is switched on, channel 1 (or channel 1a in DKM) will be automatically selected.

PRIORITY ENCODER – When two or more keys belonging to the same chip are activated simultaneously, the key having the lowest number will have priority and the corresponding code will be selected.
In Double Keying Mode, key 1 has priority over keys 2,3 and 4, key a has priority over keys b, c and d.

MULTI CHIP SYSTEM – As long as one key is activated the chip select pin 9 of the corresponding chip is pulled to ground.
That chip is now selected and any other chip connected in parallel will be disabled.
If two or more keys belonging to different chips are acutated at the same time, the chip corresponding to the first actuated key will be selected. When releasing the keys, the chip corresponding to the last released key will remain selected.

BINARY CODED OUTPUT – In SKM, binary coded program number minus one is present on lines A, B, C (pin 14, 13, 12).
Output D (pin 11) goes low when the corresponding chip is selected. In DKM the binary code output is present on lines A, B, C, D.

MOTOROLA

MC14501UB

CMOS SSI

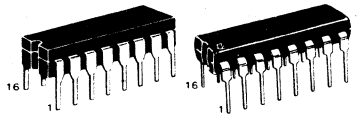
(LOW-POWER COMPLEMENTARY MOS)

TRIPLE GATE
DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE

TRIPLE GATE
DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE

The MC14501UB constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

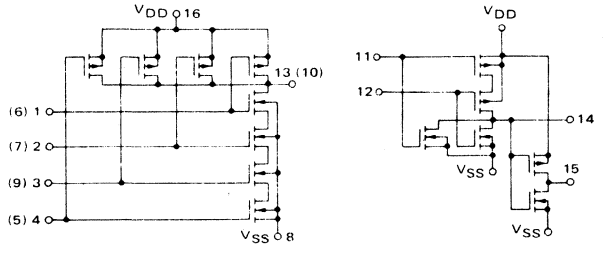
ORDERING INFORMATION

MC14XXXUB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

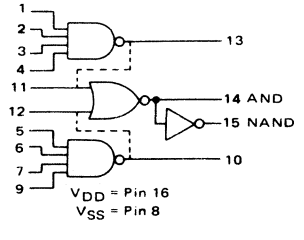
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



Numbers in parenthesis are for second 4-input gate.

LOGIC DIAGRAM
(POSITIVE LOGIC)



Use Dotted Connection Externally to Obtain 8-Input AND/NAND

Note: Pin 14 must not be used as an input to the inverter.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.4	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.6	
(V_O = 1.4 or 3.6 Vdc) "1" Level	V_{IH}	5.0	3.6	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.1	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	–	11.25	8.25	–	11.0	–	
Output Drive Current	I_{OH}									mAdc
(AL Device)										
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
(V_{OH} = 9.5 Vdc) NAND		10	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OH} = 13.5 Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OH} = 2.5 Vdc) NOR		5.0	−2.1	–	−1.75	−3.0	–	−1.22	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.42	–	−0.35	−0.63	–	−0.24	–	
(V_{OH} = 9.5 Vdc)		10	−1.06	–	−0.88	−1.58	–	−0.62	–	
(V_{OH} = 13.5 Vdc)		15	−3.1	–	−2.63	−6.12	–	−1.84	–	
(V_{OH} = 2.5 Vdc) NOR-		5.0	−3.6	–	−3.0	−5.1	–	−2.1	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.72	–	−0.6	−1.08	–	−0.42	–	
(V_{OH} = 9.5 Vdc) Inverter		10	−1.8	–	−1.5	−2.7	–	−1.05	–	
(V_{OH} = 13.5 Vdc)		15	−5.4	–	−4.5	−10.5	–	−3.15	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc) NAND		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
(V_{OL} = 0.4 Vdc) NOR		5.0	0.92	–	0.77	1.32	–	0.54	–	mAdc
(V_{OL} = 0.5 Vdc)		10	2.34	–	1.95	3.37	–	1.36	–	
(V_{OL} = 1.5 Vdc)		15	6.12	–	5.1	13.2	–	3.57	–	
(V_{OL} = 0.4 Vdc) NOR-		5.0	1.54	–	1.28	2.2	–	0.90	–	mAdc
(V_{OL} = 0.5 Vdc) Inverter		10	3.90	–	3.25	5.63	–	2.27	–	
(V_{OL} = 1.5 Vdc)		15	10.2	–	8.5	22	–	5.95	–	
Output Drive Current	I_{OH}									mAdc
(CL/CP Device)										
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	−0.8	−1.7	–	−0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.2	–	−0.16	−0.36	–	−0.12	–	
(V_{OH} = 9.5 Vdc) NAND		10	−0.5	–	−0.4	−0.9	–	−0.3	–	
(V_{OH} = 13.5 Vdc)		15	−1.4	–	−1.2	−3.5	–	−1.0	–	
(V_{OH} = 2.5 Vdc) NOR		5.0	−1.68	–	−1.4	−3.0	–	−1.05	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.34	–	−0.28	−0.63	–	−0.21	–	
(V_{OH} = 9.5 Vdc)		10	−0.84	–	−0.7	−1.58	–	−0.52	–	
(V_{OH} = 13.5 Vdc)		15	−2.52	–	−2.1	−6.12	–	−1.57	–	
(V_{OH} = 2.5 Vdc) NOR-		5.0	−2.88	–	−2.4	−5.1	–	−1.8	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.58	–	−0.48	−1.08	–	−0.36	–	
(V_{OH} = 9.5 Vdc) Inverter		10	−1.44	–	−1.2	−2.7	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.32	–	−3.6	−10.5	–	−2.7	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc) NAND		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
(V_{OL} = 0.4 Vdc) NOR		5.0	0.79	–	0.66	1.32	–	0.54	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.98	–	1.65	3.37	–	1.36	–	
(V_{OL} = 1.5 Vdc)		15	5.4	–	4.5	13.2	–	3.57	–	
(V_{OL} = 0.4 Vdc) NOR-		5.0	1.32	–	1.1	2.2	–	0.90	–	mAdc
(V_{OL} = 0.5 Vdc) Inverter		10	3.3	–	2.75	5.63	–	2.27	–	
(V_{OL} = 1.5 Vdc)		15	9.0	–	7.5	22.0	–	5.95	–	

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.2\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (2.4\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.6\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

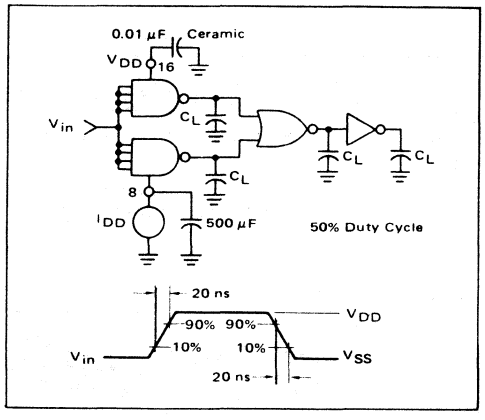
SWITCHING CHARACTERISTICS** (C_L = 50 pF, T_A = 25°C)

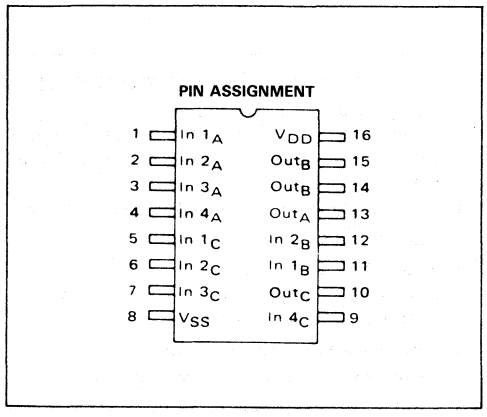
Characteristic		Figure	Symbol	V_{DD}	Typ All Types	Max	Unit
Output Rise Time	NAND, NOR	2, 3	t_{TLH}				ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns				5.0	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns				10	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns				15	65	130	
Output Fall Time	NAND, NOR	2, 3	t_{THL}				ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns				5.0	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns				10	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns				15	40	80	
Output Rise Time	NOR-Inverter	3	t_{TLH}				ns
t_{TLH} = (1.35 ns/pF) C_L + 32.5 ns				5.0	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns				10	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 17 ns				15	40	80	
Output Fall Time	NOR-Inverter	3	t_{THL}				ns
t_{THL} = (0.67 ns/pF) C_L + 26.5 ns				5.0	60	120	
t_{THL} = (0.45 ns/pF) C_L + 17.5 ns				10	40	80	
t_{THL} = (0.37 ns/pF) C_L + 11.5 ns				15	30	60	
Propagation Delay Time	NAND	2	t_{PLH}, t_{PHL}				ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 45 ns				50	130	260	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 37 ns				10	70	140	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns				15	50	100	
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns	NOR	3	t_{PLH}, t_{PHL}	5.0	115	230	ns
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 32 ns				10	65	130	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 20 ns				15	45	90	
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 45 ns	NOR-Inverter	3	t_{PLH}, t_{PHL}	5.0	130	260	ns
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 37 ns				10	70	140	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns				15	50	100	

** The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM





3

FIGURE 2 – 4-INPUT "NAND" GATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

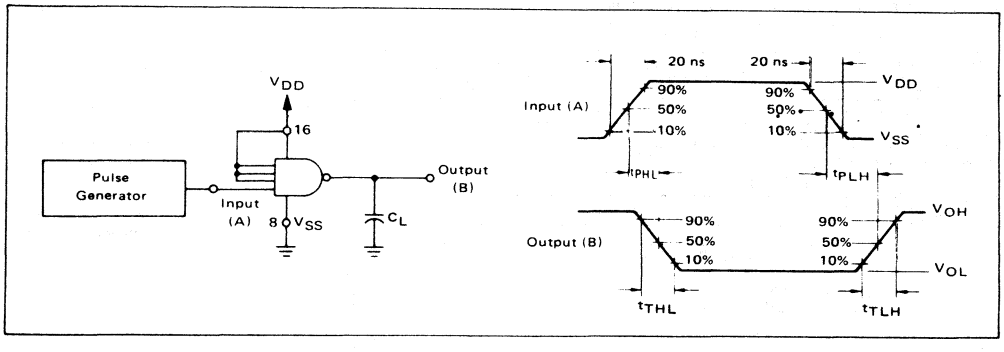
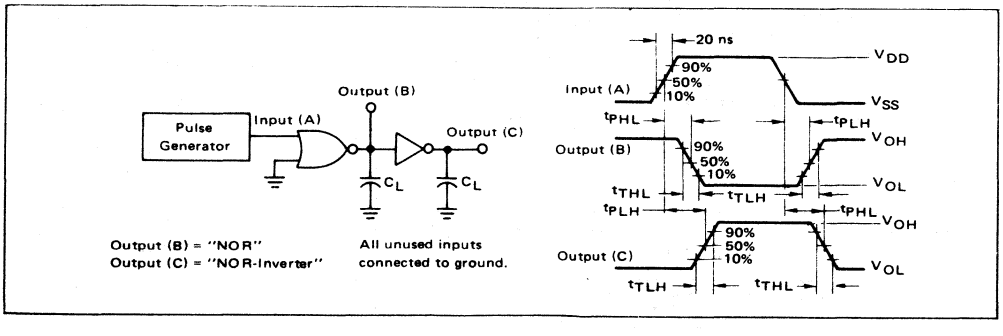


FIGURE 3 – "NOR" GATE and "NOR-INVERTER" SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MOTOROLA

MC14502B

STROBED HEX INVERTER/BUFFER

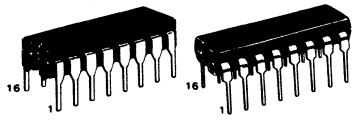
The MC14502B is a strobed hex buffer/inverter with 3-state output, an inhibit control, and guaranteed TTL drive over the temperature range. The 3-state output simplifies design by allowing a common bus.

- Quiescent Current = 2.0 nA/package typical @ 5 Vdc
- Separate Output Disable Control
- 3-State Output
- Output Impedance = 200 ohms @ 5.0 V Supply Guaranteed Over Full Temperature Range
- Input Impedance = 10^{12} ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

STROBED HEX INVERTER/BUFFER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

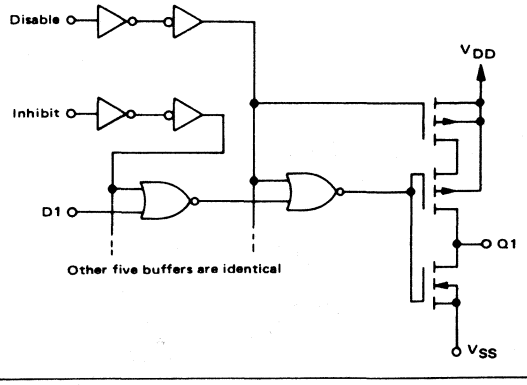
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

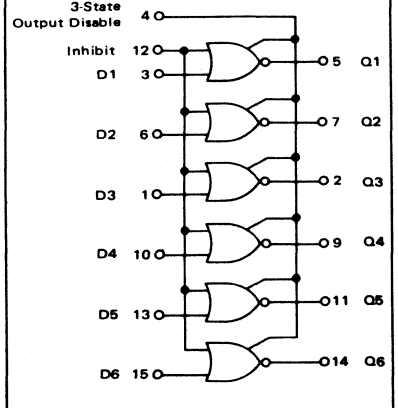
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	30	mAdc
Operating Temperature Range — AL Device	T_A	−55 to +125	°C
CL/CP Device		−40 to +85	
Storage Temperature Range	T_{stg}	−65 to +150	°C

CIRCUIT DIAGRAM



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

D_n	Inhibit	Disable	Q_n
0	0	0	1
1	0	0	0
X	1	0	0
X	X	1	High Impedance

X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	3.5	–	2.8	6.6	–	2.0	–	mAdc
(V_{OL} = 0.5 Vdc)		10	7.8	–	6.3	17	–	4.4	–	
(V_{OL} = 1.5 Vdc)		15	29	–	24	66	–	16	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	2.3	–	1.9	6.6	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	5.0	–	4.2	17	–	3.4	–	
(V_{OL} = 1.5 Vdc)		15	19	–	16	66	–	13	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (2.7 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (5.3 μA/kHz) f + I_{DD}							
		15	I_T = (8.0 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

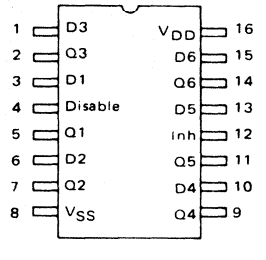
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (0.6 ns/pF) C_L + 10 ns		5.0	–	40	80	
t_{THL} = (0.3 ns/pF) C_L + 5.0 ns		10	–	20	40	
t_{THL} = (0.27 ns/pF) C_L + 1.5 ns		15	–	15	30	
Propagation Delay Time Data to Q	t_{PHL}	5.0	–	135	270	ns
		10	–	55	110	
		15	–	40	80	
Propagation Delay Time, Inhibit to Q	t_{PHL}	5.0	–	335	670	ns
		10	–	145	290	
		15	–	95	190	
Propagation Delay Time Data to Q, Inhibit to Q	t_{PLH}	5.0	–	295	590	ns
		10	–	130	260	
		15	–	95	190	
3-State Propagation Delay, Output "1" to High Impedance	t_{PHZ}	5.0	–	65	130	ns
		10	–	30	60	
		15	–	25	50	
3-State Propagation Delay, High Impedance to "1" Level	t_{PZH}	5.0	–	260	520	ns
		10	–	105	210	
		15	–	80	160	
3–State Propagation Delay, Output "0" to High Impedance	t_{PLZ}	5.0	–	150	300	ns
		10	–	70	140	
		15	–	55	110	
3-State Propagation Delay, High Impedance to "0" Level	t_{PZL}	5.0	–	160	320	ns
		10	–	65	130	
		15	–	50	100	

*The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT TEST CIRCUIT (I_{OH})

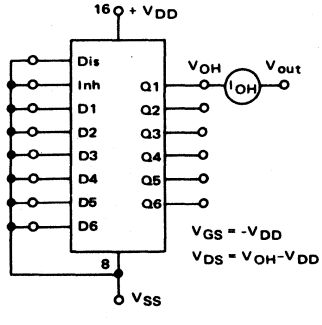


FIGURE 2 – TYPICAL OUTPUT SINK CURRENT TEST CIRCUIT (I_{OL})

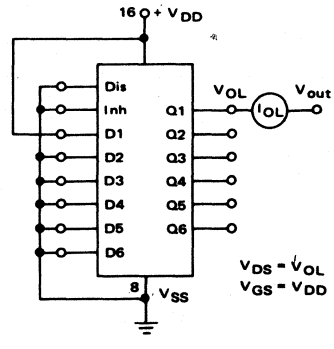


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

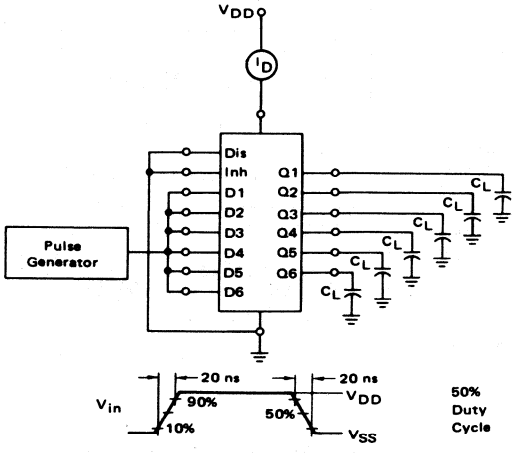


FIGURE 4 – AMBIENT TEMPERATURE POWER DERATING

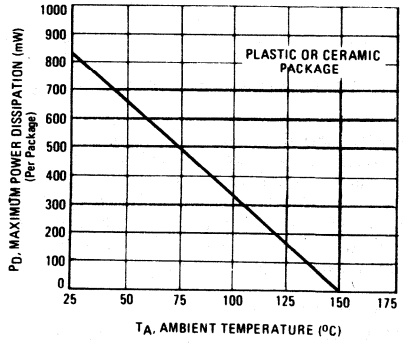
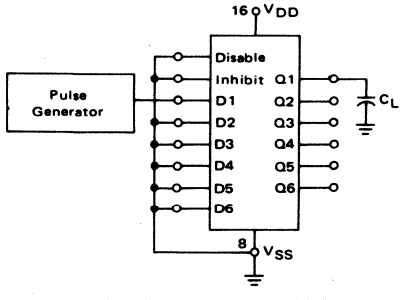


FIGURE 5 – AC TEST CIRCUIT AND WAVEFORMS (t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH})



For all t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH} measurements V_{in} may be applied to any other D_n input or to Inhibit.

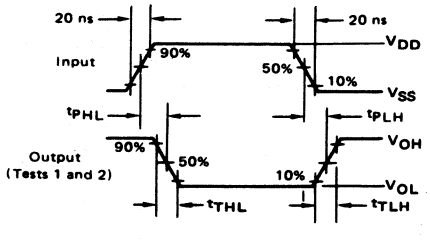
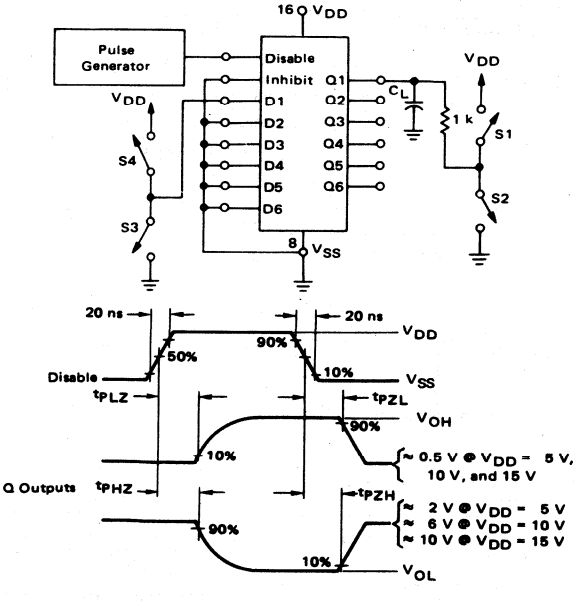


FIGURE 6 – 3-STATE AC TEST CIRCUIT AND WAVEFORMS (t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL})

Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open



MOTOROLA

MC14503B

HEX NON-INVERTING 3-STATE BUFFER

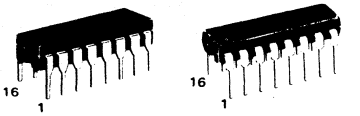
The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

- 3-State Outputs
- TTL Compatible — Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Symmetrical Turn-On and Turn-off Delays
- Symmetrical Output Rise and Fall Times
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX 3-STATE BUFFER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

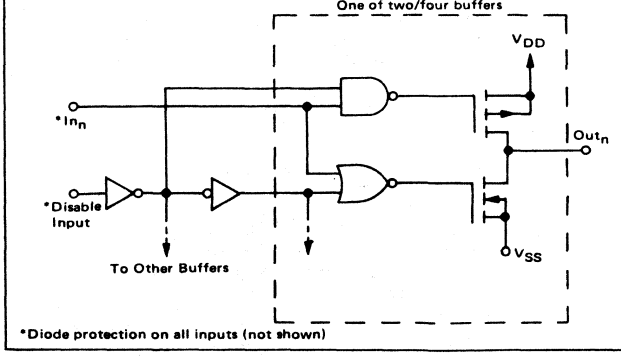
MC14XXXB — Suffix

Suffix	Denotes
L	Ceramic Package
P	Plastic Package
A	Extended Operating Temperature Range
C	Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	25	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

CIRCUIT DIAGRAM



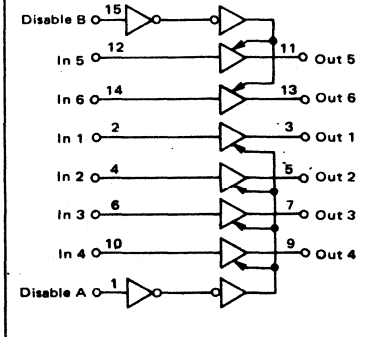
*Diode protection on all inputs (not shown)

TRUTH TABLE

In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

X = Don't Care

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage # "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 11.5 or 3.5 Vdc) "1" Level		15	–	3.75	–	6.75	3.75	–	3.75	
(V_O = 1.4 or 3.6 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.0	–	7.0	5.5	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.25	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)***	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		4.5	-4.3	–	-3.6	-5.0	–	-2.5	–	
(V_{OH} = 2.5 Vdc)		5.0	-5.8	–	-4.80	-6.1	–	-3.0	–	
(V_{OH} = 4.6 Vdc)		5.0	-1.2	–	-1.02	-1.4	–	-0.7	–	
(V_{OH} = 9.5 Vdc)		10	-3.1	–	-2.60	-3.7	–	-1.8	–	
(V_{OH} = 13.5 Vdc)		15	-8.2	–	-6.80	-14.1	–	-4.8	–	
Sink	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		4.5	2.2	–	1.8	2.1	–	1.2	–	
(V_{OL} = 0.4 Vdc)		5.0	2.6	–	2.1	2.3	–	1.3	–	
(V_{OL} = 0.5 Vdc)		10	6.5	–	5.5	6.2	–	3.8	–	
(V_{OL} = 1.5 Vdc)		15	19.2	–	16.10	25.00	–	11.2	–	
Output Drive Current (CL/CP Device)***	I_{OH}						–			mAdc
(V_{OH} = 2.5 Vdc) Source		4.75	-4.0	–	-3.60	-5.5	–	-2.4	–	
(V_{OH} = 2.5 Vdc)		5.0	-4.6	–	-4.20	-6.1	–	-3.0	–	
(V_{OH} = 4.6 Vdc)		5.0	-1.0	–	-0.88	-1.4	–	-0.7	–	
(V_{OH} = 9.5 Vdc)		10	-2.4	–	-2.20	-3.7	–	-1.8	–	
(V_{OH} = 13.5 Vdc)		15	-6.6	–	-6.00	-14.1	–	-4.8	–	
Sink	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		4.75	2.1	–	1.95	2.2	–	1.25	–	
(V_{OL} = 0.4 Vdc)		5.0	2.3	–	2.10	2.3	–	1.3	–	
(V_{OL} = 0.5 Vdc)		10	6.0	–	5.45	6.2	–	3.8	–	
(V_{OL} = 1.5 Vdc)		15	15.2	–	13.80	25.00	–	11.2	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_Q	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**†	I_T	5.0	I_T = (2.5 μA/kHz) f + I_{DD}							μAdc
(Dynamic plus Quiescent, Per Package)		10	I_T = (6.0 μA/kHz) f + I_{DD}							
(C_L = 50 pF on all outputs)		15	I_T = (10 μA/kHz) f + I_{DD}							
(All outputs switching, 50% Duty Cycle)										
3-State Output Leakage Current	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	μAdc
(AL Device)			–		–			–		
3-State Output Leakage Current	I_{TL}	15	–	±1.0	–	±0.0001	±1.0	–	±7.5	μAdc
(CL/CP Device)			–		–			–		

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

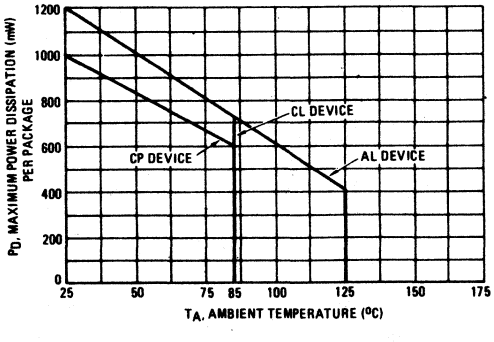
I_T is in μA (per package) C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C
***Care must be taken not to exceed maximum current ratings (see maximum ratings table and Figure 1).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V_{CC}	All Types Typ	All Types Max	Unit
Output Rise Time	t_{TLH}				ns
t_{TLH} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{TLH} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{TLH} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Output Fall Time	t_{THL}				ns
t_{THL} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{THL} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{THL} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Turn-Off Delay Time, all Outputs	t_{PLH}				ns
t_{PLH} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PLH} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PLH} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
Turn-On Delay Time, all Outputs	t_{PHL}				ns
t_{PHL} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PHL} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PHL} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
3-State Propagation Delay Time	t_{PHZ}	5.0	75	150	ns
Output "1" to High Impedance		10	40	80	
		15	35	70	
Output "0" to High Impedance	t_{PLZ}	5.0	80	160	ns
		10	40	80	
		15	35	70	
High Impedance to "1" Level	t_{PZH}	5.0	65	130	ns
		10	25	50	
		15	20	40	
High Impedance to "0" Level	t_{PZL}	5.0	100	200	ns
		10	35	70	
		15	25	50	

*The formulas given are for the typical characteristics only.

FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING



PIN ASSIGNMENT

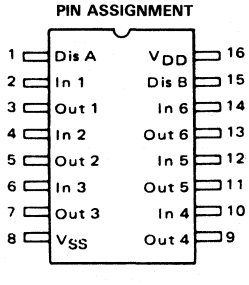


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH})

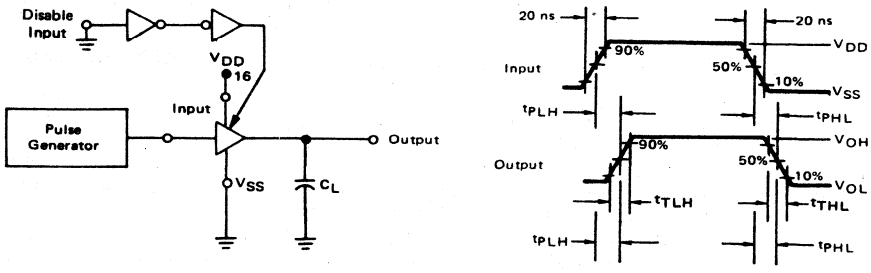
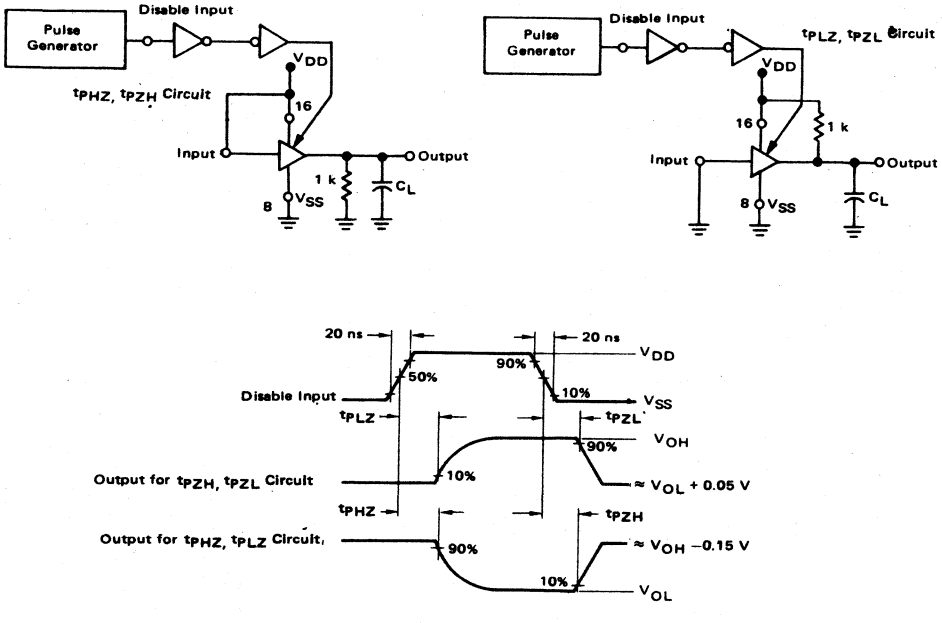


FIGURE 3 – 3 STATE AC TEST CIRCUITS AND WAVEFORMS
(t_{PLZ}, t_{PHZ}, t_{PZH}, t_{PZL})



MOTOROLA

MC14504B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

TTL or CMOS to CMOS
HEX LEVEL SHIFTER

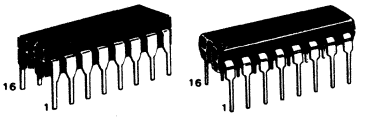
3

HEX LEVEL SHIFTER FOR TTL to CMOS or CMOS to CMOS

The MC14504B is a hex non-inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level. Either up or down level translating is accomplished by selection of power supply levels V_{DD} and V_{CC}. The V_{CC} level sets the input signal levels while V_{DD} selects the output voltage levels.

Supply current is typically 1 nA @ V_{DD} = 10 V for CMOS to CMOS operation. When translating from TTL to CMOS supply current is typically 2.5 mA taken from V_{CC}.

- UP Translates from a Low to a High Voltage or
  DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- *No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for V_{DD} and V_{CC}
- Diode Protected Inputs to V_{SS}
- Capable of Driving Two Low Power TTL Loads, One Low Power Schottky TL Load or Two HTL Loads over the Rated Temperature Range



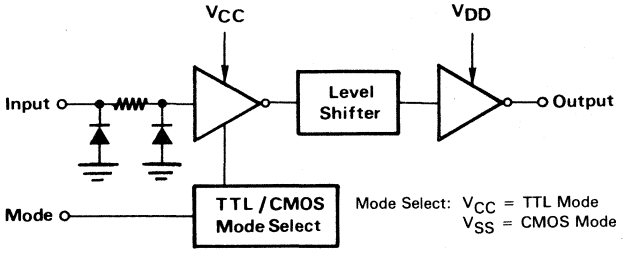
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

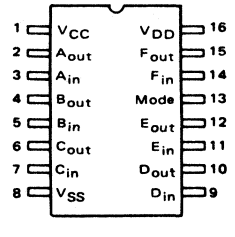
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

LOGIC DIAGRAM



1/6 of package shown.

PIN ASSIGNMENT



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	−0.5 to +18	Vdc
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{CC} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq V_{in} \leq V_{CC}$ and $V_{SS} \leq V_{out} \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either V_{SS} or V_{CC}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{CC} Vdc	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	–	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = 0 V		–	10	–	0.05	–	0	0.05	–	0.05	
		–	15	–	0.05	–	0	0.05	–	0.05	
V_{in} = V_{CC} "1" Level	V_{OH}	–	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		–	10	9.95	–	9.95	10	–	9.95	–	
		–	15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}										Vdc
(V_{OL} = 1.0 Vdc) TTL–CMOS		5	10	–	0.8	–	1.3	0.8	–	0.8	
(V_{OL} = 1.5 Vdc) TTL–CMOS		5	15	–	0.8	–	1.3	0.8	–	0.8	
(V_{OL} = 1.0 Vdc) CMOS–CMOS		5	10	–	1.5	–	2.25	1.5	–	1.4	
(V_{OL} = 1.5 Vdc) CMOS–CMOS		5	15	–	1.5	–	2.25	1.5	–	1.5	
(V_{OL} = 1.5 Vdc) CMOS–CMOS		10	15	–	3.0	–	4.5	3.0	–	2.9	
Input Voltage "1" Level	V_{IH}										Vdc
(V_{OH} = 9.0 Vdc) TTL–CMOS		5	10	2.0	–	2.0	1.5	–	2.0	–	
(V_{OH} = 13.5 Vdc) TTL–CMOS		5	15	2.0	–	2.0	1.5	–	2.0	–	
(V_{OH} = 9.0 Vdc) CMOS–CMOS		5	10	3.6	–	3.5	2.75	–	3.5	–	
(V_{OH} = 13.5 Vdc) CMOS–CMOS		5	15	3.6	–	3.5	2.75	–	3.5	–	
(V_{OH} = 13.5 Vdc) CMOS–CMOS		10	15	7.1	–	7.0	5.5	–	7.0	–	
Output Drive Current (AL Device)	I_{OH}										mAdc
(V_{OH} = 2.5 Vdc) Source		–	5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		–	5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		–	10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		–	15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	–	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		–	10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		–	15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}										mAdc
(V_{OH} = 2.5 Vdc) Source		–	5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		–	5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		–	10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		–	15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	–	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		–	10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		–	15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL)	I_{in}	–	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP)	I_{in}	–	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD} or	–	5.0	–	0.05	–	0.0005	0.05	–	1.5	μAdc
(Per Package)	I_{CC}	–	10	–	0.10	–	0.0010	0.10	–	3.0	
CMOS–CMOS Mode		–	15	–	0.20	–	0.0015	0.20	–	6.0	
Quiescent Current (CL/CP Device)	I_{DD} or	–	5.0	–	0.5	–	0.0005	0.5	–	3.8	μAdc
(Per Package)	I_{CC}	–	10	–	1.0	–	0.0010	1.0	–	7.5	
CMOS–CMOS Mode		–	15	–	2.0	–	0.0015	2.0	–	15.0	
Quiescent Current (AL/CL/CP Device)	I_{DD}	5.0	5.0	–	0.5	–	0.0005	0.5	–	3.8	μAdc
(Per Package)		5.0	10	–	1.0	–	0.0010	1.0	–	7.5	
TTL–CMOS Mode		5.0	15	–	2.0	–	0.0015	2.0	–	15.0	
Quiescent Current (AL/CL/CP Device)	I_{CC}	5.0	5.0	–	5.0	–	2.5	5.0	–	6.0	mAdc
(Per Package)		5.0	10	–	5.0	–	2.5	5.0	–	6.0	
TTL–CMOS Mode		5.0	15	–	5.0	–	2.5	5.0	–	6.0	

*T_{LOW} = −55°C for AL Device, −40°C for CL/CP Device
T_{HIGH} = +125°C for AL Device, +85°C for CL/CP Device

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	Shifting Mode	V_{CC} Vdc	V_{DD} Vdc	Limits Min	Limits Typ	Limits Max	Units
Propagation Delay, High to Low	t_{PHL}	TTL–CMOS	5.0	10	–	120	280	ns
		$V_{DD} > V_{CC}$	5.0	15	–	120	280	
		CMOS–CMOS	5.0	10	–	100	240	
		$V_{DD} > V_{CC}$	5.0	15	–	120	240	
			10	15	–	50	140	
		CMOS–CMOS	10	5.0	–	160	370	
		$V_{CC} > V_{DD}$	15	5.0	–	160	370	
			15	10	–	160	–	
Propagation Delay, Low to High	t_{PLH}	TTL–CMOS	5.0	10	–	200	340	ns
		$V_{DD} > V_{CC}$	5.0	15	–	160	320	
		CMOS–CMOS	5.0	10	–	100	340	
		$V_{DD} > V_{CC}$	5.0	15	–	120	340	
			10	15	–	50	200	
		CMOS–CMOS	10	5.0	–	160	550	
		$V_{CC} > V_{DD}$	15	5.0	–	160	550	
			15	10	–	65	290	
Output Rise and Fall Time	t_{TLH}, t_{THL}	ALL	–	5.0	–	100	200	ns
			–	10	–	50	100	
			–	15	–	40	80	

3

FIGURE 1 – INPUT SWITCHPOINT CMOS to CMOS MODE

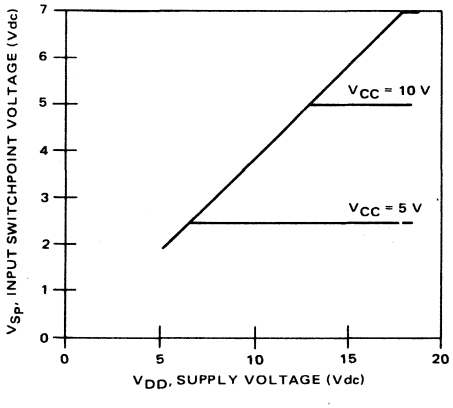


FIGURE 2 – INPUT SWITCHPOINT TTL to CMOS MODE

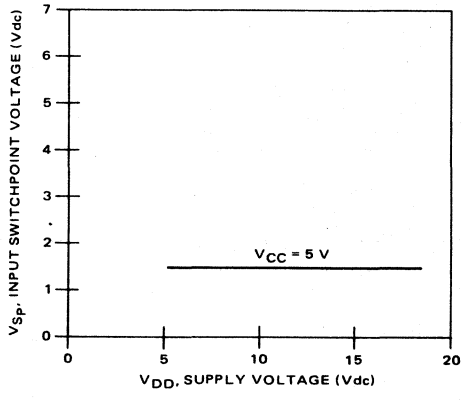


FIGURE 3 – OPERATING BOUNDARY CMOS to CMOS MODE

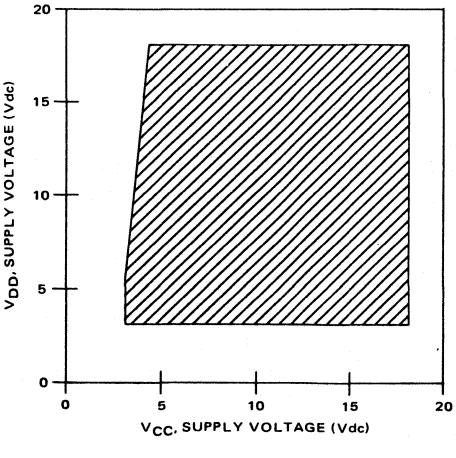
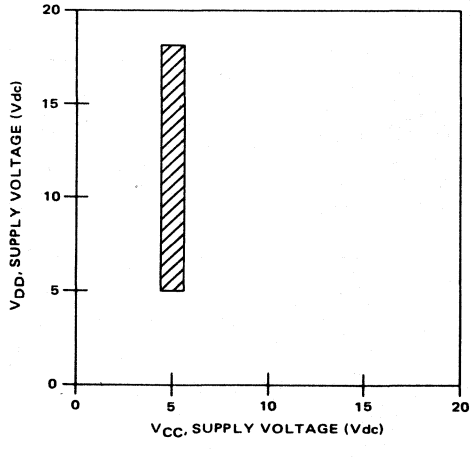


FIGURE 4 – OPERATING BOUNDARY TTL to CMOS MODE



MOTOROLA

MC14506UB

DUAL 2-WIDE, 2-INPUT EXPANDABLE AND-OR-INVERT GATE

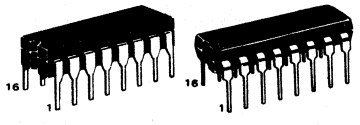
The MC14506UB is an expandable AND-OR-INVERT gate with inhibit and 3-state output. The expand option allows cascading with any other gate, which may be carried as far as desired as long as the propagation delay added with each gate is considered. For example, the second AOI gate in this device may be used to expand the first gate, giving an expanded 4-wide, 2-input AOI gate. This device is useful in data control and digital multiplexing applications.

- Quiescent Current = 2.0 nA/Package typical @ 5 Vdc
- 3-State Output
- Separate Inhibit Line
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL EXPANDABLE AND-OR-INVERT GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

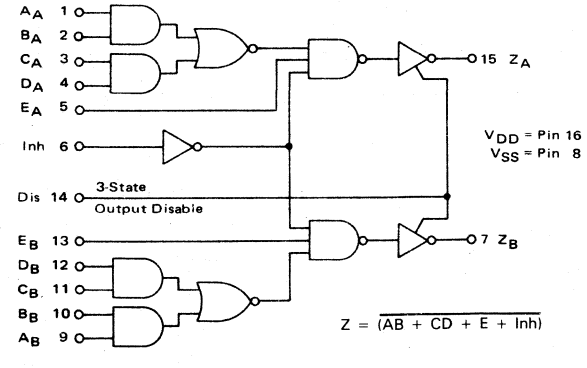
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

LOGIC DIAGRAM



TRUTH TABLE

A	B	C	D	E	INHIBIT	DISABLE	Z
0	0	0	0	1	0	0	1
0	X	0	X	1	0	0	1
0	X	X	0	1	0	0	1
X	0	0	X	1	0	0	1
X	0	X	0	1	0	0	1
1	1	X	X	X	X	0	0
X	X	1	1	X	X	0	0
X	X	X	X	0	X	0	0
X	X	X	X	X	1	0	0
X	X	X	X	X	X	1	High Impedance

X = Don't Care

ELECTRICAL CHARACTERISTICS

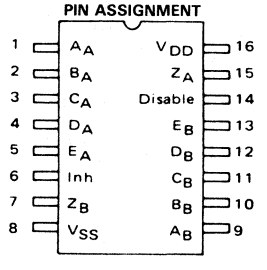
Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	
(V_O = 9.0 or 1.0 Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	μAdc
		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.6\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (1.1\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (1.7\ \mu A/kHz)\ f + I_{DD}$							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



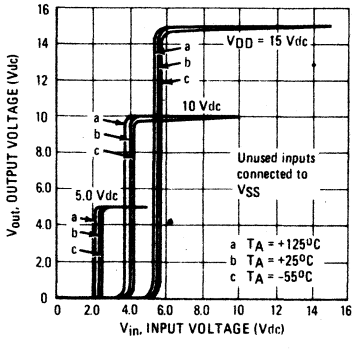
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Data Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 210 ns		5.0	–	295	580	
t_{PLH} = (0.66 ns/pF) C_L + 77 ns		10	–	110	225	
t_{PLH} = (0.5 ns/pF) C_L + 50 ns		15	–	75	180	
t_{PHL} = (1.7 ns/pF) C_L + 185 ns	t_{PHL}	5.0	–	270	480	ns
t_{PHL} = (0.66 ns/pF) C_L + 62 ns		10	–	95	175	
t_{PHL} = (0.5 ns/pF) C_L + 40 ns		15	–	65	140	
Expand Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 95 ns		5.0	–	180	430	
t_{PLH} = (0.66 ns/pF) C_L + 42 ns		10	–	75	160	
t_{PLH} = (0.5 ns/pF) C_L + 25 ns		15	–	50	125	
t_{PHL} = (1.7 ns/pF) C_L + 115 ns	t_{PHL}	5.0	–	200	330	ns
t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	–	80	110	
t_{PHL} = (0.5 ns/pF) C_L + 30 ns		15	–	55	90	
Inhibit Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 135 ns		5.0	–	220	500	
t_{PLH} = (0.66 ns/pF) C_L + 67 ns		10	–	100	225	
t_{PLH} = (0.5 ns/pF) C_L + 40 ns		15	–	65	160	
t_{PHL} = (1.7 ns/pF) C_L + 145 ns	t_{PHL}	5.0	–	230	400	ns
t_{PHL} = (0.66 ns/pF) C_L + 62 ns		10	–	95	175	
t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	150	
3-State Propagation Delay Time						
"1" to High Impedance	t_{PHZ}	5.0	–	60	150	ns
		10	–	45	110	
		15	–	35	90	
"0" to High Impedance	t_{PLZ}	5.0	–	90	225	ns
		10	–	55	140	
		15	–	40	100	
High Impedance to "1"	t_{PZH}	5.0	–	110	300	ns
		10	–	50	125	
		15	–	40	100	
High Impedance to "0"	t_{PZL}	5.0	–	170	425	ns
		10	–	70	175	
		15	–	50	125	

*The formulae given are for the typical characteristics only.

FIGURE 1 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

(a) EXPAND INPUTS



(b) DATA INPUTS

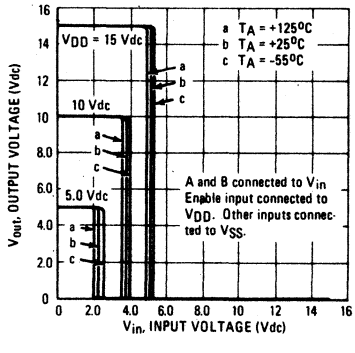


FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

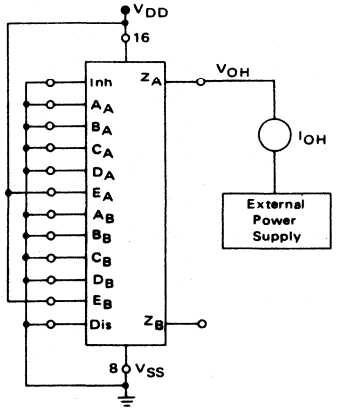


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

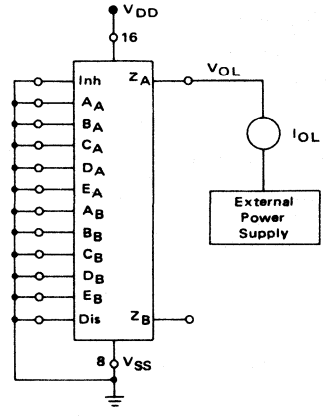


FIGURE 4 – 3-STATE LEAKAGE CURRENT TEST CIRCUIT

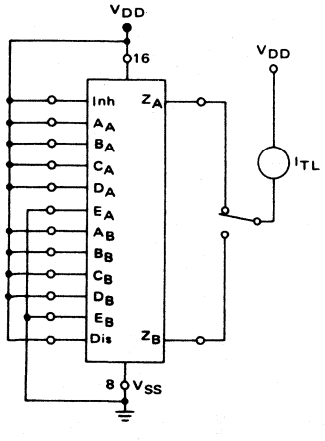


FIGURE 5 – TYPICAL POWER DISSIPATION TEST CIRCUIT

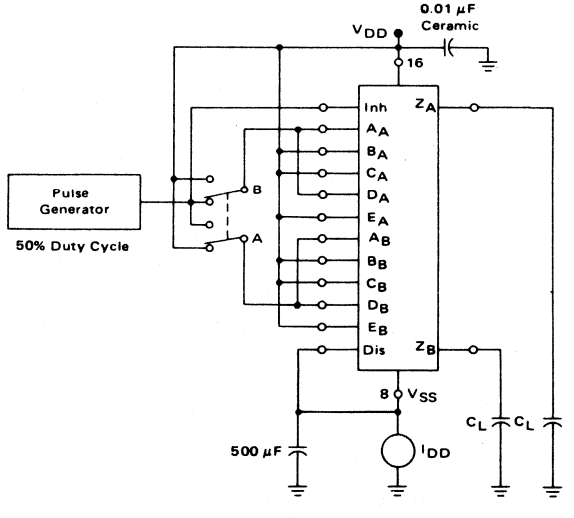


FIGURE 6 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(Data Inputs)

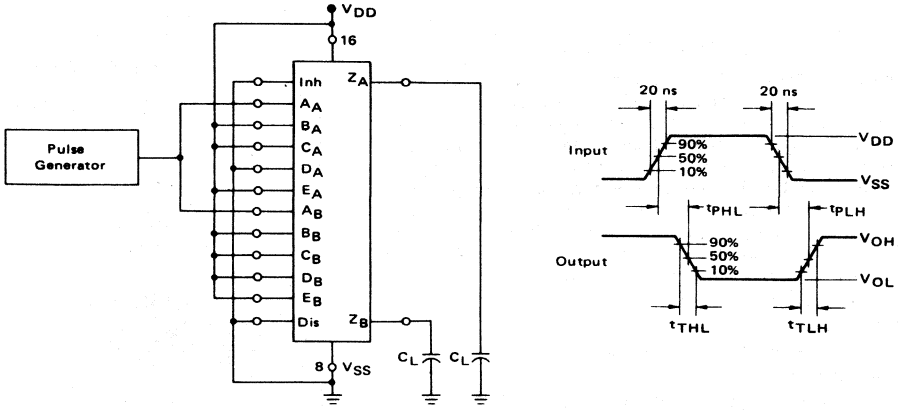
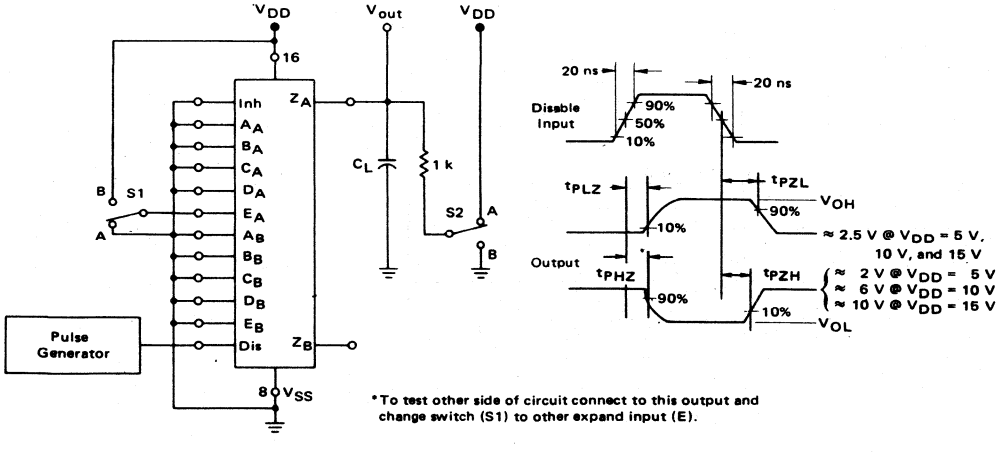


FIGURE 7 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(For 3-State Output)



*To test other side of circuit connect to this output and change switch (S1) to other expand input (E).

SWITCH POSITIONS

TEST	S1	S2
t_{PLZ}	A	A
t_{PHZ}	B	B
t_{PZL}	A	A
t_{PZH}	B	B

MOTOROLA

MC14508B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

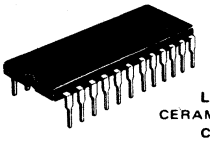
DUAL 4-BIT LATCH

DUAL 4-BIT LATCH

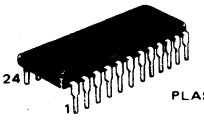
The MC14508B dual 4-bit latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The part consists of two identical, independent 4-bit latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high impedance state and allow the devices to be used in time sharing bus line applications.

These complementary MOS latches find primary use in buffer storage, holding register, or general digital logic functions where low power dissipation and/or high noise immunity is desired. Additional characteristics can be found on the Family Data Sheet.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- 3-State Output
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

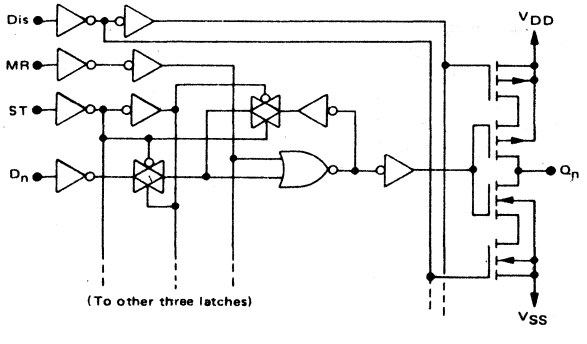
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

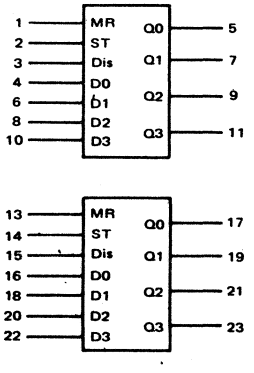
MR	ST	Disable	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1	0	0	0
0	0	0	X	X	X	X	Latched			
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X	High Impedance			

X = Don't Care

CIRCUIT DIAGRAM



BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.46 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.91 μA/kHz) f + I_{DD}							
		15	I_T = (4.37 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

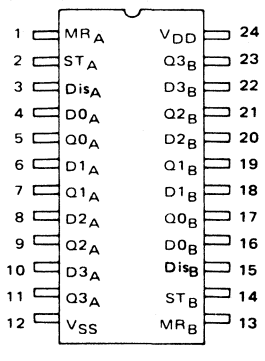
*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 8 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types Min	All Types Typ	All Types Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Master Reset Pulse Width	$t_{WH(R)}$	5.0	200	100	–	ns
		10	100	50	–	
		15	70	35	–	
Strobe Pulse Width	$t_{WH(S)}$	5.0	140	70	–	ns
		10	70	35	–	
		15	40	20	–	
Setup Time	t_{su}	5.0	50	25	–	ns
		10	20	10	–	
		15	10	5.0	–	
Hold Time	t_h	5.0	0	0	–	ns
		10	0	0	–	
		15	0	0	–	
3-State Propagation Delay Time	t_{PHZ}					ns
Output "1" to High Impedance						
t_{PHZ} = (0.49 ns/pF) C_L + 60.5 ns		5.0	–	85	170	
t_{PHZ} = (0.29 ns/pF) C_L + 35.5 ns		10	–	50	100	
t_{PHZ} = (0.19 ns/pF) C_L + 25.5 ns		15	–	35	70	
Output "0" to High Impedance	t_{PLZ}					ns
t_{PLZ} = 0.32 ns/pF) C_L + 49 ns		5.0	–	65	130	
t_{PLZ} = (0.29 ns/pF) C_L + 25.5 ns		10	–	40	80	
t_{PLZ} = (0.28 ns/pF) C_L + 16 ns		15	–	30	60	
High Impedance to "1" Level	t_{PZH}					ns
t_{PZH} = (0.41 ns/pF) C_L + 64.5 ns		5.0	–	85	170	
t_{PZH} = (0.31 ns/pF) C_L + 34.5 ns		10	–	50	100	
t_{PZH} = (0.30 ns/pF) C_L + 20 ns		15	–	35	70	
High Impedance to "0" Level	t_{PZL}					ns
t_{PZL} = (0.49 ns/pF) C_L + 60.5 ns		5.0	–	85	170	
t_{PZL} = (0.29 ns/pF) C_L + 35.5 ns		10	–	50	100	
t_{PZL} = (0.19 ns/pF) C_L + 25.5 ns		15	–	35	70	

*The formulae given are for the typical characteristics only.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

FIGURE 1 – AC WAVEFORMS

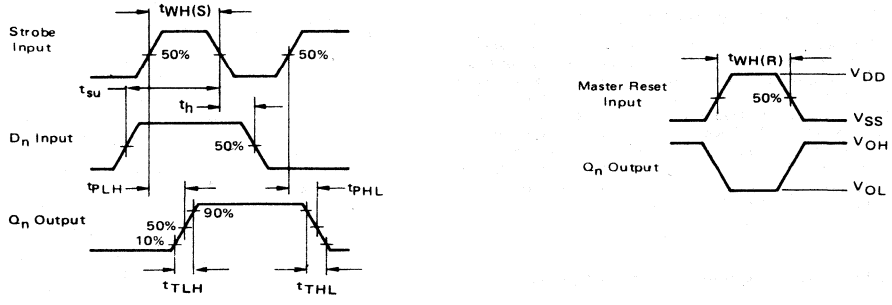
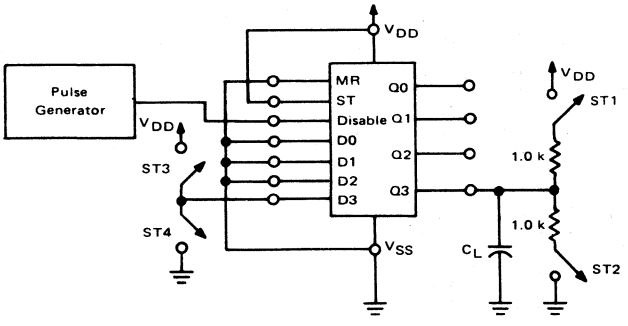
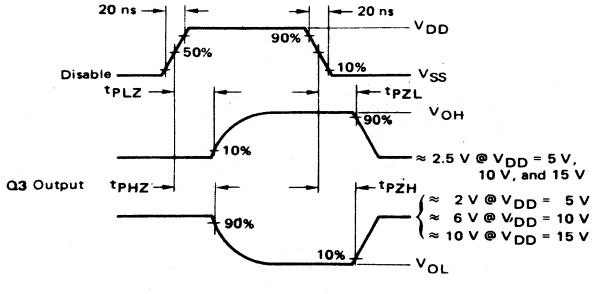


FIGURE 2 – 3-STATE AC TEST CIRCUIT AND WAVEFORMS



TEST	ST1	ST2	ST3	ST4
t_{PHZ}	OPEN	CLOSE	CLOSE	OPEN
t_{PLZ}	CLOSE	OPEN	OPEN	CLOSE
t_{PZL}	CLOSE	OPEN	OPEN	CLOSE
t_{PZH}	OPEN	CLOSE	CLOSE	OPEN

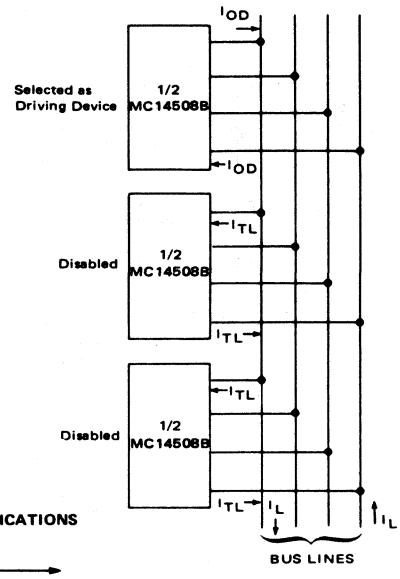


3-STATE MODE OF OPERATION

The MC14508B can be used in bussed systems as shown. The output terminals of N 4-bit latches can be directly wired to a bus line, and to one of the 4-bit latches selected. The selected latch controls the logic state of the bus line, and the remaining (N-1) 4-bit latches are disabled into a high impedance "off" state. The number of latches, N, which may be connected to a bus line is determined from the output drive current, I_{OD}, the 3-state or disabled output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs) and can be calculated by the following:

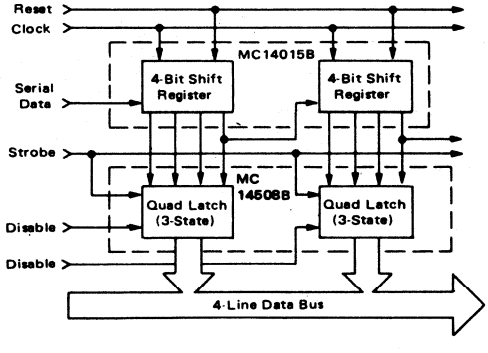
$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the bus line.

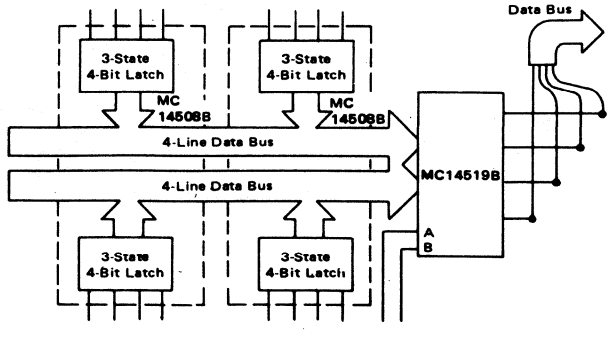


TYPICAL 3–STATE APPLICATIONS

EXAMPLE 1



EXAMPLE 2



MOTOROLA

MC14510B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

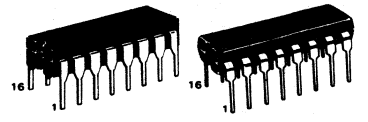
BCD UP/DOWN COUNTER

3

BCD UP/DOWN COUNTER

The MC14510B BCD up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide type T flip-flop capability. The counter can be cleared by applying a high level on the Reset line. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

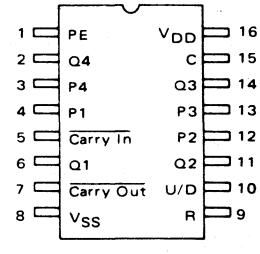
- Quiescent Current = 5.0 nA/package typical @ 5.0 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance — 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design — Count Occurs on Positive Going Edge of Clock
- 5.0-MHz Counting Rate
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

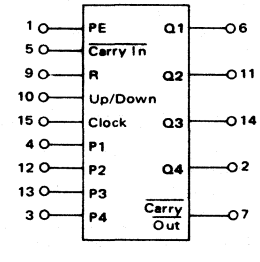
PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

CARRY IN	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.70	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L +15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Clock to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns		5.0	–	180	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 47 ns		10	–	80	160	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Preset or Reset to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Preset or Reset ot $\overline{\text{Carry Out}}$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
Clock Pulse Width	t_{WH}	5.0	350	200	–	ns
		10	170	100	–	
		15	140	75	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Preset or Reset Removal Time**	t_{rem}	5.0	650	325	–	ns
		10	230	115	–	
		15	180	90	–	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
$\overline{\text{Carry In}}$ Setup Time	t_{su}	5.0	200	130	–	ns
		10	120	60	–	
		15	100	50	–	
Up/Down Setup Time	t_{su}	5.0	500	250	–	ns
		10	200	100	–	
		15	175	75	–	
Preset Enable Pulse Width	t_{WH}	5.0	200	100	–	ns
		10	100	50	–	
		15	80	40	–	

* The formulae given are for the typical characteristics only.

** The Preset or Reset Signal must be low prior to a positive-going transition of the clock.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

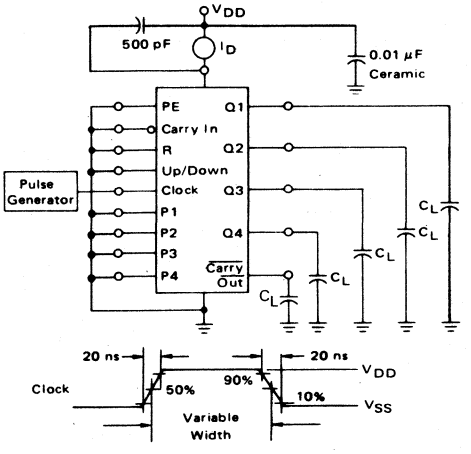
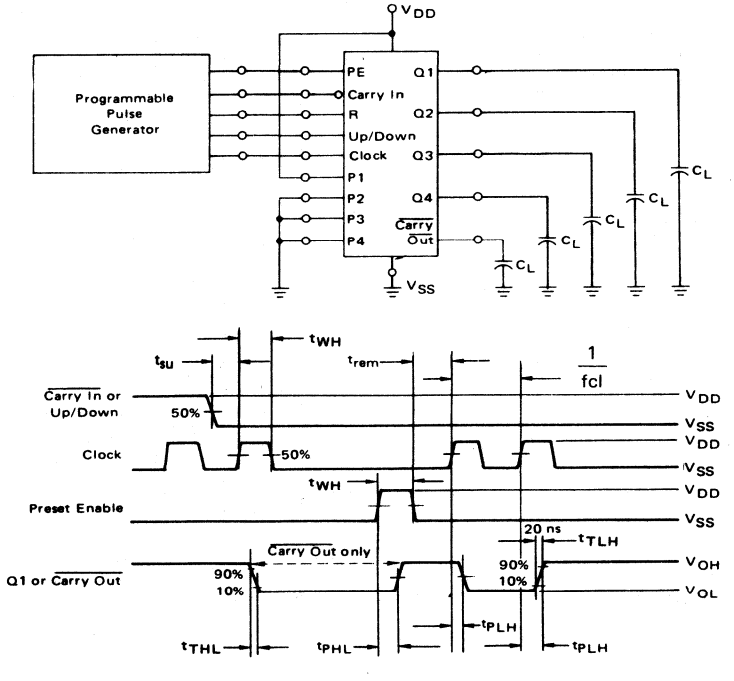
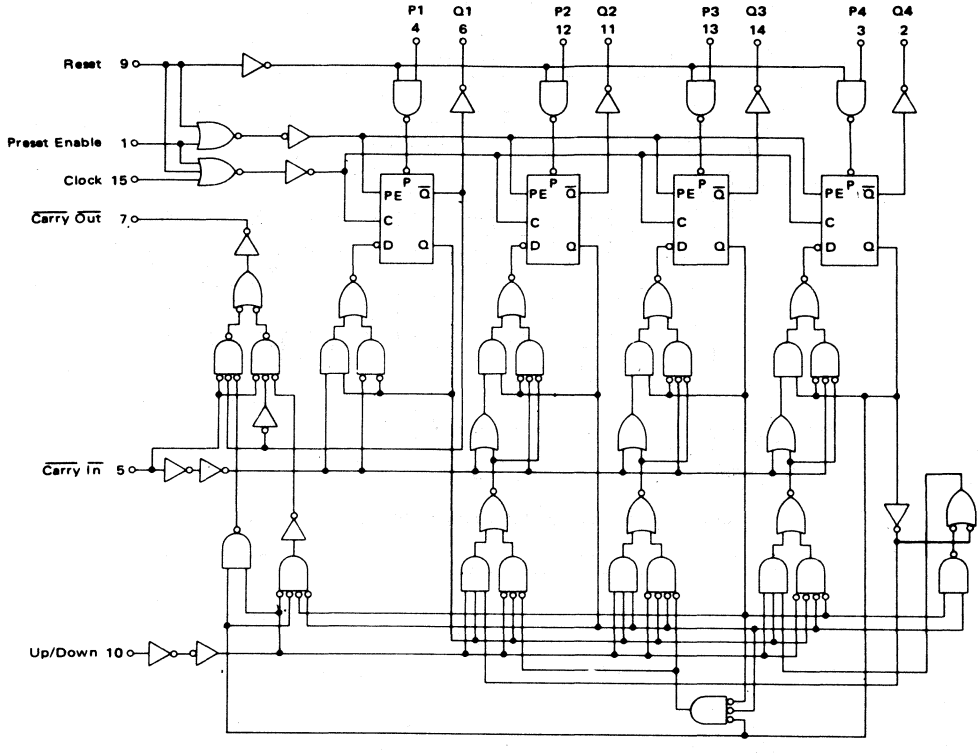


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAM



TIMING DIAGRAM

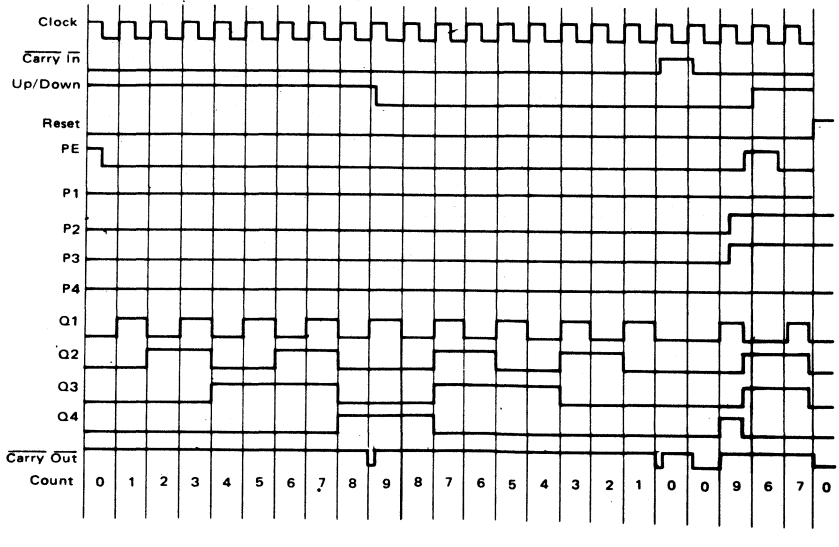


FIGURE 3 – PRESETTABLE CASCADED UP/DOWN COUNTER

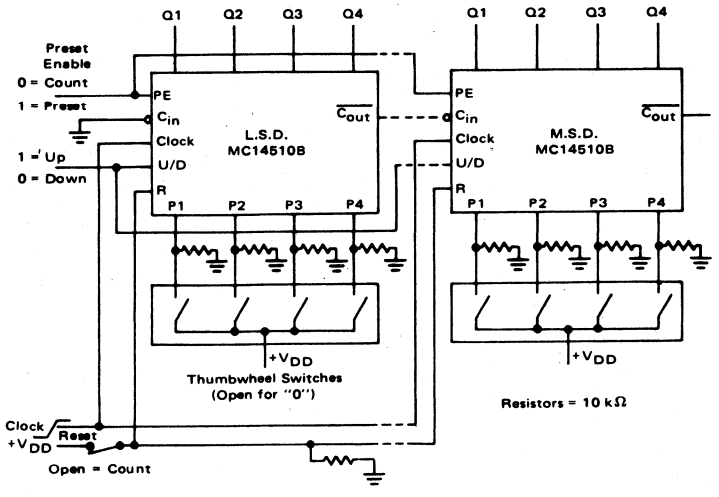
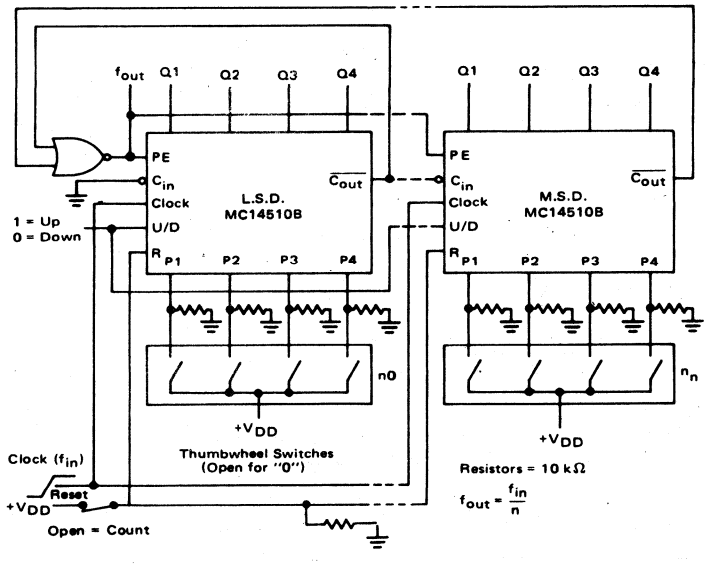


FIGURE 4 – PROGRAMMABLE CASCADED FREQUENCY DIVIDER



MOTOROLA

MC14512B

8-CHANNEL DATA SELECTOR

The MC14512B is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- High Fanout > 50
- Single Supply Operation – Positive or Negative
- 3-State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

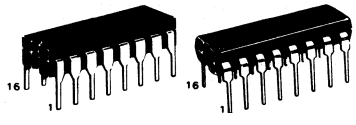
C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
ϕ	ϕ	ϕ	1	0	0
ϕ	ϕ	ϕ	ϕ	1	High Impedance

ϕ = Don't Care

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-CHANNEL DATA SELECTOR



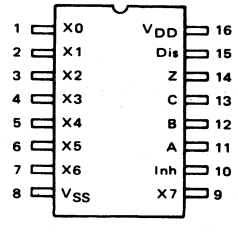
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage#	"0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)			5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)			10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)			15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)			5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)			10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)			15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)		I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)		I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)		I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)			10	–	10	–	0.010	10	–	300	
			15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)		I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)			10	–	40	–	0.010	40	–	300	
			15	–	80	–	0.015	80	–	600	
Total Supply Current**†		I_T	5.0	I_T = (0.8 µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package)			10	I_T = (1.6 µA/kHz) f + I_{DD}							
(C_L = 50 pF on all outputs, all buffers switching)			15	I_T = (2.4 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)		I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)		I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3}(C_L - 50)\ V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types		Unit
			Typ	Max	
Output Rise Time	^tTLH				ns
^tTLH = (3.0 ns/pF) C_L + 25 ns		5.0	100	200	
^tTLH = (1.5 ns/pF) C_L + 12 ns		10	50	100	
^tTLH = (1.1 ns/pF) C_L + 8 ns		15	40	80	
Output Fall Time	^tTHL				ns
^tTHL = (1.5 ns/pF) C_L + 47 ns		5.0	130	200	
^tTHL = (0.75 ns/pF) C_L + 24 ns		10	65	100	
^tTHL = (0.55 ns/pF) C_L + 17 ns		15	50	80	
Turn-Off Delay Time	^tPLH				ns
^tPLH = (0.9 ns/pF) C_L + 211 ns		5.0	330	650	
^tPLH = (0.3 ns/pF) C_L + 70 ns		10	125	250	
^tPLH = (0.23 ns/pF) C_L + 54 ns		15	85	170	
Turn-On Delay Time	^tPHL				ns
^tPHL = (2.7 ns/pF) C_L + 184 ns		5.0	330	650	
^tPHL = (0.9 ns/pF C_L + 61 ns		10	125	250	
^tPHL = (0.68 ns/pF) C_L + 47 ns		15	85	170	
3-State Output Delay Times	^tPHZ, ^tPLZ,	5.0	60	150	ns
"1" or "0" to High Z, and	^tPZH, ^tPZL	10	35	100	
High Z to "1" or "0"		15	30	75	

* The formulae given are for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

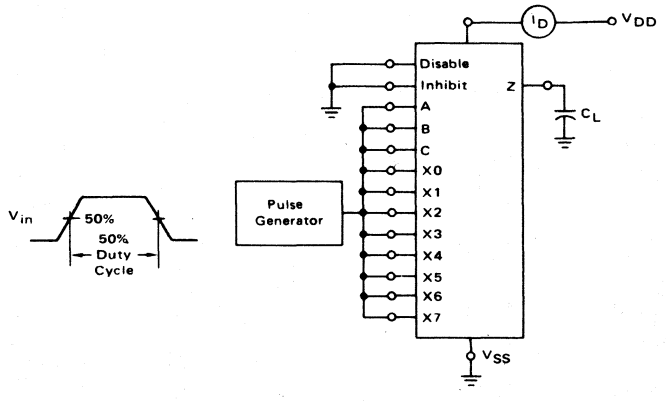
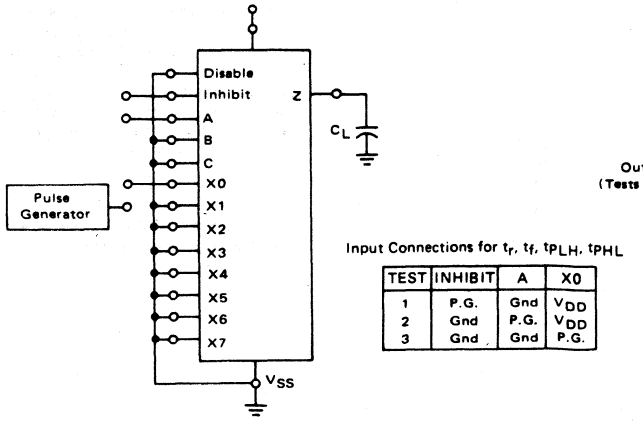


FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



Input Connections for t_r, t_f, t_{PLH}, t_{PHL}

TEST	INHIBIT	A	X0
1	P.G.	Gnd	V_{DD}
2	Gnd	P.G.	V_{DD}
3	Gnd	Gnd	P.G.

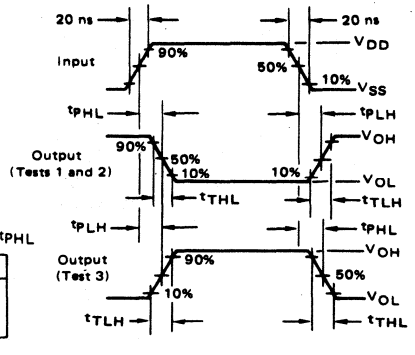
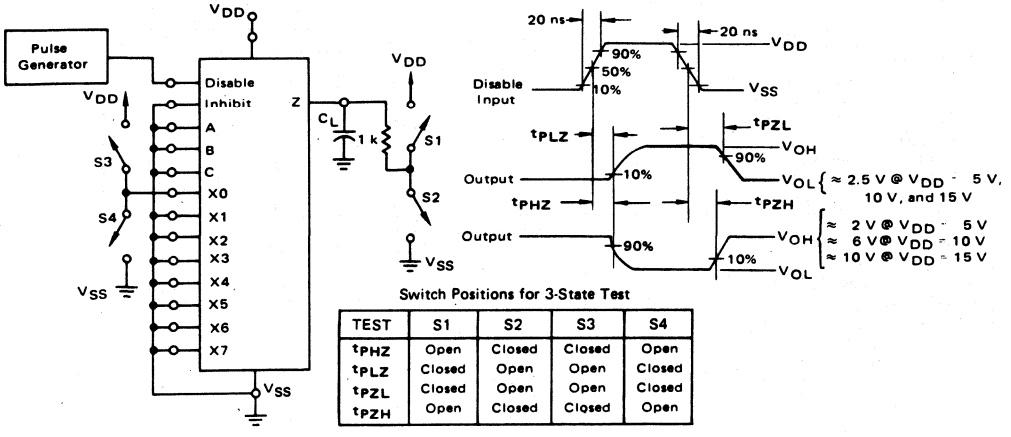


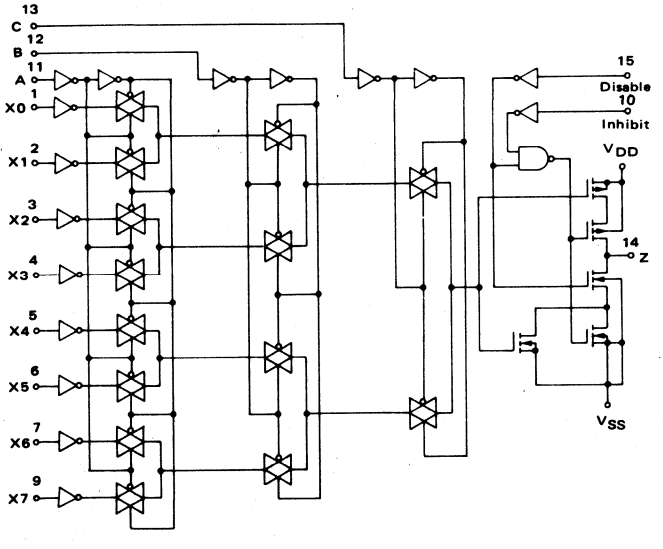
FIGURE 3 – 3-STATE AC TEST CIRCUIT AND WAVEFORM

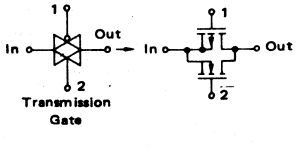


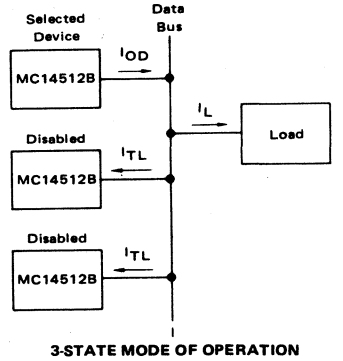
Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

LOGIC DIAGRAM







3-STATE MODE OF OPERATION

Output terminals of several MC14512B 8-Bit Data Selectors can be connected to a single data bus as shown. One MC14512B is selected by the 3-state control, and the remaining devices are disabled into a high-impedance "off" state. The number of 8-bit data selectors, N, that may be connected to a bus line is determined from the output drive current, I_{OD}, 3-state or disable output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs), and can be calculated by:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic state of the bus line.

MOTOROLA

MC14514B
MC14515B

4-BIT TRANSPARENT LATCH/4-TO-16 LINE DECODER

The MC14514B and MC14515B are two output options of a 4 to 16 line decoder with latched inputs. The MC14514B (output active high option) presents a logical "1" at the selected output, whereas the MC14515B (output active low option) presents a logical "0" at the selected output. The latches are R-S type flip-flops which hold the last input data presented prior to the strobe transition from "1" to "0". These high and low options of a 4-bit latch/4 to 16 line decoder are constructed with N-channel and P-channel enhancement mode devices in a single monolithic structure. The latches are R-S type flip-flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 5.0 nA package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Single Supply Operation – Positive or Negative
- Input Impedance = 10^{12} ohms typical

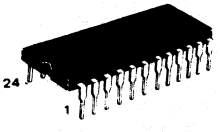
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

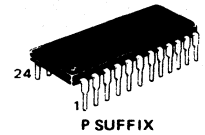
CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT TRANSPARENT LATCH/4-TO-16 LINE DECODER



L SUFFIX
CERAMIC PACKAGE
CASE 623



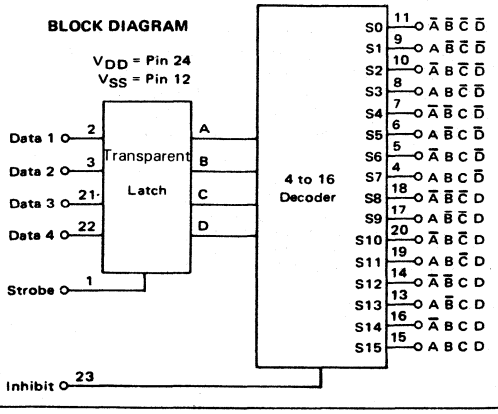
P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM

V_{DD} = Pin 24
V_{SS} = Pin 12



DECODE TRUTH TABLE (Strobe = 1)*

INHIBIT	DATA INPUTS D	C	B	A	SELECTED OUTPUT (MC14514 = Logic "1" MC14515 = Logic "0")
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, MC14514 All Outputs = 1, MC14515

X = Don't Care
*Strobe = 0, Data is latched

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.35 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.70 μA/kHz) f + I_{DD}							
		15	I_T = (4.05 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns	t_{PHL}	5.0	–	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
Inhibit Propagation Delay Times	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns	t_{PHL}	5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	150	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Setup Time	t_{su}					ns
		5.0	250	125	–	
		10	100	50	–	
		15	75	38	–	
Strobe Pulse Width	t_{WH}					ns
		5.0	350	175	–	
		10	100	50	–	
		15	75	38	–	

*The formula given is for the typical characteristics only.

FIGURE 1 – DRAIN CHARACTERISTICS TEST CIRCUIT

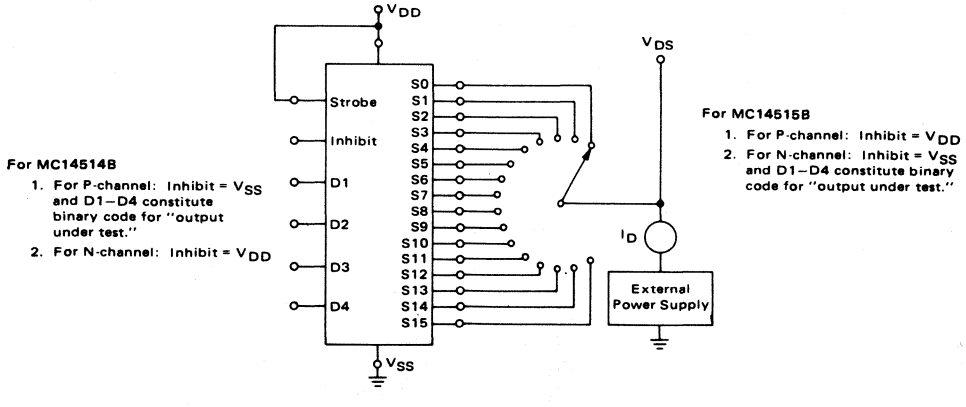


FIGURE 2 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

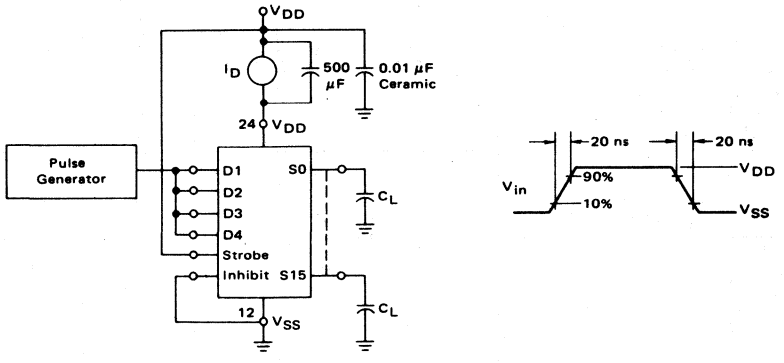
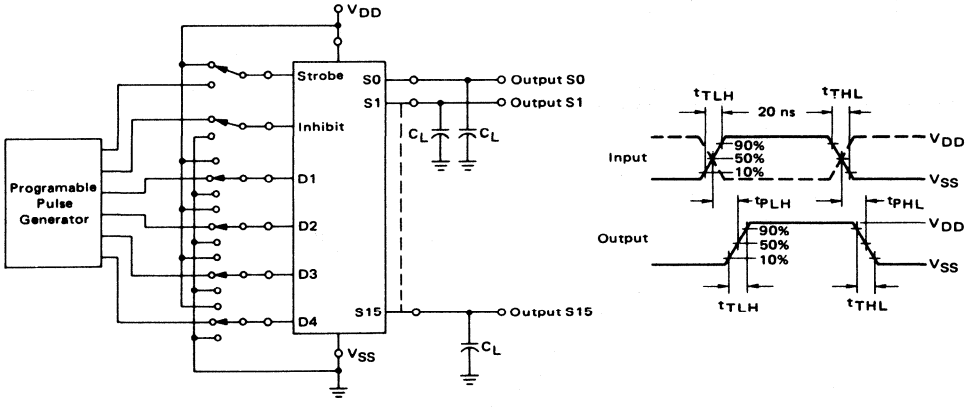
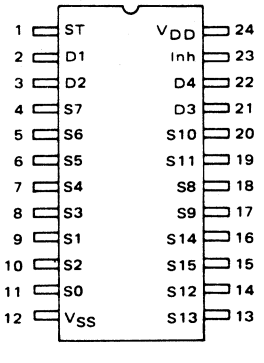


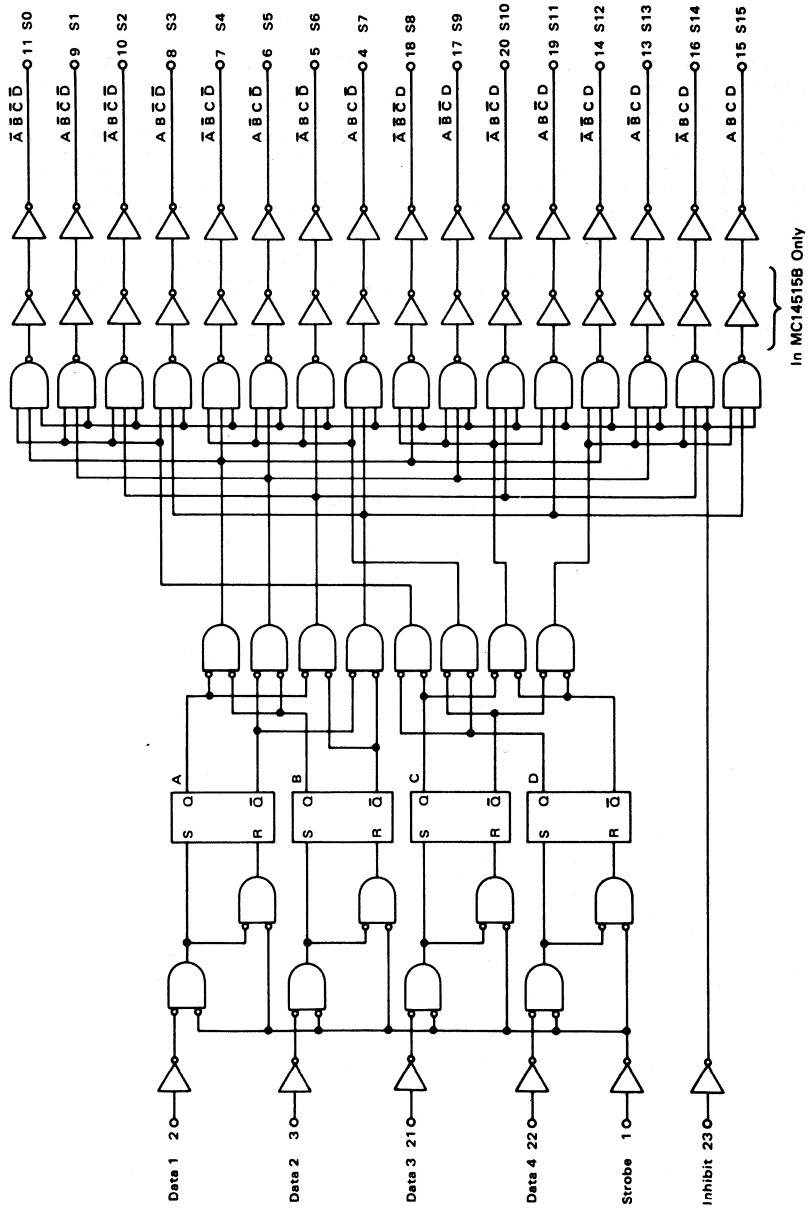
FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



PIN ASSIGNMENT



LOGIC DIAGRAM



COMPLEX DATA ROUTING

Two MC14512 eight-channel data selectors are used here with the MC14514B four-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3-state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

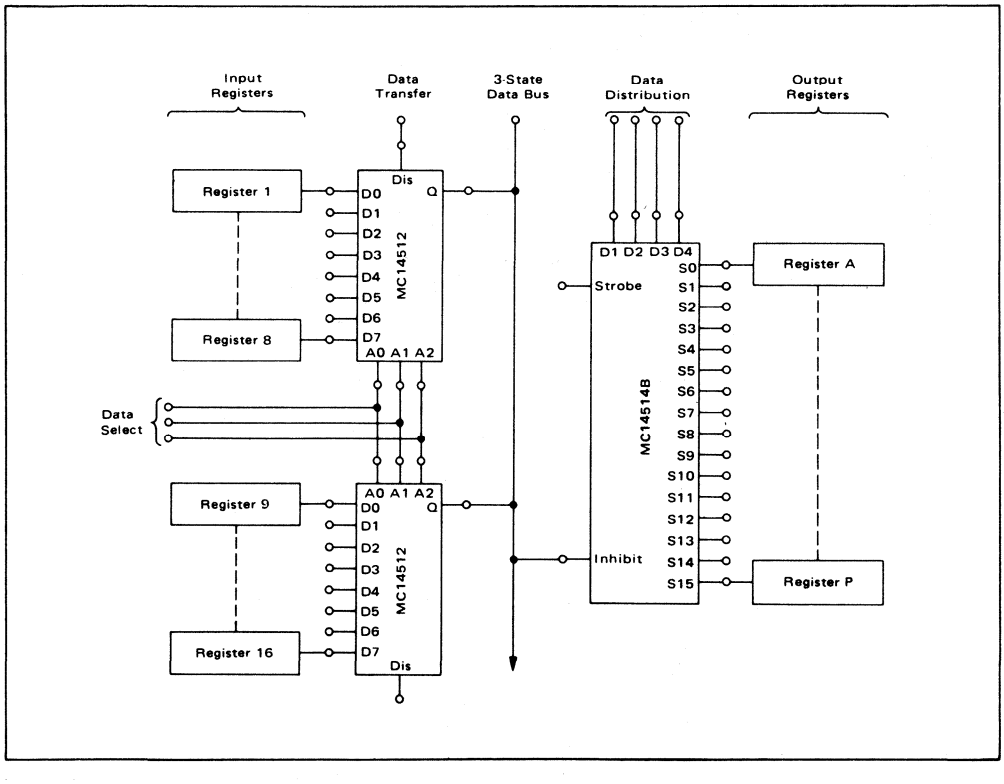
Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3-state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-state bus is redistributed by the MC14514B four-bit latch/decoder. Using the four-bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

3

DATA ROUTING SYSTEM



MOTOROLA

MC14516B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

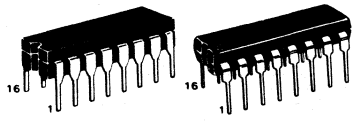
BINARY UP/DOWN COUNTER

BINARY UP/DOWN COUNTER

The MC14516B is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This complementary MOS circuit finds primary use where low power dissipation and/or high noise immunity is desired.

This binary presettable up/down counter may be used as a counting/frequency synthesizer, in A/D and D/A conversion, for up/down counting, for magnitude and sign generation, and for difference counting.

- Quiescent Current = 5.0nA/package typical @ 5.0 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance — 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design — Count Occurs on Positive Going Edge of Clock
- 5.0-MHz Counting Rate
- Single Pin Reset
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

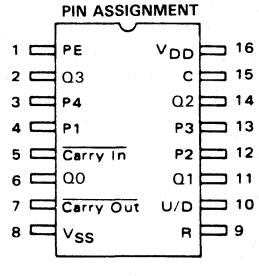
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN ASSIGNMENT



TRUTH TABLE

CARRY IN	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.58 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.7 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

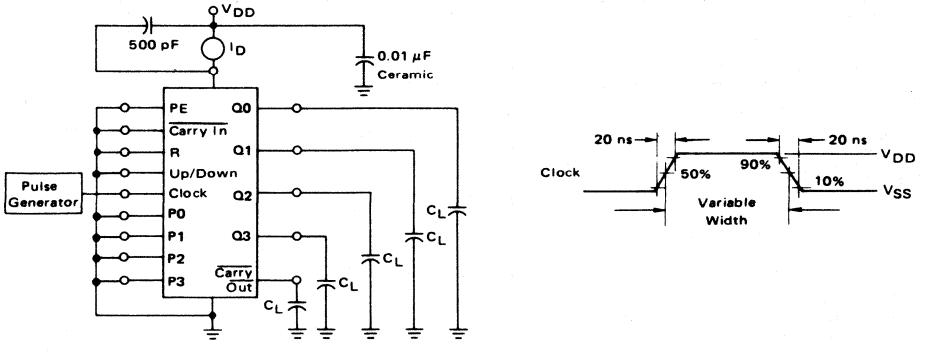
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns		5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Clock to $\overline{\text{Carry Out}}$	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns	t_{PHL}	5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns	t_{PHL}	5.0	–	180	360	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 74 ns		10	–	80	160	
t_{PLH}, t_{PHL} = 0.5 ns/pF) C_L + 35 ns		15	–	60	120	
Preset or Reset to Q	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns	t_{PHL}	5.0	–	315	630	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Preset or Reset to $\overline{\text{Carry Out}}$	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns	t_{PHL}	5.0	–	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns		10	–	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
Clock Pulse Width	t_{WH}	5.0	350	200	–	ns
		10	170	100	–	
		15	140	75	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Preset or Reset Removal Time **	t_{rem}	5.0	650	325	–	ns
		10	230	115	–	
		15	180	90	–	
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
$\overline{\text{Carry In}}$ Setup Time	t_{su}	5.0	260	130	–	ns
		10	120	60	–	
		15	100	50	–	
Up/Down Setup Time	t_{su}	5.0	500	250	–	ns
		10	200	100	–	
		15	150	75	–	
Preset Enable Pulse Width	t_{WH}	5.0	200	100	–	ns
		10	100	50	–	
		15	80	40	–	

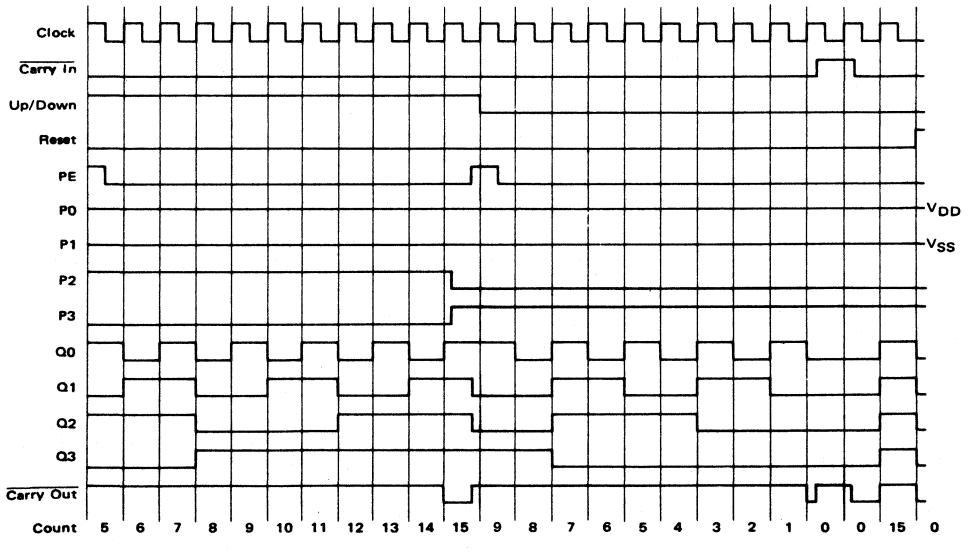
* The formulae given are for the typical characteristics only.

** The Preset or Reset signal must be low prior to a positive-going transition of the clock.

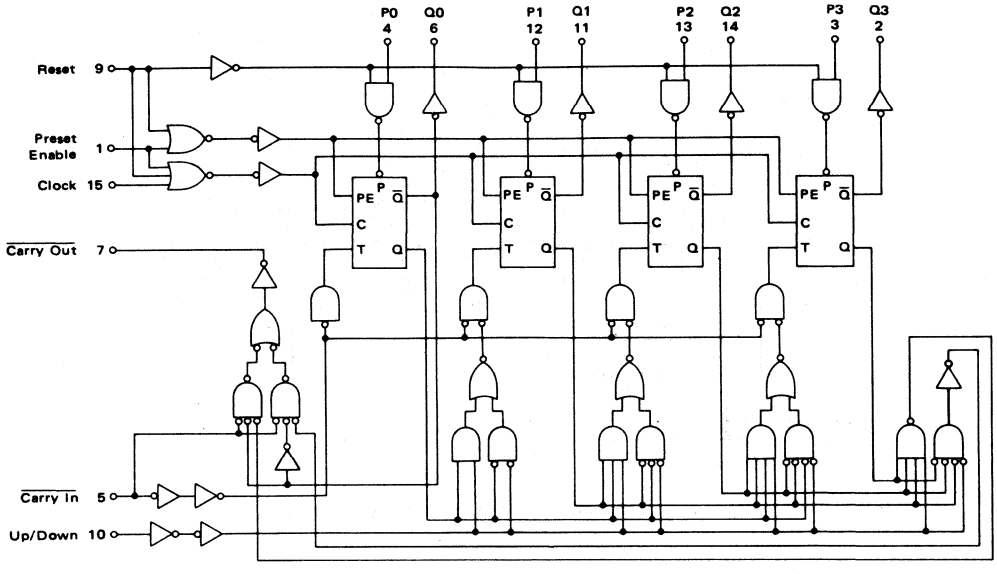
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



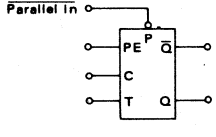
TIMING DIAGRAM



LOGIC DIAGRAM



TOGGLE FLIP-FLOP



FLIP-FLOP FUNCTIONAL TRUTH TABLE

PRESET ENABLE	CLOCK	T	Q_{n+1}
1	X	X	Parallel In
0	↑	0	Q_n
0	↑	1	$\overline{Q}_n$
0	↓	X	Q_n

X = Don't Care

FIGURE 2 – SWITCHING TIME WAVEFORMS

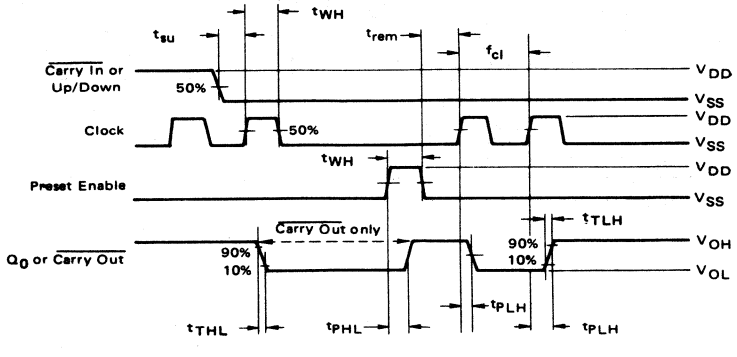


FIGURE 3 – PRESETTABLE CASCADED UP/DOWN COUNTER

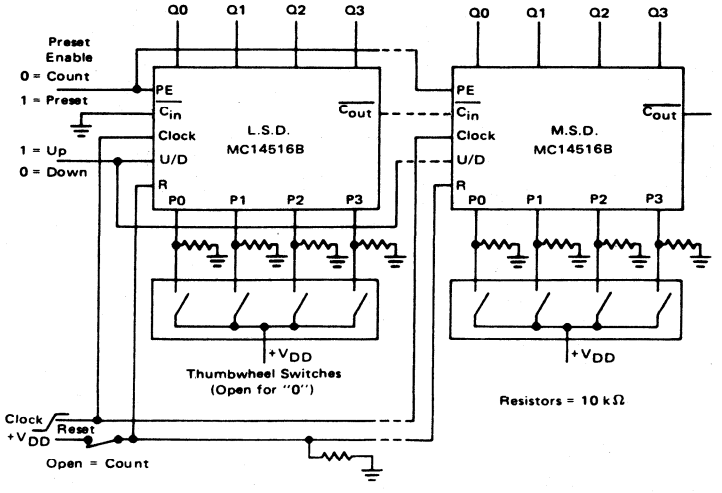
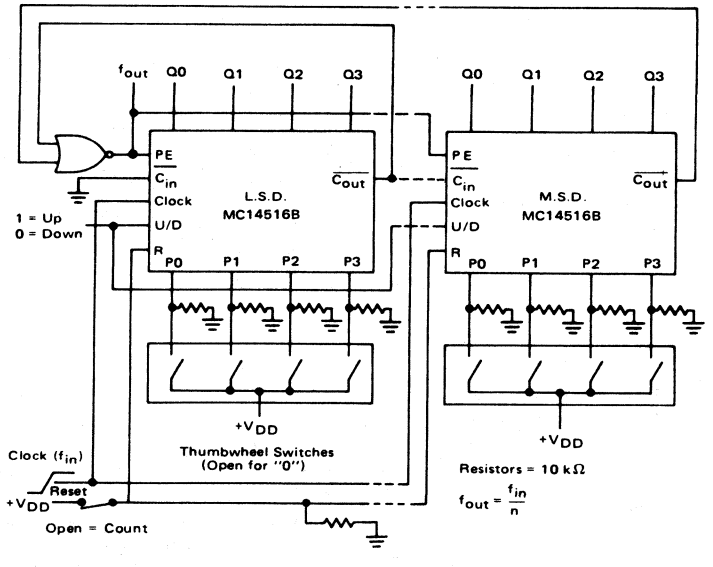


FIGURE 4 – PROGRAMMABLE CASCADED FREQUENCY DIVIDER



MOTOROLA

MC14517B

CMOS LSI

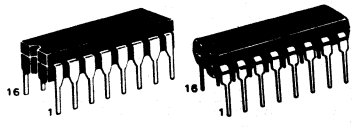
(LOW-POWER COMPLEMENTARY MOS)

DUAL 64-BIT STATIC SHIFT REGISTER

DUAL 64-BIT STATIC SHIFT REGISTER

The MC14517B dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Quiescent Current = 10 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- 6.7 MHz Operation @ V_{DD} = 10 Vdc
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3-State Output at 64th-Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



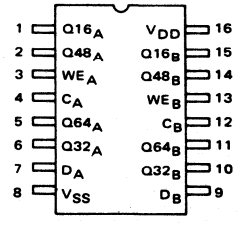
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FUNCTIONAL TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	16-BIT TAP	32-BIT TAP	48-BIT TAP	64-BIT TAP
0	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
⎍	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
⎍	1	Data entered into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 33-Bit	Data at tap entered into 49-Bit	High Impedance
⎎	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
⎎	1	X	High Impedance	High Impedance	High Impedance	High Impedance

X = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (4.2 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (8.8 µA/kHz) f + I_{DD}							
		15	I_T = (13.7 µA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 390 ns	t_{PHL}	5.0	–	475	770	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 177 ns		10	–	210	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	–	140	215	
Clock Pulse Width	t_{WH}	5.0	330	170	–	ns
		10	125	75	–	
		15	100	60	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	6.7	4.0	
		15	–	8.3	5.3	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	**See Note			–
		10				
		15				
Data to Clock Setup Time	t_{su}	5.0	0	-40	–	ns
		10	10	-15	–	
		15	15	0	–	
Data to Clock Hold Time	t_h	5.0	150	75	–	ns
		10	75	25	–	
		15	35	10	–	
Write Enable to Clock Setup Time	t_{su}	5.0	400	170	–	ns
		10	200	65	–	
		15	110	50	–	
Write Enable to Clock Release Time	t_{rel}	5.0	380	160	–	ns
		10	180	55	–	
		15	100	40	–	

* The formulae given are for the typical characteristics only.

* * When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less tha the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

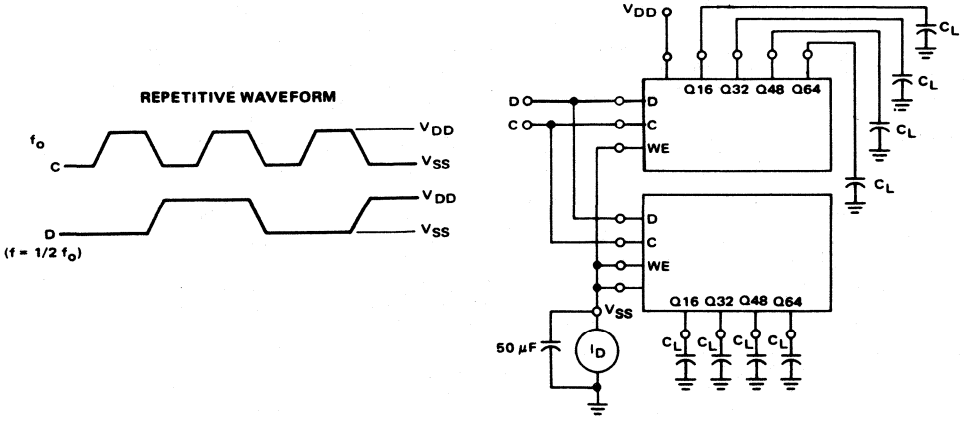
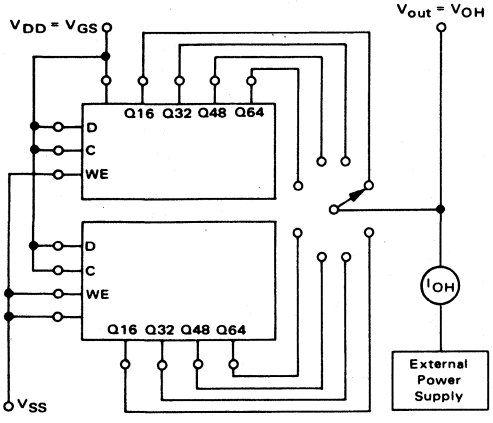
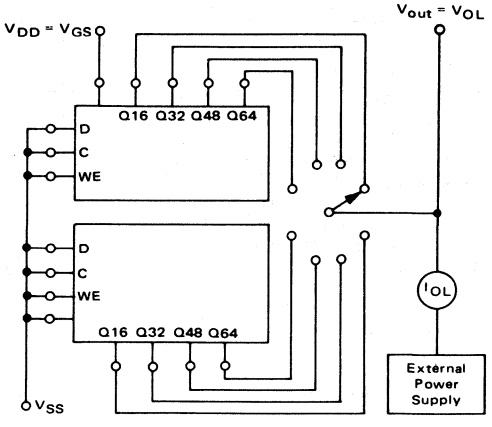


FIGURE 2 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT



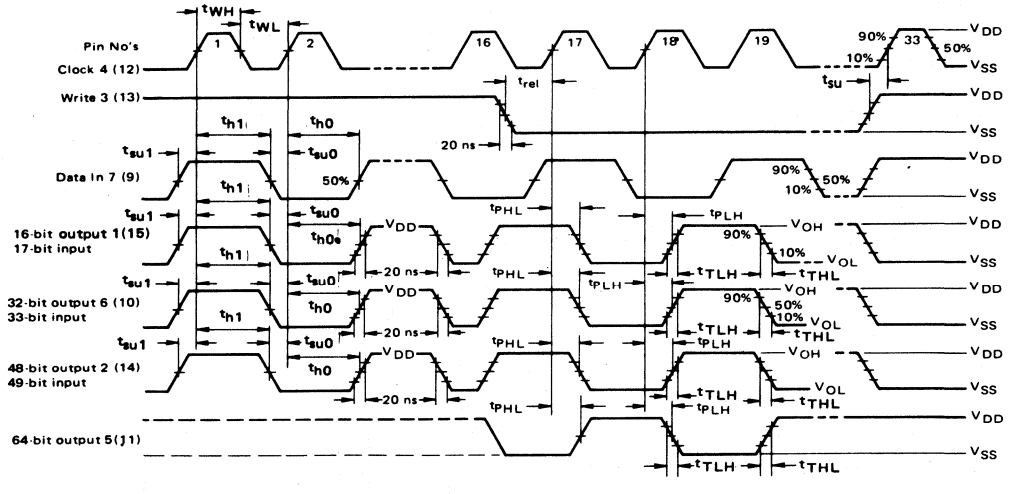
(Output being tested should be in the high-logic state).

FIGURE 3 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT

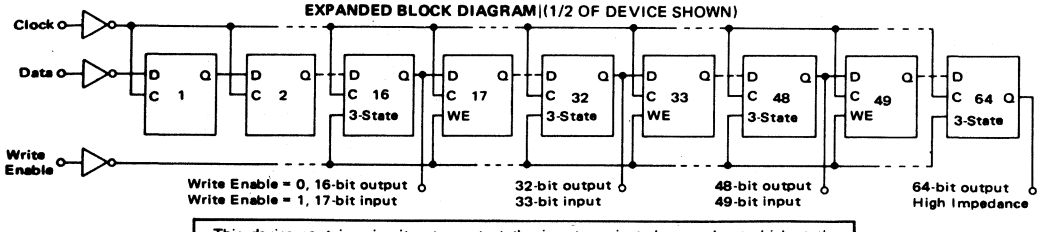


(Output being tested should be in the low-logic state).

FIGURE 4 – AC TEST WAVEFORMS



EXPANDED BLOCK DIAGRAM (1/2 OF DEVICE SHOWN)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14518B
MC14520B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

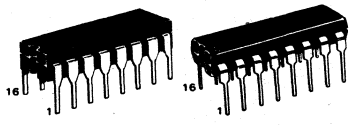
DUAL BCD UP COUNTER
(MC14518B)
DUAL BINARY UP COUNTER
(MC14520B)

3

DUAL UP COUNTERS

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



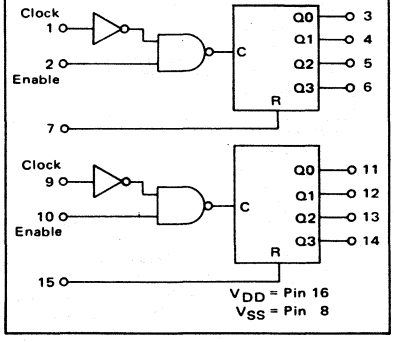
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.6 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.2 µA/kHz) f + I_{DD}							
		15	I_T = (1.7 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q/Enable to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	115	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	80	160	
Reset to Q						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	330	650	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	130	230	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 95 ns		15	–	90	170	
Clock Pulse Width	t_{WH}	5.0	200	100	–	ns
	t_{WL}	10	100	50	–	
		15	70	35	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.5	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Clock or Enable Rise and Fall Time	t_{THL}, t_{TLH}	5.0	–	–	15	µs
		10	–	–	5	
		15	–	–	4	
Enable Pulse Width	$t_{WH(E)}$	5.0	440	220	–	ns
		10	200	100	–	
		15	140	70	–	
Reset Pulse Width	$t_{WH(R)}$	5.0	280	125	–	ns
		10	120	55	–	
		15	90	40	–	

* The formulae given are for the typical characteristics only.

PIN ASSIGNMENT

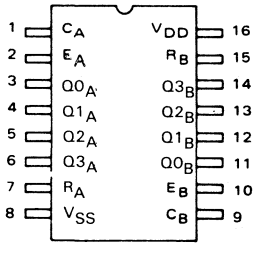


FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

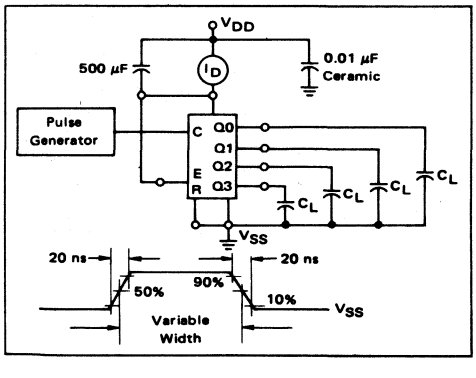
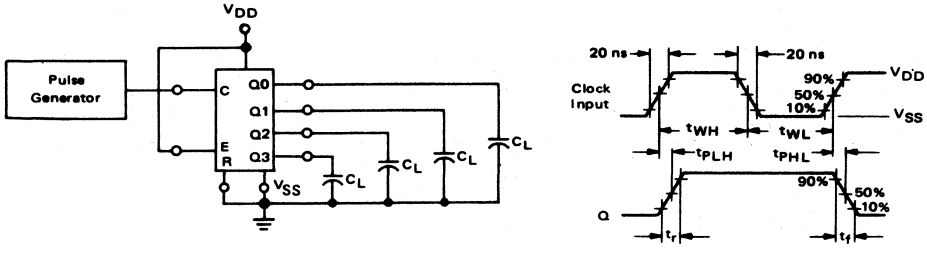


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



3

FIGURE 3 – TIMING DIAGRAM

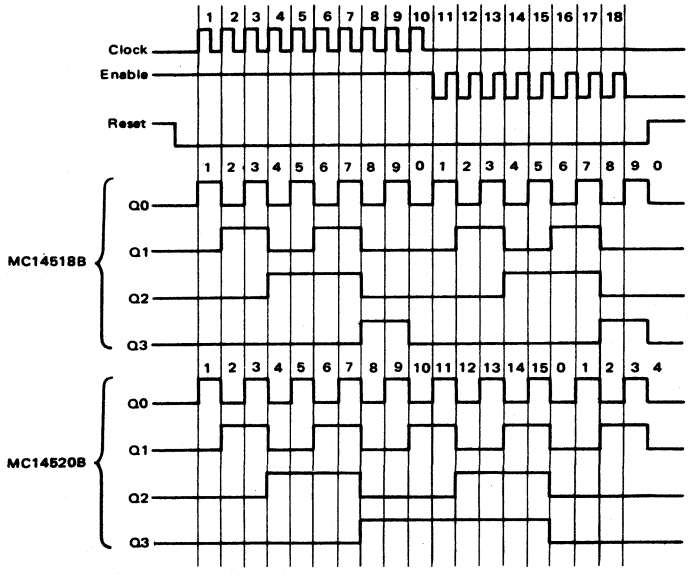


FIGURE 4 – DECADE COUNTER (MC14518B) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)

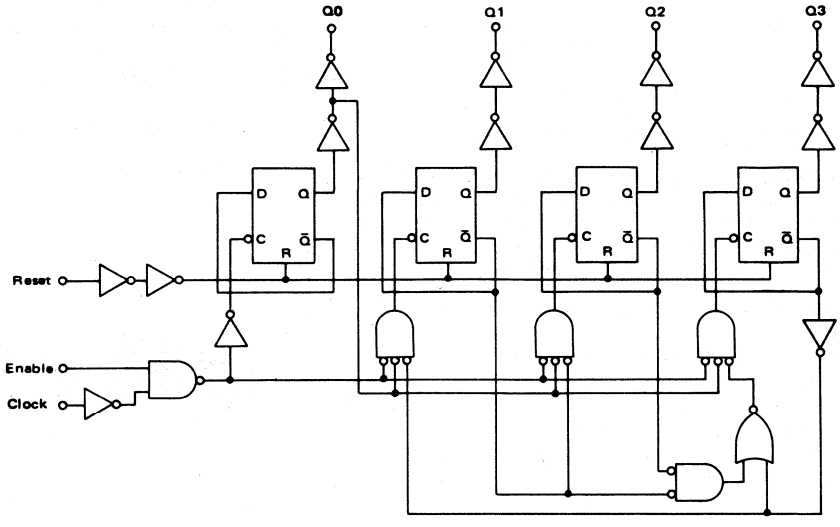
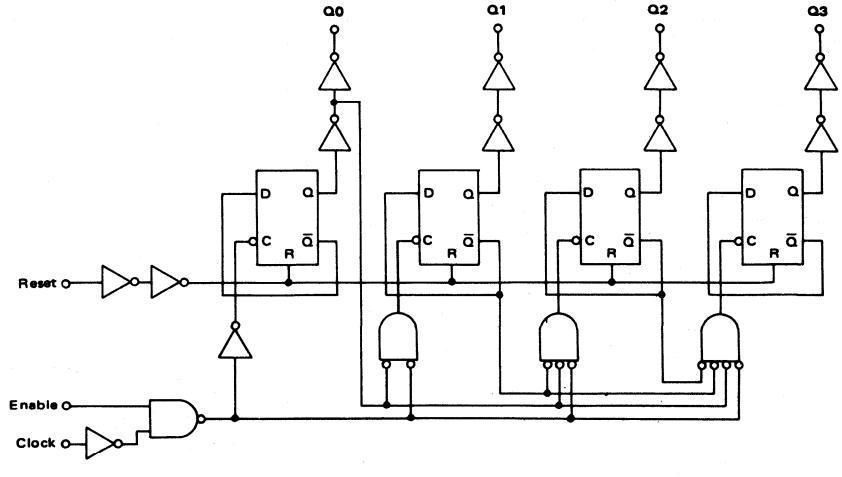


FIGURE 5 – BINARY COUNTER (MC14520B) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)



MOTOROLA

MC14519B

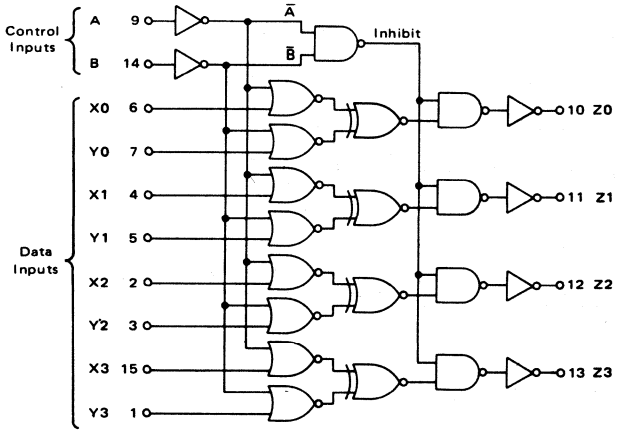
4-BIT AND/OR SELECTOR
or
QUAD 2-CHANNEL DATA SELECTOR
or
QUAD EXCLUSIVE "NOR" GATE

The MC14519B is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device exemplifies the design versatility of McMOS logic structure. This part provides three functions in one package; a 4-Bit AND/OR Selector, a Quad 2-Channel Data Selector, or a Quad Exclusive NOR Gate.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation — Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Plug-In Replacement for CD4019 in Most Applications

LOGIC DIAGRAM
(Positive Logic)

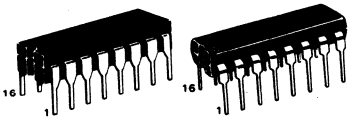


V_{DD} = Pin 16
V_{SS} = Pin 8

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

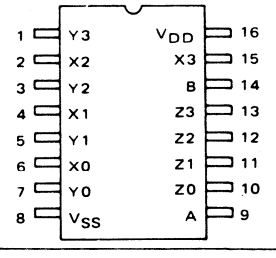
4-BIT AND/OR SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



TRUTH TABLE

CONTROL INPUTS		OUTPUT
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \circledcirc Y_n$

Note:
$X_n \circledcirc Y_n$ means X_n (Exclusive-NOR) Y_n

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.2 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.4 μA/kHz) f + I_{DD}							
		15	I_T = (3.6 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 165 hs		5.0	–	250	500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 82		10	–	115	225	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	165	

*The formulae given are for the typical characteristics only.

3

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

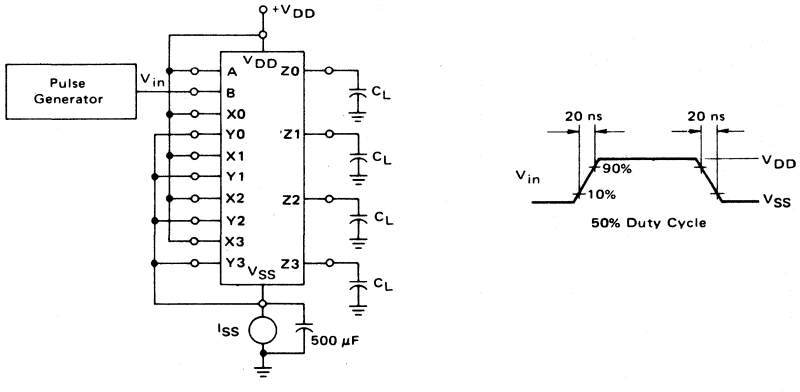
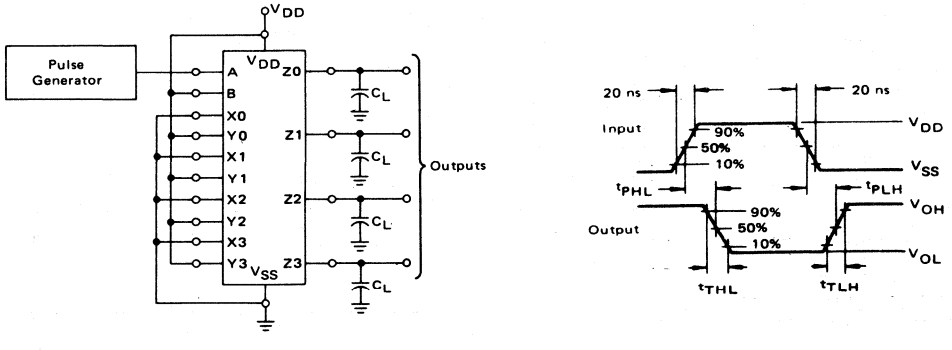
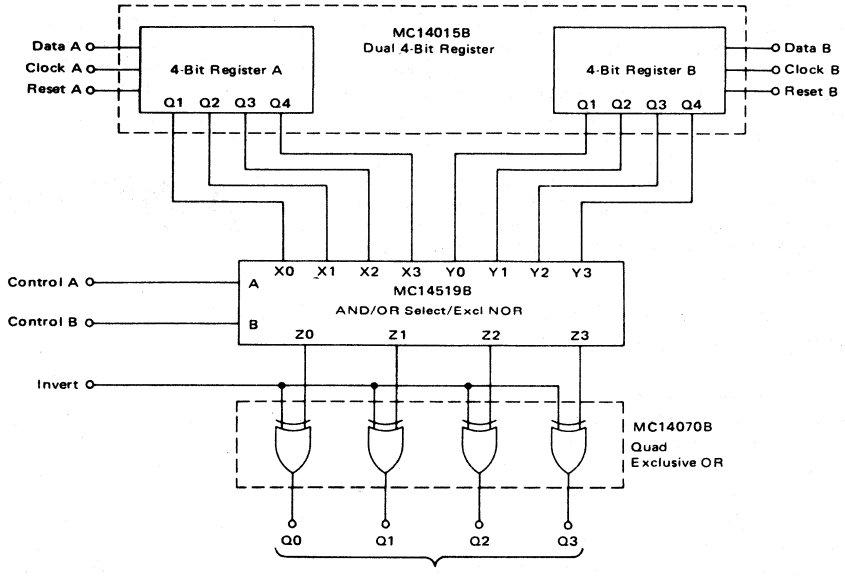


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TYPICAL CIRCUIT APPLICATIONS

DATA REGISTER SELECTION COMPARISON



CONVERSION TABLE

OPERATION CODE			OUTPUT				FUNCTION
A	B	INV	Q0	Q1	Q2	Q3	
0	0	0	0	0	0	0	Inhibit, all zeros
0	0	1	1	1	1	1	Inhibit, all ones
1	0	0	X0	X1	X2	X3	Control A
1	0	1	$\overline{X0}$	$\overline{X1}$	$\overline{X2}$	$\overline{X3}$	Control A and Invert
0	1	0	Y0	Y1	Y2	Y3	Control B
0	1	1	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	Control B and Invert
1	1	0	X0 ⊙ Y0	X1 ⊙ Y1	X2 ⊙ Y2	X3 ⊙ Y3	Exclusive NOR
1	1	1	X0 ⊕ Y0	X1 ⊕ Y1	X2 ⊕ Y2	X3 ⊕ Y3	Exclusive OR

MOTOROLA

MC14520B

FOR COMPLETE DATA
SEE MC14518B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

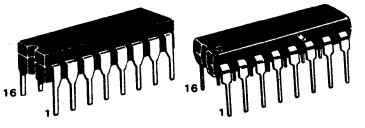
DUAL BCD UP COUNTER
(MC14518B)
DUAL BINARY UP COUNTER
(MC14520B)

3

DUAL UP COUNTERS

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



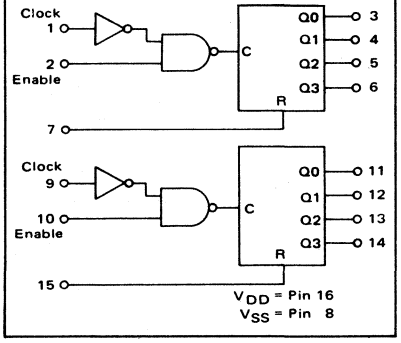
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
↓	X	0	No Change
X	↑	0	No Change
↑	0	0	No Change
1	↓	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MOTOROLA

MC14521B

CMOS MSI

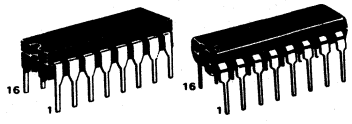
(LOW-POWER COMPLEMENTARY MOS)

24-STAGE FREQUENCY DIVIDER

24-STAGE FREQUENCY DIVIDER

The MC14521B consists of a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently this part will count up to 2^{24} = 16,777,216. The count advances on the negative going edge of the clock. The outputs of the last seven-stages are available for added flexibility.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- $f_{(max)}$ = 9.0 MHz typical @ V_{DD} = 10V
- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- V_{DD}' and V_{SS}' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low-Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

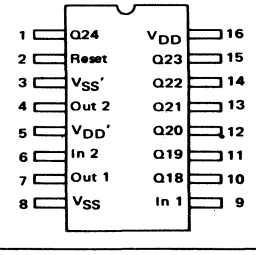
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

3

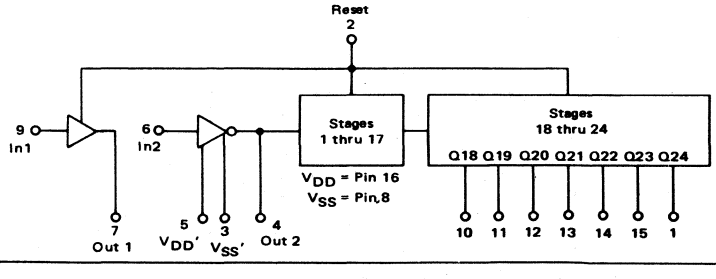
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN ASSIGNMENT



BLOCK DIAGRAM



OUTPUT	COUNT CAPACITY
Q18	2^{18} = 262,144
Q19	2^{19} = 524,288
Q20	2^{20} = 1,048,576
Q21	2^{21} = 2,097,152
Q22	2^{22} = 4,194,304
Q23	2^{23} = 8,388,608
Q24	2^{24} = 16,777,216

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.5	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage # "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	
(V_{OH} = 4.6 Vdc) Pins 4 & 7		5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
(V_{OH} = 9.5 Vdc)		10	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OH} = 13.5 Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	mAdc
(V_{OH} = 4.6 Vdc) Pins 1, 10,		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc) 11, 12, 13, 14		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc) and 15		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	−0.8	−1.7	–	−0.6	–	
(V_{OH} = 4.6 Vdc) Pins 4 & 7		5.0	−0.2	–	−0.16	−0.36	–	−0.12	–	
(V_{OH} = 9.5 Vdc)		10	−0.5	–	−0.4	−0.9	–	−0.3	–	
(V_{OH} = 13.5 Vdc)		15	−1.4	–	−1.2	−3.5	–	−1.0	–	
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	mAdc
(V_{OH} = 4.6 Vdc) Pins 1, 10,		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc) 11, 12, 13, 14		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc) and 15		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.42 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.85 µA/kHz) f + I_{DD}							
		15	I_T = (1.4 µA/kHz) f + I_{DD}							

* T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

\# Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

† To calculate total supply current at loads other than 50 pF: I_T (C_L) = I_T (50 pf) + 3×10^{-3} (C_L-50) V_{DD}f.
where: I_T is in µA (Per Package) C_L in pF, V_{DD} in Vdc and f in kHz is input frequency.

** The formulae given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time (Counter Outputs)	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time (Counter Outputs)	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	110	
t_{THL} = (0.55 ns/pF) C_L + 12.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					µs
Clock to Q18	t_{PHL}					
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 4415 ns		5.0	–	4.5	9.0	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 1667 ns		10	–	1.7	3.5	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 1275 ns		15	–	1.3	2.7	
Clock to Q24						µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns		5.0	–	6.0	12	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2167 ns		10	–	2.2	4.5	
t_{PHL}, t_{PHL} = (0.5 ns/pF) C_L + 1675 ns		15	–	1.7	3.5	
Propagation Delay Time	t_{PHL}					ns
Reset to Q_n						
t_{PHL} = (1.7 ns/pF) C_L + 1215 ns		5.0	–	1300	2600	
t_{PHL} = (0.66 ns/pF) C_L + 467 ns		10	–	500	1000	
t_{PHL} = (0.5 ns/pF) C_L + 350 ns		15	–	375	750	
Clock Pulse Width	$t_{WH(cl)}$	5.0	385	140	–	ns
		10	150	55	–	
		15	120	40	–	
Clock Pulse Frequency	f_{cl}	5.0	–	3.5	2.0	MHz
		10	–	9.0	5.0	
		15	–	12	6.5	
Clock Rise and Fall Time	t_{TLH},	5.0	–	–	15	µs
	t_{THL}	10	–	–	5	
		15	–	–	4	
Reset Pulse Width	$t_{WH(R)}$	5.0	1400	700	–	ns
		10	600	300	–	
		15	450	225	–	

*The formulae given are for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

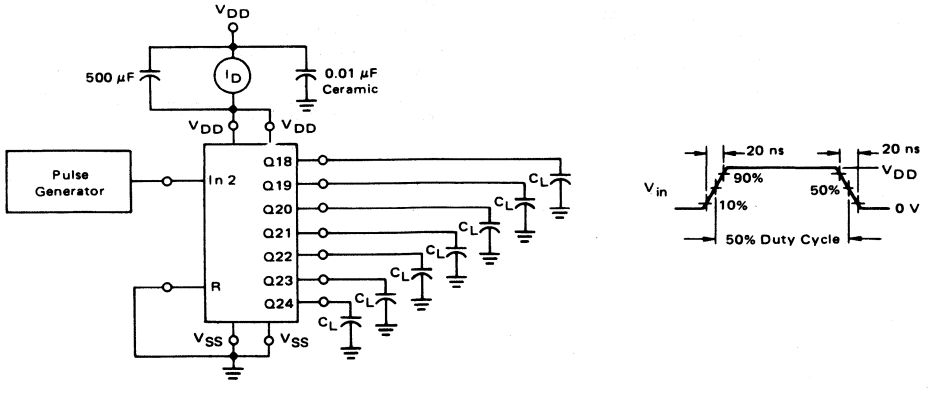
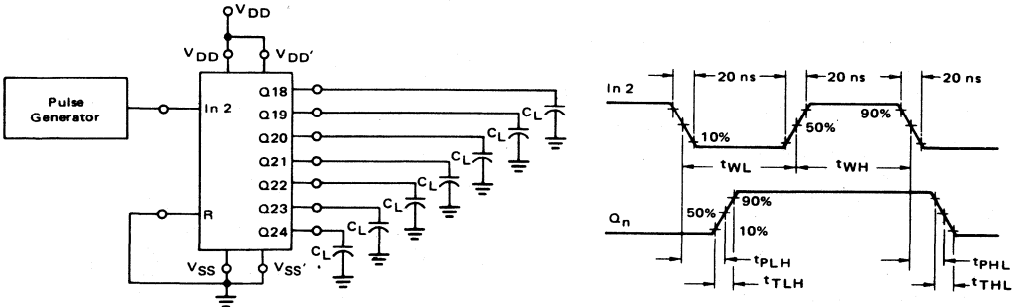
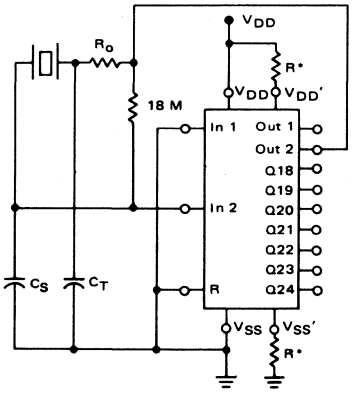


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



3

FIGURE 3 – CRYSTAL OSCILLATOR CIRCUIT



*Optional for low power operation.
10 kΩ ≤ R ≤ 70 kΩ

FIGURE 4 – TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

CHARACTERISTIC	500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Equivalent Resistance, R_S	1.0	6.2	kΩ
External Resistor/Capacitor Values			
R_o	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Change as a Function of V_{DD} (T_A = 25°C)			
V_{DD} Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V_{DD} Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature (V_{DD} = 10 V)			
T_A Change from -55°C to +25°C			
MC14521 only	-4.0	-2.0	ppm
Complete Oscillator*	+100	+120	ppm
T_A Change from +25°C to +125°C			
MC14521 only	-2.0	-2.0	ppm
Complete Oscillator*	-160	-560	ppm

*Complete oscillator includes crystal, capacitors, and resistors.

FIGURE 5 – RC OSCILLATOR STABILITY

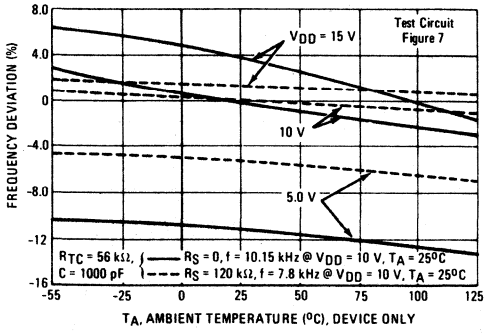


FIGURE 6 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C

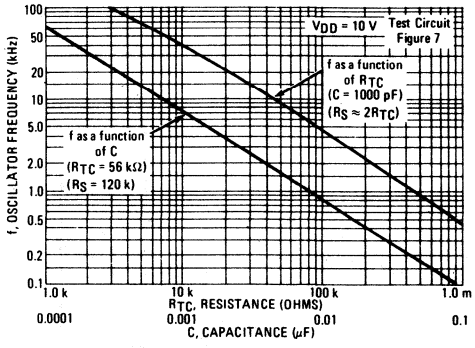


FIGURE 7 – RC OSCILLATOR CIRCUIT

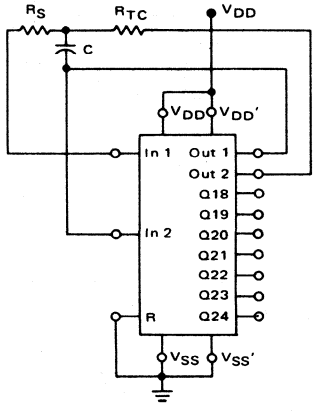
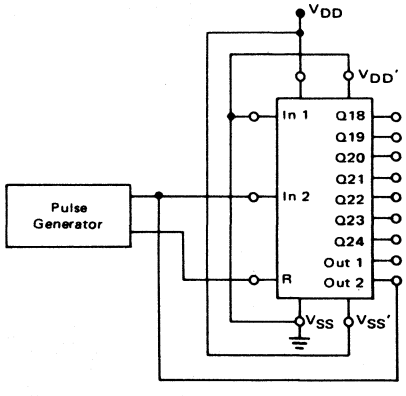


FIGURE 8 – FUNCTIONAL TEST CIRCUIT

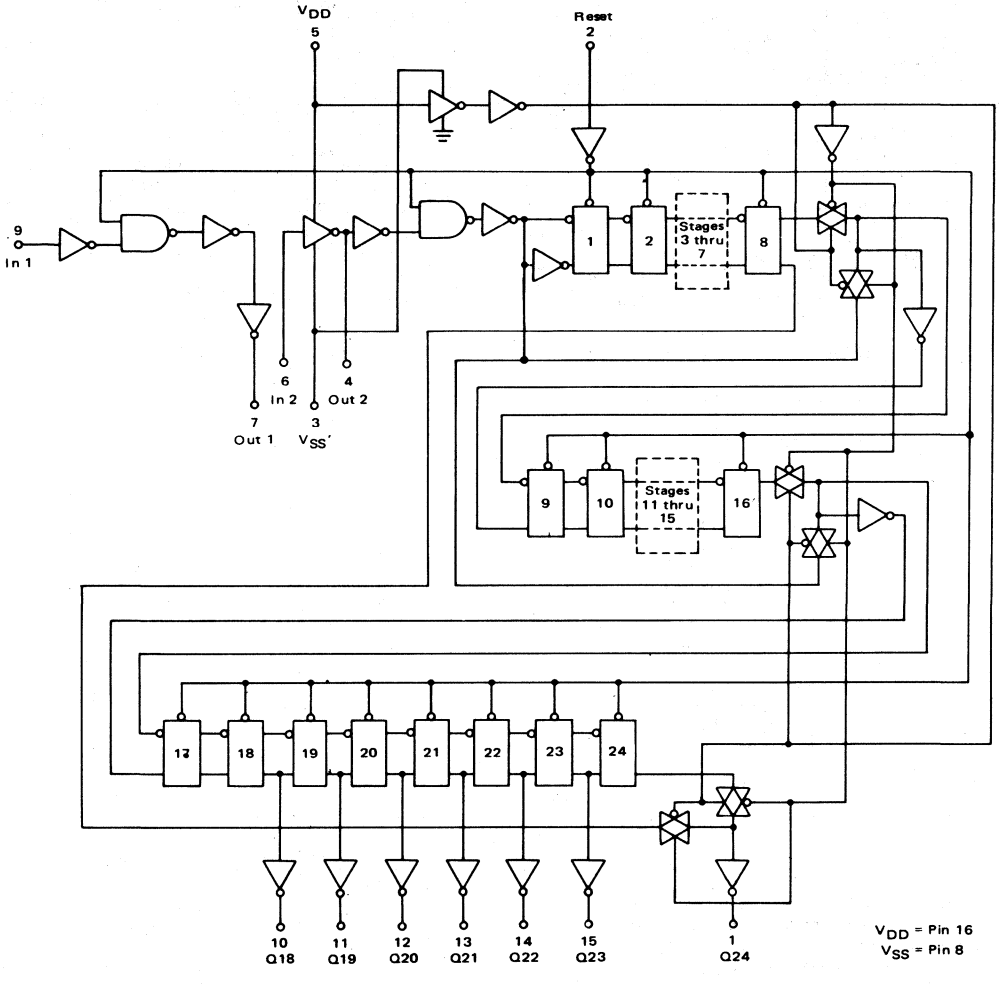


FUNCTIONAL TEST SEQUENCE

A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections, and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all "1" state to an all "0" state.

INPUTS		OUTPUTS				COMMENTS
Reset	In 2	Out 2	V_{SS}'	V_{DD}'	Q18 thru Q24	
1	0	0	V_{DD}	Gnd	0	Counter is in three 8-stage sections in parallel mode Counter is reset. In 2 and Out 2 are connected together
0	1	1				First "0" to "1" transition on In 2, Out 2 node.
	0	0				255 "0" to "1" transitions are clocked into this In 2, Out 2 node.
	1	1				
	–	–				
	–	–				
	–	–				
	1	1			1	The 255th "0" to "1" transition.
	0	0			1	
	0	0	Gnd		1	
	1	0		V_{DD}	1	Counter converted back to 24-stages in series mode.
	1				1	Out 2 converts back to an output.
	0				0	Counter ripples from an all "1" state to an all "0" stage.

LOGIC DIAGRAM



MOTOROLA

MC14522B
MC14526B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

BCD – MC14522B
Binary – MC14526B

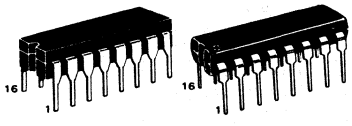
PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

The MC14522B BCD counter and the MC14526B binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure.

These devices are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Clock Inhibit input allows disabling of the pulse counting function.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds.
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition of Clock Inhibit
- 5.0 MHz Counting Rate
- Asynchronous Preset Enable
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

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- L Ceramic Package
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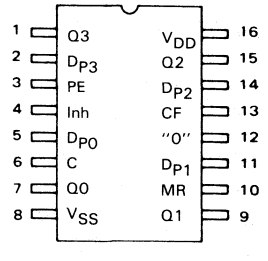
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN ASSIGNMENT



TRUTH TABLES

BOTH TYPES

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
↓	0	0	0	Count-1
X	1	0	0	No Count
1	↓	0	0	Count-1
X	X	1	0	Preset
X	X	X	1	Reset

MC14522B

Count	Output Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC14526B

Count	Output Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0'	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.7 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.4 μA/kHz) f + I_{DD}							
		15	I_T = (5.1 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 9.5 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Q Outputs						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	550	1100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	225	450	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	–	160	320	
"0" Output						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 155 ns		5.0	–	240	480	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	100	200	
Minimum Clock Pulse Width	$t_{WH(cl)}$	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	
Maximum Clock Pulse Frequency (with PE = low)	f_{cl}	5.0	–	2.0	1.5	MHz
		10	–	5.0	3.0	
		15	–	6.6	4.0	
Maximum Clock or Inhibit Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	µs
		10	–	–	5	
		15	–	–	4	
Hold Time	t_h	5.0	150	75	–	ns
		10	50	25	–	
		15	40	20	–	
Minimum Preset Enable Pulse Width	$t_{WH(PE)}$	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	
Minimum Master Reset Pulse Width	$t_{WH(R)}$	5.0	350	175	–	ns
		10	250	125	–	
		15	200	100	–	

* The formulae given are for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

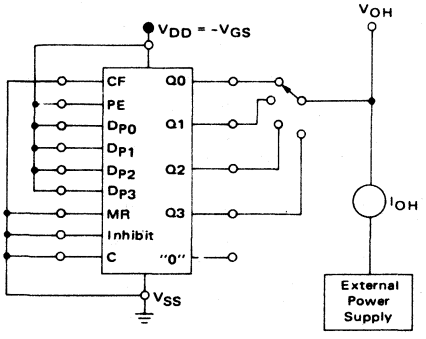
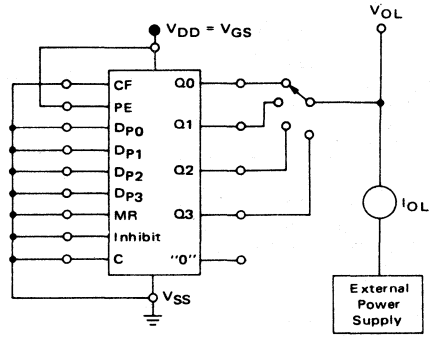


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



3

FIGURE 3 – POWER DISSIPATION

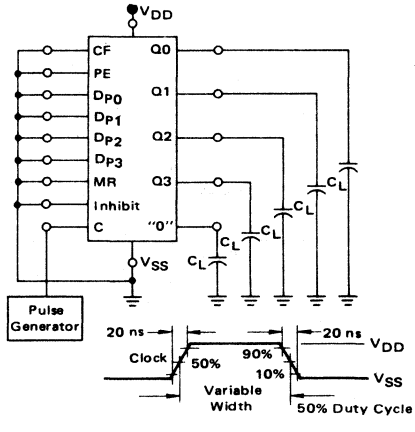
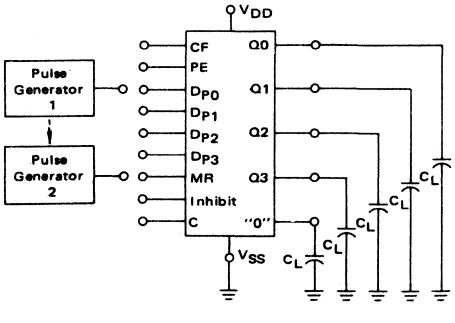


FIGURE 4 – AC TEST CIRCUITS

A) TEST NOS. 1 – 6



B) TEST NO. 7

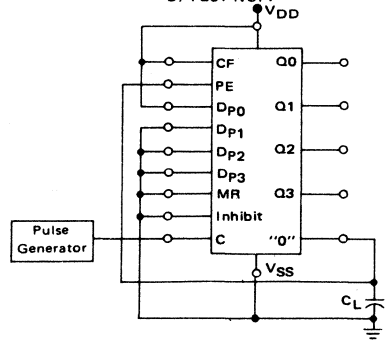
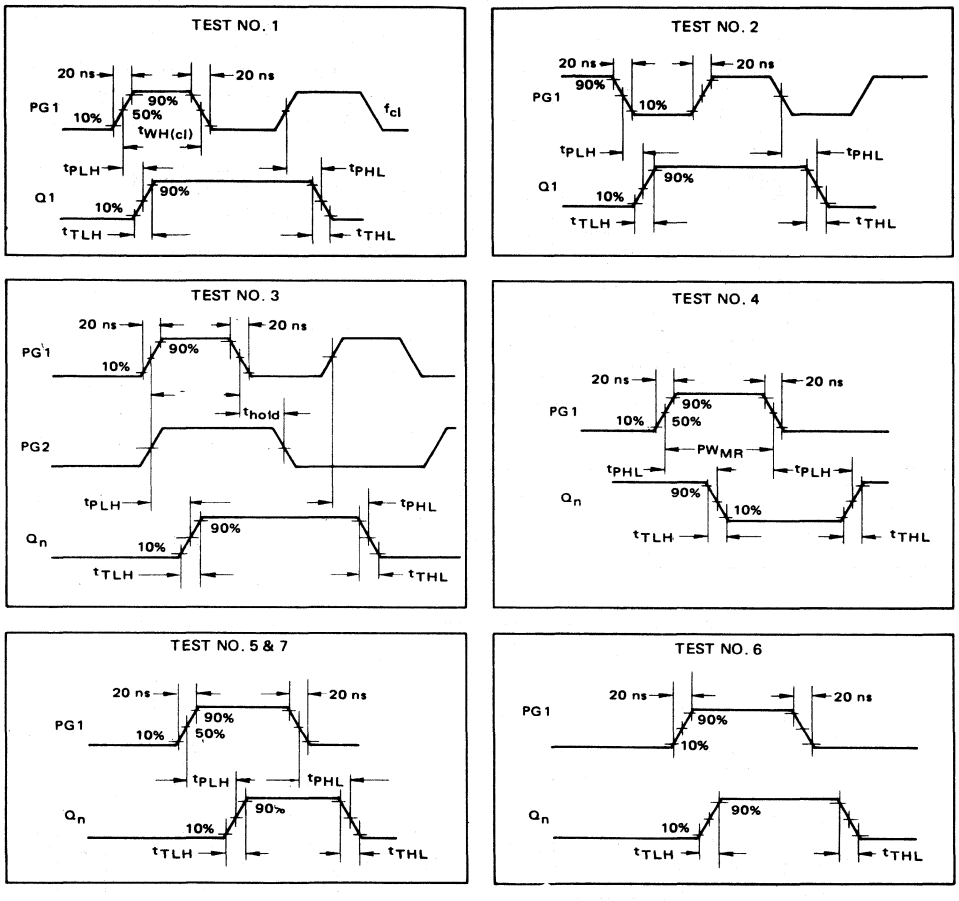


FIGURE 5 – AC TEST CONNECTIONS AND WAVEFORMS



CHARACTERISTIC	TEST NO.	CLOCK	INHIBIT	PE	MR	D_{Pn}	CF	OUTPUT
t_{TLH}, t_{THL}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	2	V_{DD}	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
	5	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	V_{SS}	Q_n
$t_{WH(R)}$	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
$t_{WH(PE)}$	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
$t_{WH(cl)}$	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
f_{cl}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
t_h	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
t_{TLH}, t_{THL}	6	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	"0"
t_{PLH}, t_{PHL}	7	PG	V_{SS}	Fig 4B	V_{SS}	Fig 4B	V_{DD}	"0"

FIGURE 6 – MC14522B LOGIC DIAGRAM (BCD Divide-by-N Counter)

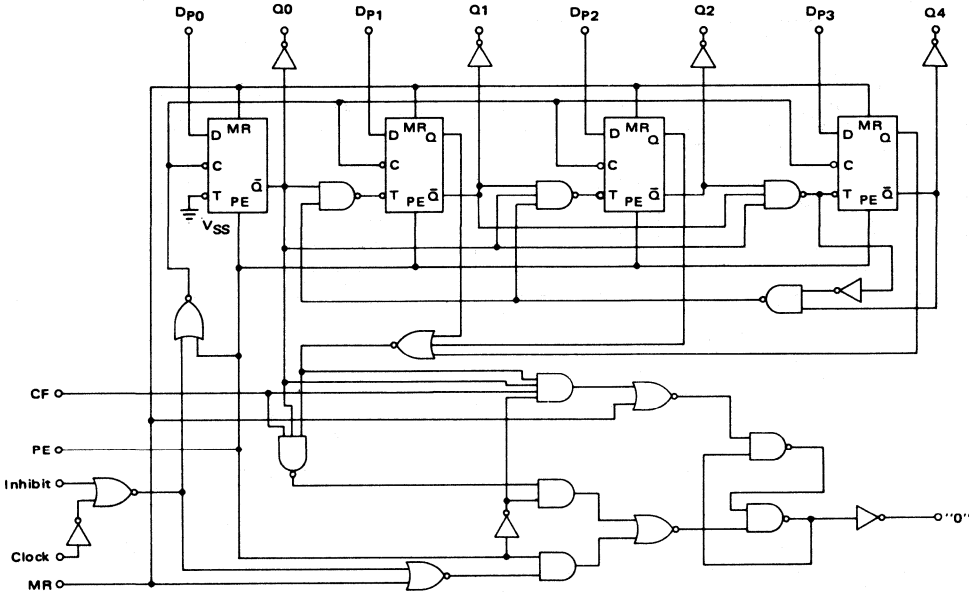


FIGURE 7 – MC14526B LOGIC DIAGRAM (Binary Divide-by-N Counter)

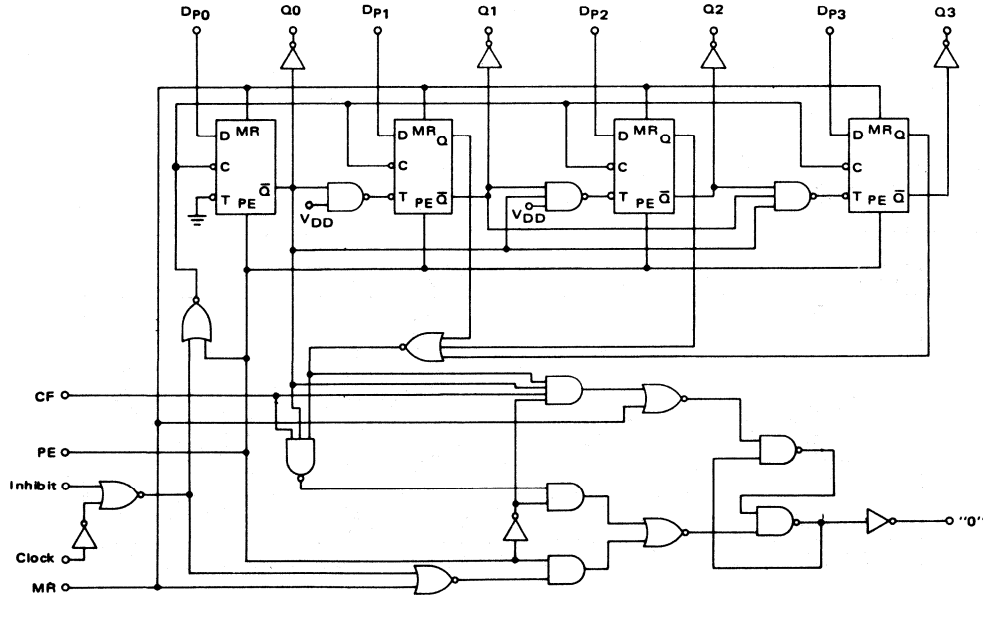
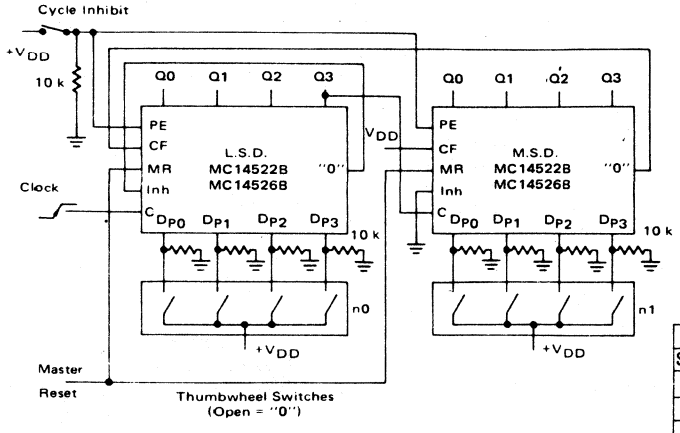
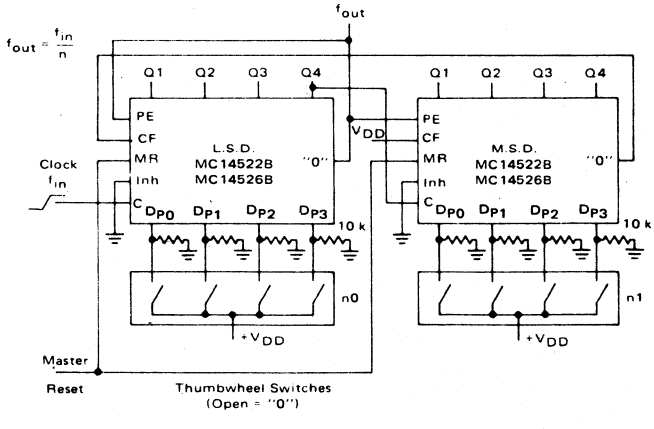


FIGURE 8 – 2-STAGE PROGRAMMABLE DOWN COUNTER
(One Cycle)



From		To		Range of N
Stage	Pin	Stage	Pin	
LSD	"0"	All	PE	LSD ≤ N ≤ MSD
N	"0"	N-1	CF	LSD+1≤N≤ MSD
N	"$\overline{0}_3$"	N+1	C	LSD ≤ N ≤ MSD-1

FIGURE 9 – 2-STAGE PROGRAMMABLE FREQUENCY DIVIDER



From		To		Range of N
Stage	Pin	Stage	Pin	
LSD	"0"	All	PE	LSD ≤ N ≤ MSD
N	"0"	N-1	CF	LSD+1≤N≤ MSD
N	"$\overline{0}_3$"	N+1	C	LSD ≤ N ≤ MSD-1

MOTOROLA

MC14527B

BCD RATE MULTIPLIER

The MC14527B BCD rate multiplier (DRM) provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten input pulses. This part may be used for arithmetic operations including multiplication and division. Typical applications include digital filters, motor speed control and frequency synthesizers.

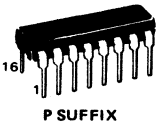
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance — 5.0 pF typical
- Internally Synchronous for High Speed
- Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and Cascade Inputs for Cascade Operation of Two or More DRMs
- "9" Output for the Parallel Enable Configuration and DRMs in Cascade
- Complementary Outputs
- Clear and Set to Nine Inputs

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD RATE MULTIPLIER

L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

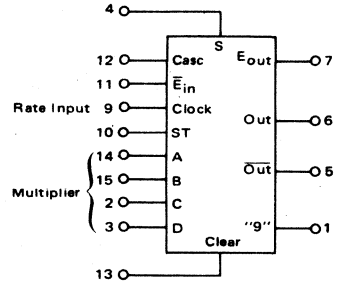
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS										OUTPUT LOGIC LEVEL NUMBER OF PULSES			
D	C	B	A	No. of Clock Pulses	$\overline{E}_{in}$	STROBE	CASCADE	CLEAR	SET	OUT	$\overline{OUT}$	E_{out}	"9"
0	0	0	0	10	0	0	0	0	0	0	1	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	—	—	—	—
X	X	X	X	10	0	1	0	0	0	0	1	1	1
X	X	X	X	10	0	0	1	0	0	1	0	1	1
1	X	X	X	10	0	0	0	1	0	10	10	1	0
0	X	X	X	10	0	0	0	1	0	0	1	1	0
X	X	X	X	10	0	0	0	0	1	0	1	0	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

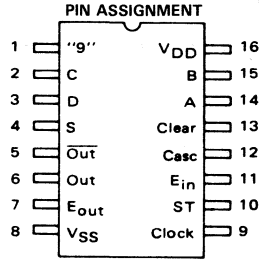
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.85 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.75 μA/kHz) f + I_{DD}							
		15	I_T = (2.6 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1.2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PHL}, t_{PHL}					ns
Clock to Out						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 115 ns		5.0	–	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	140	
Clock to Out	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 40 ns		5.0	–	125	250	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 32 ns		10	–	65	130	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 20 ns		15	–	45	90	
Clock to E_{out}	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 210 ns		5.0	–	295	590	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	–	85	170	
Clock to "9"	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns		5.0	–	400	800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 122 ns		10	–	155	310	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Set or Clear to Out	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 295 ns		5.0	–	380	760	
t_{PHL} = (0.66 ns/pF) C_L + 132 ns		10	–	165	330	
t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Cascade to Out	t_{PLH}					ns
t_{PHL} = (1.7 ns/pF) C_L + 40 ns		5.0	–	125	250	
t_{PHL} = (0.66 ns/pF) C_L + 32 ns		10	–	65	130	
t_{PHL} = (0.5 ns/pF) C_L + 20 ns		15	–	45	90	
Strobe to Out	t_{PLH}					ns
t_{PHL} = (1.7 ns/pF) C_L + 145 ns		5.0	–	230	260	
t_{PHL} = (0.66 ns/pF) C_L + 72 ns		10	–	105	210	
t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	140	
Clock Pulse Width	t_{WH}	5.0	500	250	–	ns
		10	200	110	–	
		15	150	80	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.0	1.2	MHz
		10	–	4.5	2.5	
		15	–	6.0	3.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
Set or Clear Pulse Width	t_{WH}	5.0	240	80	–	ns
		10	100	35	–	
		15	75	30	–	
Set Removal Time	t_{rem}	5.0	0	-20	–	ns
		10	0	-10	–	
		15	0	-7.5	–	
Enable In Setup Time	t_{su}	5.0	400	175	–	ns
		10	150	60	–	
		15	120	45	–	

* The formulae given are for the typical characteristics only.

FIGURE 1 – TEST CIRCUIT AND TIMING DIAGRAM

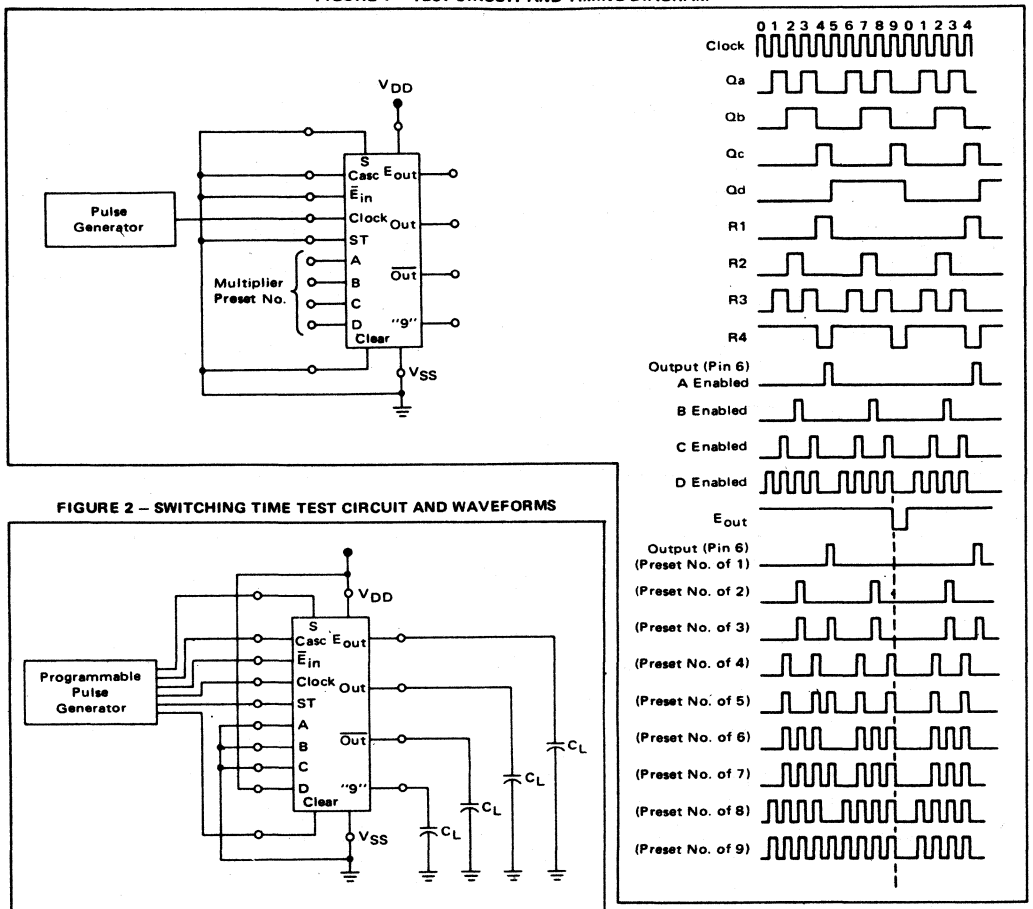


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

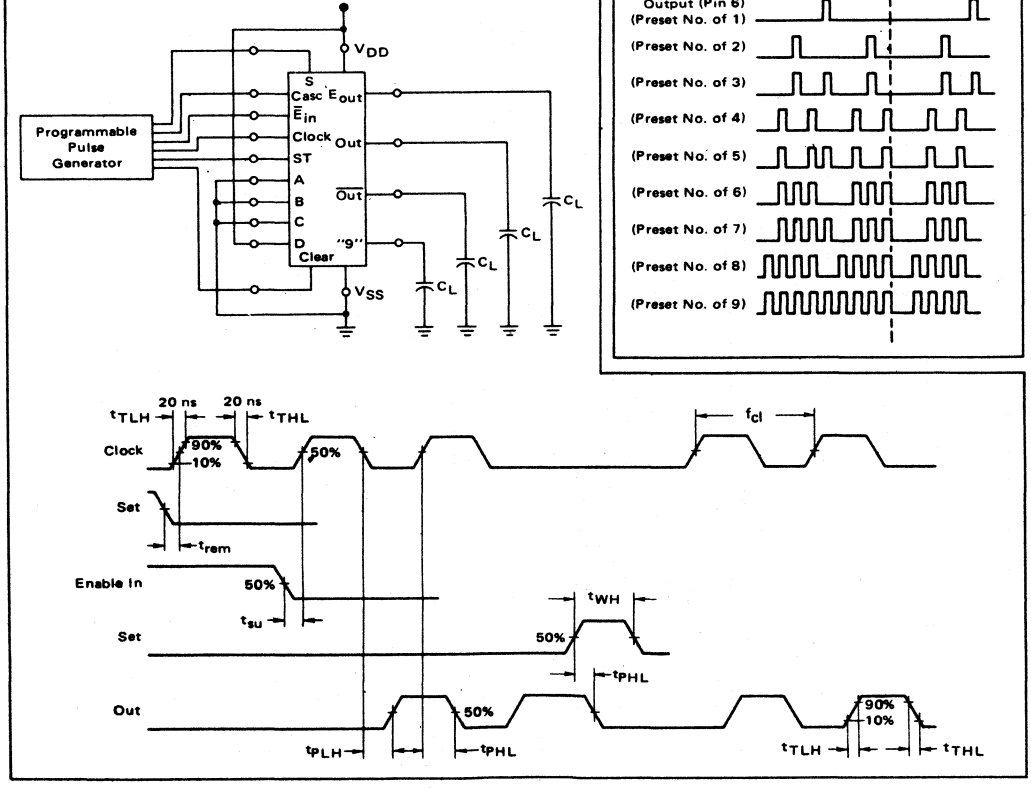
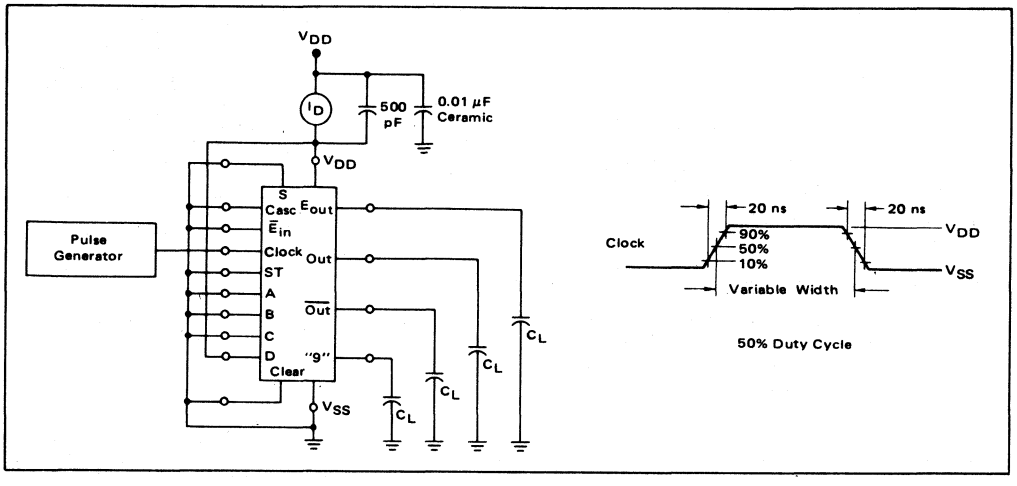


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



LOGIC DIAGRAM

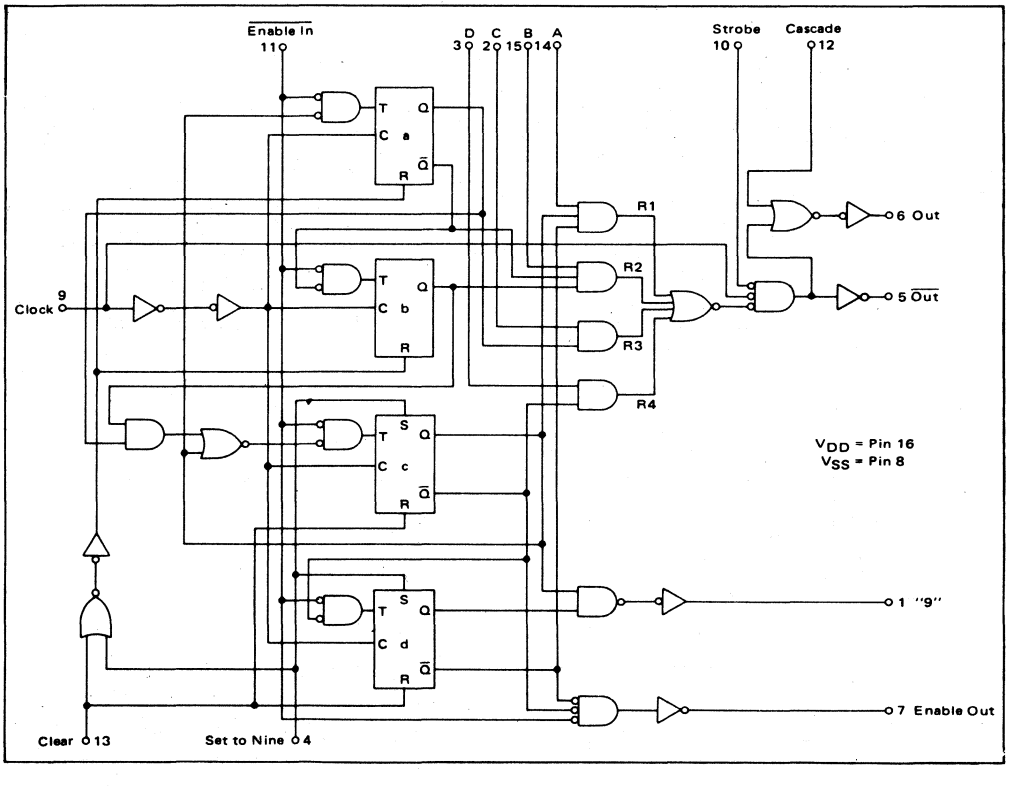
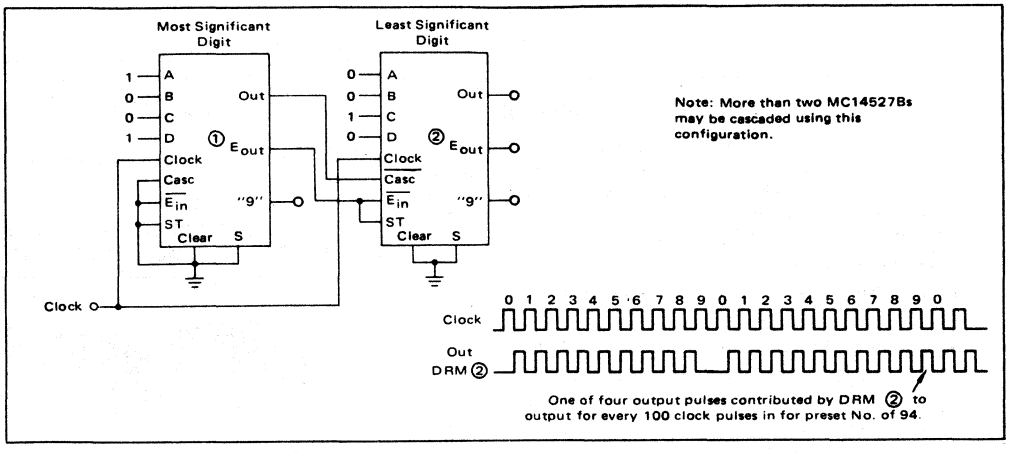


FIGURE 4 – TWO MC14527Bs IN CASCADE WITH PRESET NO. of 94



3

MOTOROLA

MC14528B

CMOS MSI

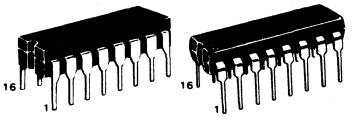
(LOW-POWER COMPLEMENTARY MOS)

DUAL RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

DUAL MONOSTABLE MULTIVIBRATOR

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

- Separate Reset Available
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- For Pulse Width Greater than 1.0 μS, the MC14548B Is Recommended



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

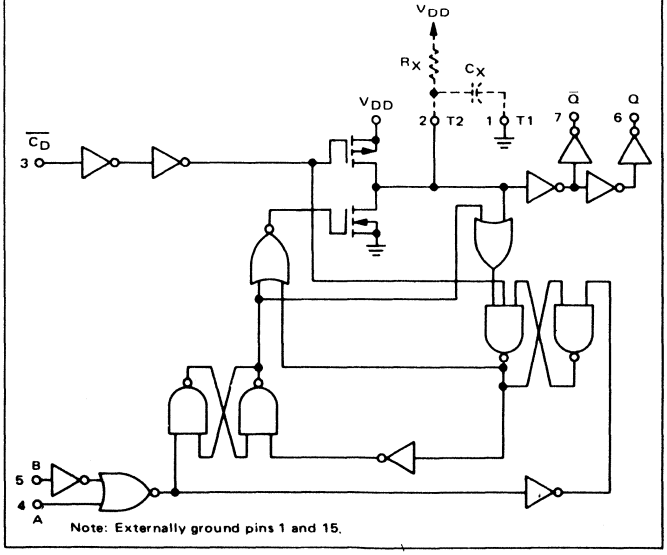
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

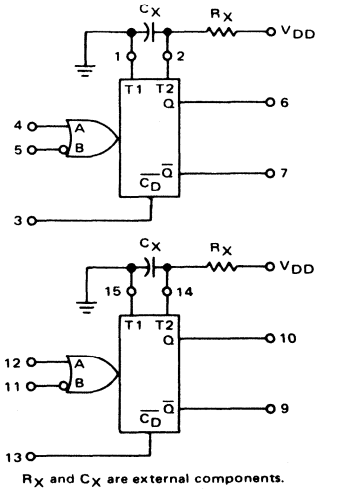
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM
(1/2 of Device Shown)



Note: Externally ground pins 1 and 15.

BLOCK DIAGRAM



R_X and C_X are external components.
V_{DD} = Pin 16
V_{SS} = Pin 8, Pin 1, Pin 15

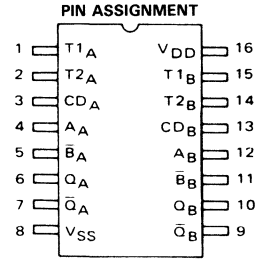
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	−0.8	−0.7	–	−0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
**Total Supply Current at an external load Capacitance (C_L) and at external timing capacitance (C_X), use the formula –	I_T	–	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2\times10^{-8} R_X C_X(V_{DD}-2)^2 f] \times 10^{-3}$ where: I_T in μA (per circuit), C_L and C_X in pF, R_X in megohms, V_{DD} in Vdc, f in kHz is input frequency.							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS** (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	–	–					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns				5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns				10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns				15	–	40	80	
Output Fall Time	t_{THL}	–	–					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns				5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns				10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns				15	–	40	80	
Turn-Off, Turn-On Delay Time – A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 240 ns				5.0	–	325	650	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns				10	–	120	240	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns				15	–	90	180	
Turn-Off, Turn-On Delay Time – A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	1000	10					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 620 ns				5.0	–	705	–	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns				10	–	290	–	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns				15	–	210	–	
Input Pulse Width – A or B	t_{WH}	15	5.0	5.0	150	70	–	ns
				10	75	30	–	
				15	55	30	–	
	t_{WL}	1000	10	5.0	–	70	–	ns
				10	–	30	–	
				15	–	30	–	
Output Pulse Width – Q or $\overline{Q}$ (For C_X < 0.01 μF use graph for appropriate V_{DD} level.)	t_W	15	5.0	5.0	–	550	–	ns
				10	–	350	–	
				15	–	300	–	
Output Pulse Width – Q or $\overline{Q}$ (For C_X > 0.01 μF use formula: $t_W = 0.2\ R_X\ C_X\ \text{Ln}\ [V_{DD} - V_{SS}]$)†	t_W	10,000	10	5.0	–	30	±15	μs
				10	–	50	±40	
				15	–	55	±40	
Pulse Width Match between Circuits in the same package	t1 - t2	10,000	10	5.0	–	6.0	25	%
				10	–	8.0	35	
				15	–	8.0	35	
Reset Propagation Delay – C_D to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0	5.0	–	325	600	ns
				10	–	90	225	
				15	–	60	170	
		1000	10	5.0	–	1000	–	ns
				10	–	300	–	
				15	–	250	–	
Retrigger Time	t_{rr}	15	5.0	5.0	0	–	–	ns
				10	0	–	–	
				15	0	–	–	
		1000	10	5.0	0	–	–	ns
				10	0	–	–	
				15	0	–	–	
						Min		
External Timing Resistance	R_X	–	–	–	5.0	1000	1000	kΩ
External Timing Capacitance	C_X	–	–	–	No Limits *			μF

** The formulae given are for the typical characteristics only.

† R_X is in Ohms, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.

* If C_X > 15 μF, Use Discharge Protection Diode D_X, per Fig. 7.

FUNCTION TABLE

Inputs			Outputs	
Reset	A	B	Q	$\overline{Q}$
H	↓	H	⊓	⊔
H	L	↓	⊓	⊔
H	↓, ↑	L	Not Triggered	
H	H	↓, ↑	Not Triggered	
H	L, H, ↑	H	Not Triggered	
H	L	L, H, ↓	Not Triggered	
L	X	X	L	H
↑↓	X	X	Not Triggered	

FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT

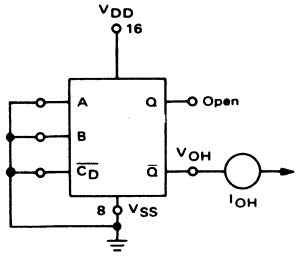


FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT

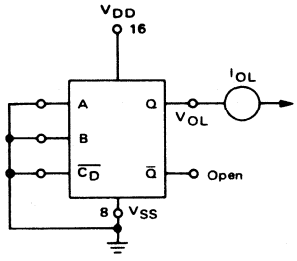
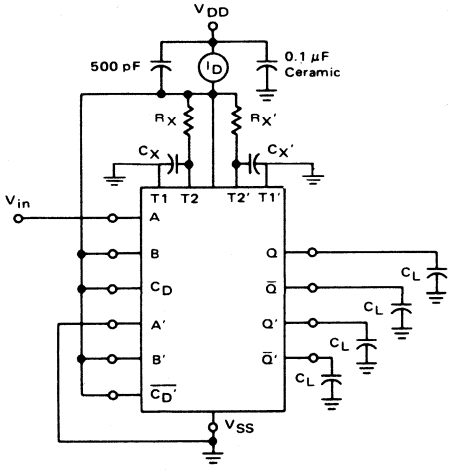
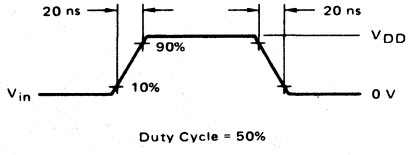


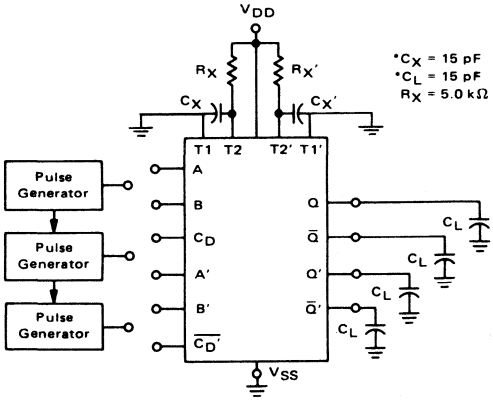
FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS





Duty Cycle = 50%

FIGURE 4 – AC TEST CIRCUIT



INPUT CONNECTIONS

CHARACTERISTICS	C_D	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} t_W	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} t_W	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_W	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: AC test waveforms for PG1, PG2, and PG3 on next page.

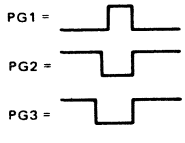


FIGURE 5 — AC TEST WAVEFORMS

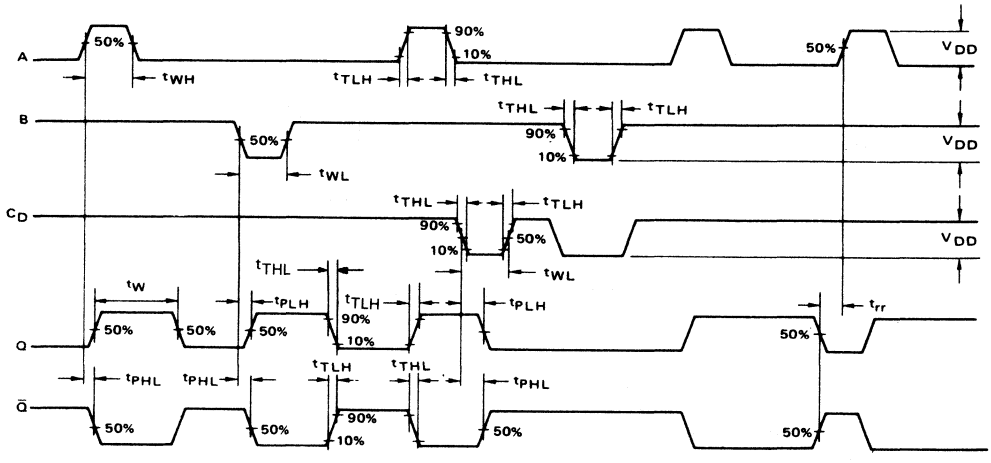


FIGURE 6 — PULSE WIDTH versus C_X

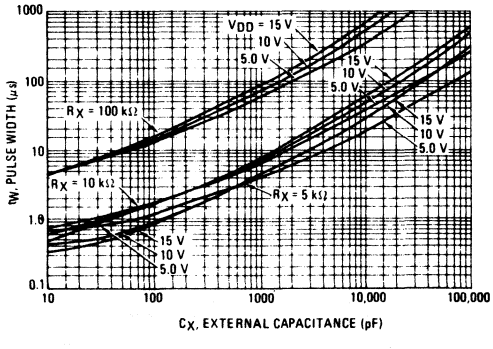
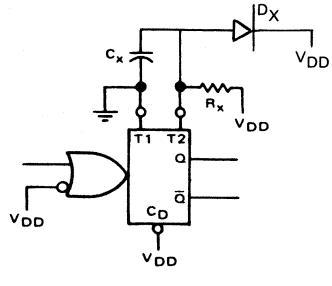


FIGURE 7 — USE OF A DIODE TO LIMIT POWER DOWN CURRENT SURGE



MOTOROLA

MC14529B

DUAL 4-CHANNEL ANALOG DATA SELECTOR

The MC14529B analog data selector is a dual 4-channel or single 8-channel device depending on the input coding. The device is suitable for digital as well as analog application, including various one-of-four and one-of-eight data selector functions. Since the device has bidirectional analog characteristics it can also be used as a dual binary to 1-of-4 or a binary to 1-of-8 decoder.

- Data Paths Are Bidirectional
- Quiescent Current = 1.0 nA/package typical @ 5.0 Vdc
- 10-MHz Operation (typical)
- 3-State Outputs
- Linear "On" Resistance
- "On" Resistance 120 Ohms typical @ 15 V
- Low Noise – 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	ϕ	ϕ	High Impedance		

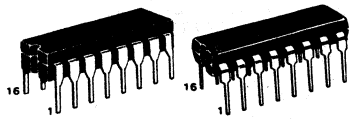
ϕ = Don't Care

This device contains circuitry to protect the control inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} or V_{out} is not constrained to the range $V_{SS} \leq V_{in}$ or $V_{out} \leq V_{DD}$.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-CHANNEL ANALOG DATA SELECTOR OR 8-CHANNEL ANALOG DATA SELECTOR



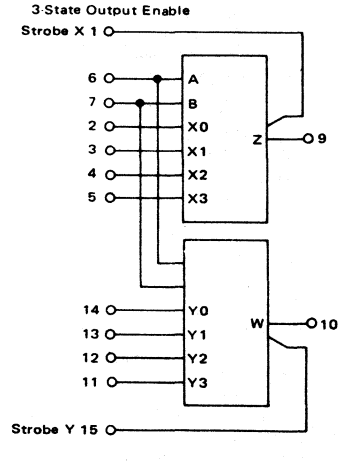
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

3

3

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{SS} Vdc	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	1	V_{OL}	0.0	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0				10	–	0.05	–	0	0.05	–	0.05	
				15	–	0.05	–	0	0.05	–	0.05	
"1" Level		V_{OH}	0.0	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
				10	9.95	–	9.95	10	–	9.95	–	
V_{in} = 0 or V_{DD}				15	14.95	–	14.95	15	–	14.95	–	
Input Voltage # "0" Level	2	V_{IL}	0.0									Vdc
(V_O = 4.5 or 0.5 Vdc)				5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)				10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)				15	–	4.0	–	6.75	4.0	–	4.0	
(V_O = 0.5 or 4.5 Vdc) "1" Level		V_{IH}	0.0	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)				10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)				15	11	–	11	8.25	–	11	–	
Input Current (AL Device) Control		I_{in}	0.0	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device) Control		I_{in}	0.0	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	0.0									pF
Control				–	–	–	–	5.0	7.5	–	–	
Switch Input				–	–	–	–	8.0	–	–	–	
Switch Output				–	–	–	–	20	–	–	–	
Feed Through				–	–	–	–	0.3	–	–	–	
*Quiescent Current (AL Device)	3	I_{DD}	–	5.0	–	1.0	–	0.001	1.0	–	60	µAdc
(Per Package)				10	–	1.0	–	0.002	1.0	–	60	
				15	–	2.0	–	0.003	2.0	–	120	
Quiescent Current (CL/CP Device)	3	I_{DD}	–	5.0	–	5.0	–	0.001	5.0	–	70	µAdc
(Per Package)				10	–	5.0	–	0.002	5.0	–	70	
				15	–	10	–	0.003	10	–	140	
"ON" Resistance (AL Device)	4,5,6	R_{ON}										Ohms
(V_C = V_{DD}, R_L = 10 kΩ)												
(V_{in} = +5.0 Vdc)			−5.0	5.0	–	400	–	200	480	–	640	
(V_{in} = −5.0 Vdc)					–	400	–	200	480	–	640	
(V_{in} = ±0.25 Vdc)					–	400	–	190	480	–	640	
(V_{in} = +7.5 Vdc)			−7.5	7.5	–	240	–	160	270	–	400	
(V_{in} = −7.5 Vdc)					–	240	–	160	270	–	400	
(V_{in} = ±0.25 Vdc)					–	240	–	120	270	–	400	
(V_{in} = +10 Vdc)			0	10	–	400	–	180	480	–	640	
(V_{in} = +0.25 Vdc)					–	400	–	180	480	–	640	
(V_{in} = +5.6 Vdc)					–	400	–	220	480	–	640	
(V_{in} = +15 Vdc)			0	15	–	250	–	180	270	–	400	
(V_{in} = +0.25 Vdc)					–	250	–	180	270	–	400	
(V_{in} = +9.3 Vdc)					–	250	–	215	270	–	400	
"ON" Resistance (CL/CP Device)	4,5,6	R_{ON}										Ohms
(V_C = V_{DD}, R_L = 10 kΩ)												
(V_{in} = +5.0 Vdc)			−5.0	5.0	–	410	–	200	480	–	560	
(V_{in} = −5.0 Vdc)					–	410	–	200	480	–	560	
(V_{in} = +0.25 Vdc)					–	410	–	190	480	–	560	
(V_{in} = +7.5 Vdc)			−7.5	7.5	–	250	–	160	270	–	350	
(V_{in} = −7.5 Vdc)					–	250	–	160	270	–	350	
(V_{in} = ±0.25 Vdc)					–	250	–	120	270	–	350	
(V_{in} = +10 Vdc)			0	10	–	410	–	180	480	–	560	
(V_{in} = +0.25 Vdc)					–	410	–	180	480	–	560	
(V_{in} = +5.6 Vdc)					–	410	–	220	480	–	560	
(V_{in} = +15 Vdc)			0	15	–	250	–	180	270	–	350	
(V_{in} = +0.25 Vdc)					–	250	–	180	270	–	350	
(V_{in} = +9.3 Vdc)					–	250	–	215	270	–	350	
△"ON" Resistance	–	$\triangle R_{ON}$										Ohms
Between any 2 circuits in a common package												
(V_{in} = ±5.0 Vdc)			−5.0	5.0	–	–	–	15	–	–	–	
(V_{in} = ±7.5 Vdc)			−7.5	7.5	–	–	–	10	–	–	–	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device
*T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

SWITCHING CHARACTERISTICS (T_A = 25°C)

Characteristic	Figure	Symbol	V_{SS}	V_{DD}	Typical All Types	Maximum AL Device	Maximum CL/CP Device	Unit
V_{in} to V_{out} Propagation Delay Time (C_L = 50 pF, R_L = 1.0 kΩ)	7	t_{PLH},t_{PHL}	0.0	5.0	20	40	60	ns
				10	10	20	30	
				15	8.0	15	25	
Propagation Delay Time, Control to Output, V_{in} = V_{DD} or V_{SS} (V_{in} ≤ 10 Vdc, C_L = 50 pF, R_L = 1.0 kΩ)	8	t_{PHL},t_{PLH}	0.0	5.0	200	400	600	ns
				10	80	160	240	
				15	50	120	180	
Crosstalk, Control to Output (C_L = 50 pF, R_L = 1.0 kΩ) R_{out} = 10 kΩ)	9	–	0.0	5.0	5.0	–	–	mV
				10	5.0	–	–	
				15	5.0	–	–	
Maximum Control Input Pulse Frequency (C_L = 50 pF, R_L = 1.0 kΩ)	10	–	0.0	5.0	5.0	–	–	MHz
				10	10	–	–	
				15	12	–	–	
Noise Voltage (f = 100 Hz)	11,12	–	0.0	5.0	24	–	–	nV/√Cycle
				10	25	–	–	
				15	30	–	–	
(f = 100 kHz)				5.0	12	–	–	
				10	12	–	–	
				15	15	–	–	
Sine Wave (Distortion) (V_{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	–	–	-5.0	5.0	0.36	–	–	%
Input/Output Leakage Current	–	–						nA
(V_{in} = +5.0 Vdc, V_{out} = -5.0 Vdc)			-5.0	5.0	±0.001	±125	±125	
(V_{in} = -5.0 Vdc, V_{out} = +5.0 Vdc)			-5.0	5.0	±0.001	±125	±125	
(V_{in} = +7.5 Vdc, V_{out} = -7.5 Vdc)			-7.5	7.5	±0.0015	±250	±250	
(V_{in} = -7.5 Vdc, V_{out} = +7.5 Vdc)			-7.5	7.5	±0.0015	±250	±250	
Insertion Loss (V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc, f = 1.0 MHz, $I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$	–	–	-5.0	5.0				dB
(R_L = 1.0 kΩ)					2.0	–	–	
(R_L = 10 kΩ)					0.8	–	–	
(R_L = 100 kΩ)					0.25	–	–	
(R_L = 1.0 MΩ)					0.01	–	–	
Bandwidth (-3 dB) (V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc)	–	BW	-5.0	5.0				MHz
(R_L = 1.0 kΩ)					35	–	–	
(R_L = 10 kΩ)					28	–	–	
(R_L = 100 kΩ)					27	–	–	
(R_L = 1.0 MΩ)					26	–	–	
Feedthrough and Crosstalk ($20 \log_{10} \frac{V_{out}}{V_{in}} = -50$ dB)	–	–	-5.0	5.0				kHz
(R_L = 1.0 kΩ)					850	–	–	
(R_L = 10 kΩ)					100	–	–	
(R_L = 100 kΩ)					12	–	–	
(R_L = 1.0 MΩ)					1.5	–	–	

3

FIGURE 1 - OUTPUT VOLTAGE TEST CIRCUIT

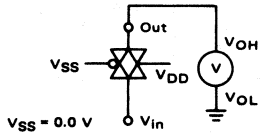
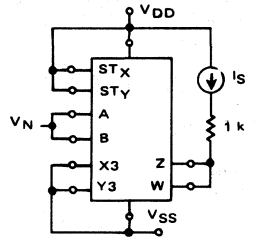


FIGURE 2 – NOISE IMMUNITY TEST CIRCUIT



$V_{NL} = V_N$ when $I_S = 10\ \mu A$
$V_{NH} = V_{DD} - V_N$ when $I_S = 10\ \mu A$
Pins 2,3,4,12,13 and 14 are left open.

3

FIGURE 3 – QUIESCENT POWER DISSIPATION TEST CIRCUIT

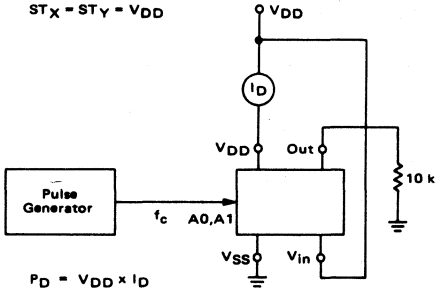
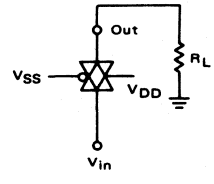


FIGURE 4 – R_{ON} CHARACTERISTICS TEST CIRCUIT



TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 5

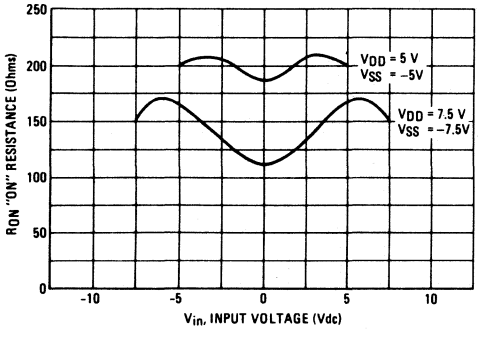


FIGURE 6

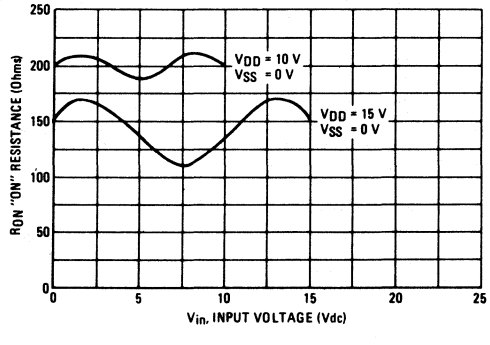


FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

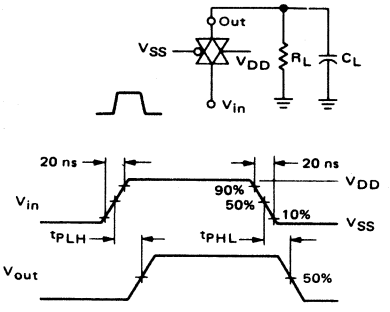


FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

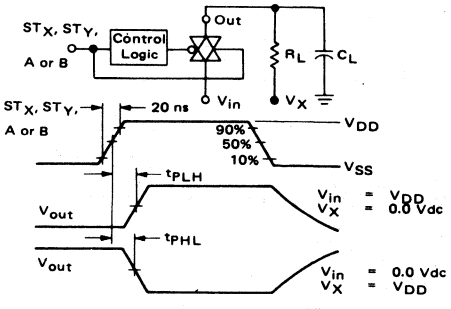


FIGURE 9 – CROSSTALK TEST CIRCUIT

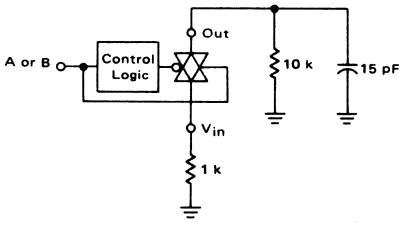


FIGURE 10 – FREQUENCY RESPONSE TEST CIRCUIT

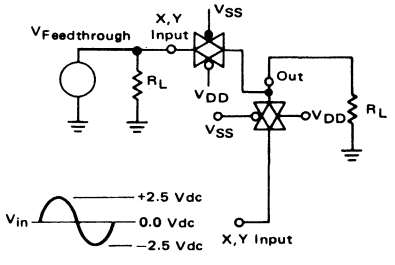


FIGURE 11 – NOISE VOLTAGE TEST CIRCUIT

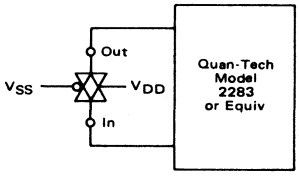


FIGURE 12 – TYPICAL NOISE CHARACTERISTICS

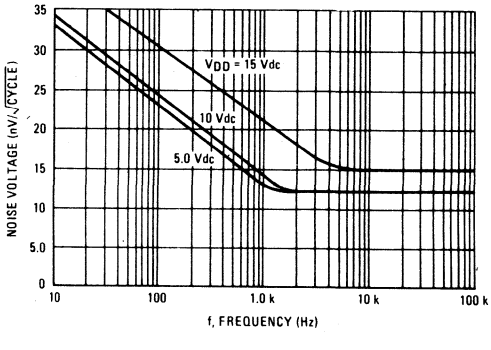
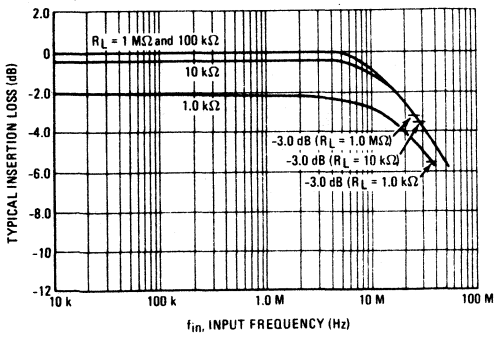
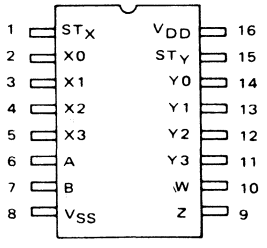


FIGURE 13 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS



PIN ASSIGNMENT



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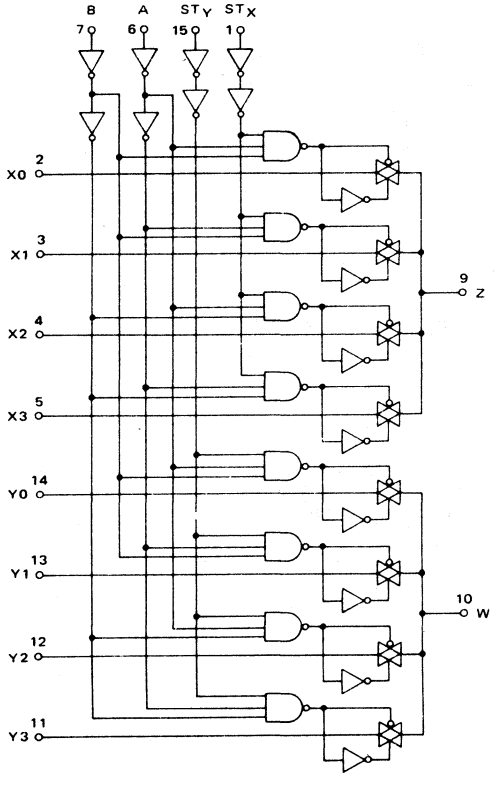
LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MOTOROLA

MC14530B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 5-INPUT MAJORITY LOGIC GATE

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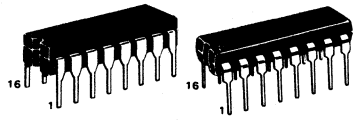
The MC14530B dual five-input majority logic gate is constructed with P-channel and N-channel enhancement mode devices in a single monolithic structure. Combinational and sequential logic expressions are easily implemented with the majority logic gate, often resulting in fewer components than obtainable with the more basic gates. This device can also provide numerous logic functions by using the W and some of the logic (A thru E) inputs as control inputs.

- Single Supply Operation – Positive or Negative
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Input Impedance = 10^{12} ohms typical
- High Fanout > 50
- Diode Protection on Inputs
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

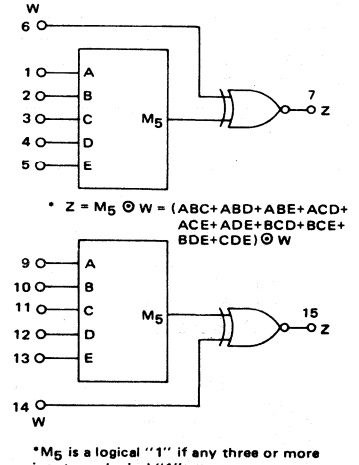
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC TABLE

INPUTS A B C D E	W	Z
For all combinations of inputs where three or more inputs are logical "0".	0	1
	1	0
For all combinations of inputs where three or more inputs are logical "1".	0	0
	1	1

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must be tied to an appropriate logic level (e.g., V_{SS} or V_{DD}).

BLOCK DIAGRAM



* $Z = M_5 \odot W = (ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE) \odot W$

*M_5 is a logical "1" if any three or more inputs are logical "1".

$\odot \equiv$ Exclusive NOR $\equiv \overline{\text{Exclusive OR}}$

TRUTH TABLE

M_5	W	Z
0	0	1
0	1	0
1	0	0
1	1	1

V_{DD} = Pin 16
V_{SS} = Pin 8

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.2	–	2.25	1.25	–	1.15	
(V_O = 9.0 or 1.0 Vdc)		10	–	2.5	–	4.50	2.5	–	2.4	
(V_O = 13.5 or 1.5 Vdc)		15	–	3.0	–	6.75	3.0	–	2.9	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.85	–	3.75	2.75	–	3.75	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.6	–	7.5	5.50	–	7.5	–	
(V_O = 1.5 or 13.5 Vdc)		15	12.1	–	12	8.25	–	12	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.75 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.50 μA/kHz) f + I_{DD}							
		15	I_T = (2.25 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination. Standard family noise margin specification is met for any one input tested at a time.

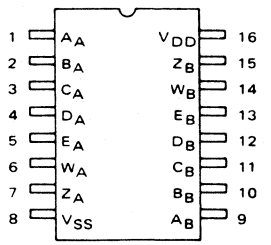
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and fin kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT

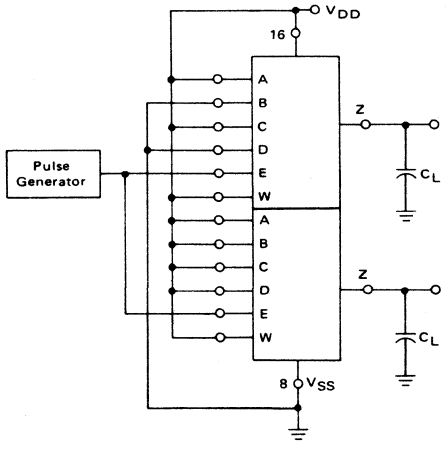


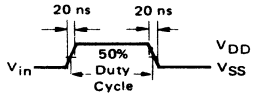
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}					ns
A, C, W = V_{DD}; B, E = Gnd; D = Pulse Generator						
t_{PLH} = (1.7 ns/pF) C_L + 290 ns		5.0	–	375	960	
t_{PLH} = (0.66 ns/pF) C_L + 127 ns		10	–	160	400	
t_{PLH} = (0.5 ns/pF) C_L + 85 ns		15	–	110	300	
t_{PHL} = (1.7 ns/pF) C_L + 345 ns	t_{PHL}	5.0	–	430	1200	ns
t_{PHL} = (0.66 ns/pF) C_L + 162 ns		10	–	195	540	
t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	120	410	
A, B, C, D, E = Pulse Generator; W = V_{DD}	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 170 ns		5.0	–	255	640	
t_{PLH} = (0.66 ns/pF) C_L + 87 ns		10	–	120	300	
t_{PLH} = (0.5 ns/pF) C_L + 60 ns		15	–	85	210	
t_{PHL} = (1.7 ns/pF) C_L + 195 ns	t_{PHL}	5.0	–	280	750	ns
t_{PHL} = (0.66 ns/pF) C_L + 92 ns		10	–	125	330	
t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	250	
A, B, C, D, E = Gnd; W = Pulse Generator	t_{PLH},					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 145 ns	t_{PHL}	5.0	–	230	575	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 72 ns		10	–	105	265	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 50 ns		15	–	75	190	

* The formulae given are for the typical characteristics only.

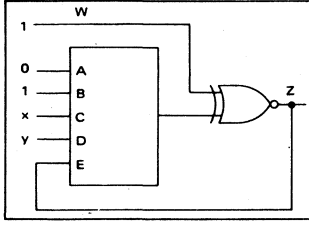
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM





SEQUENTIAL LOGIC APPLICATIONS

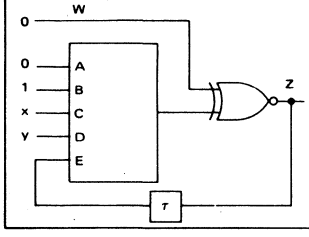
COINCIDENT FLIP-FLOP



x	y	Q_{n+1}
0	0	0
0	1	Q
1	0	Q
1	1	1

A flip-flop that will change only when both inputs agree.

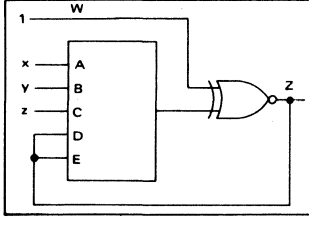
ASTABLE MULTIVIBRATOR



x	y	Q_{n+1}
0	0	1
0	1	2τ
1	0	2τ
1	1	0

A flip-flop with three output conditions, where the third state is in oscillation between "1" and "0". The period of oscillation is twice the delay of the gate and the feedback element.

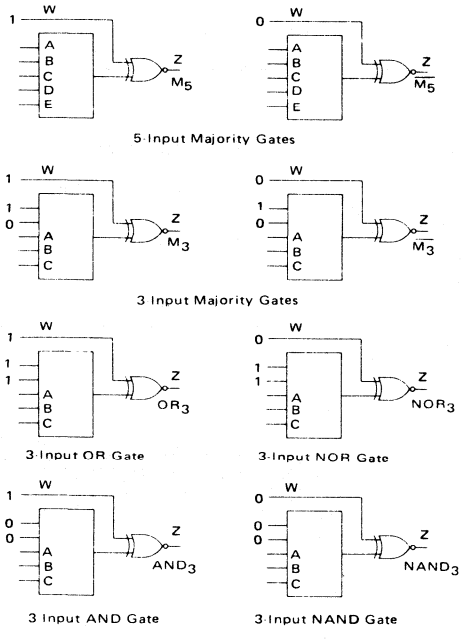
COINCIDENT FLIP-FLOP



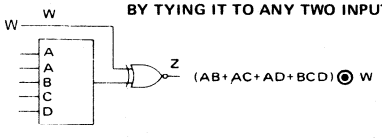
x	y	z	Q_{n+1}
0	0	0	0
0	0	1	Q_n
0	1	0	Q_n
0	1	1	Q_n
1	0	0	Q_n
1	0	1	Q_n
1	1	0	Q_n
1	1	1	1

The flip-flop changes state only when all "1's" or all "0's" are entered. This configuration may be extended by cascading M_5 gates to cover n-inputs where all inputs must be "1's" or "0's" before the output will change. As an example, this configuration is useful for controlling an n-stage up/down counter that is to cycle from a minimum to maximum count and back again without flipping over (from all "1's" to all "0's".)

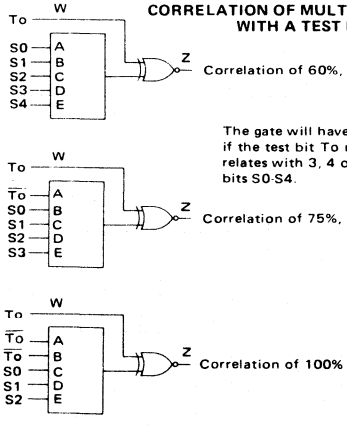
BASIC COMBINATIONAL FUNCTIONS



DOUBLING THE WEIGHT OF INPUT VARIABLE A BY TYING IT TO ANY TWO INPUTS



CORRELATION OF MULTIPLE SAMPLES WITH A TEST BIT



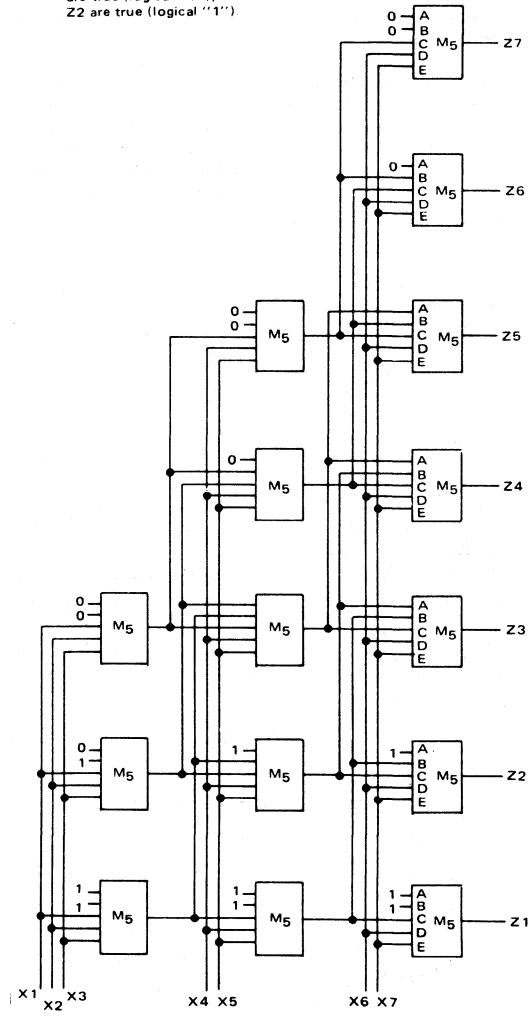
The gate will have a "1" output if the test bit To matches or correlates with 3, 4 or 5 of the sample bits S0-S4.

5-INPUT MAJORITY LOGIC GATE APPLICATIONS

Each package labeled M_5 is a single majority logic gate using five inputs, A thru E, and one output Z.

1. Majority Logic Gate Array yielding the symetric function of 1 thru 7 variables true, out of 7 input variables (X1 . . . X7)

(e.g., if any two-input variables are true (logical "1"), Z1 and Z2 are true (logical "1").



3

MOTOROLA

MC14531B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

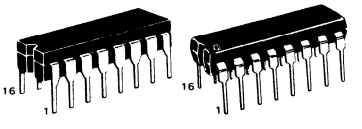
12-BIT PARITY TREE

3

12-BIT PARITY TREE

The MC14531B 12-bit parity tree is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of 12 data-bit inputs (D0 thru D11), and even or odd parity selection input (W) and an output (Q). The parity selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even or odd number of ones, respectively. Words of greater than 12-bits can be accommodated by cascading other MC14531B devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple input summer without carries.

- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Variable Word Length
- Diode Protection on All Inputs



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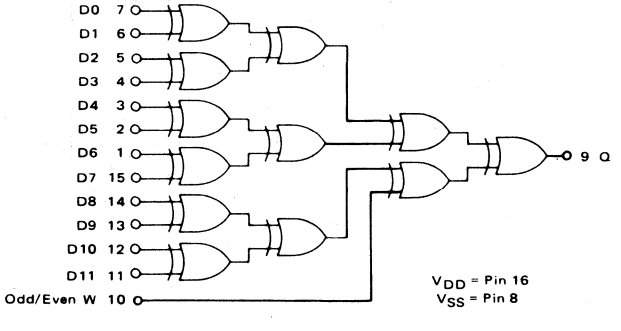
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



$Q = D0 \oplus D1 \oplus D2 \oplus \ldots . \oplus D11 \oplus W$

TRUTH TABLE

INPUTS								OUTPUT
W	D11	D10	···	D2	D1	D0	DECIMAL (OCTAL) EQUIVALENT	Q*
0	0	0	···	0	0	0	0 (0)	0
0	0	0	···	0	0	1	1 (1)	1
0	0	0	···	0	1	0	2 (2)	1
0	0	0	···	0	1	1	3 (3)	0
0	0	0	···	1	0	0	4 (4)	1
0	0	0	···	1	0	1	5 (5)	0
0	0	0	···	1	1	0	6 (6)	0
0	0	0	···	1	1	1	7 (7)	1
.	.	.	. . .	.	.	.	.	.
1	1	1	···	0	0	0	8184 (17770)	0
1	1	1	···	0	0	1	8185 (17771)	1
1	1	1	···	0	1	0	8186 (17772)	1
1	1	1	···	0	1	1	8187 (17773)	0
1	1	1	···	1	0	0	8188 (17774)	1
1	1	1	···	1	0	1	8189 (17775)	0
1	1	1	···	1	1	0	8190 (17776)	0
1	1	1	···	1	1	1	8191 (17777)	1

*0 = Even Parity
1 = Odd Parity

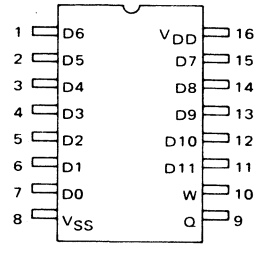
Note: May redefine to suit application by manipulating W and/or other available D's.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–		–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.25 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.50 μA/kHz) f + I_{DD}							
		15	I_T = (0.75 μA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



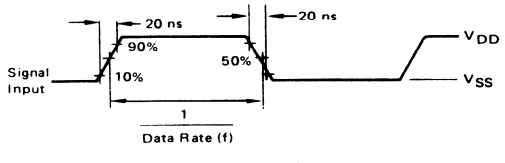
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Data to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 355 ns		5.0	–	440	1320	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 142 ns		10	–	175	525	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	120	360	
Odd/Even to Q						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 165 ns		5.0	–	250	750	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	210	

* The formulae given are for the typical characteristics only.

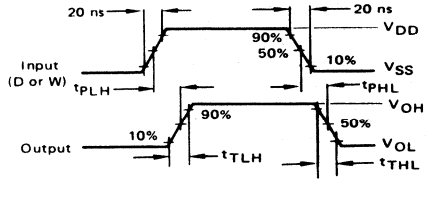
3

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORM



f in respect to system clock

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



MOTOROLA

MC14532B

8-BIT PRIORITY ENCODER

The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (E_{in}) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E_{out}).

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Low Input Capacitance — 5.0 pF typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUT									OUTPUT				
E_{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

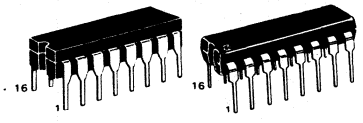
X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

8-BIT PRIORITY ENCODER



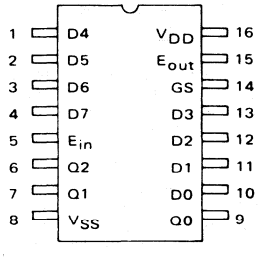
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−2.4	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.74 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.65 μA/kHz) f + I_{DD}							
		15	I_T = (5.73 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

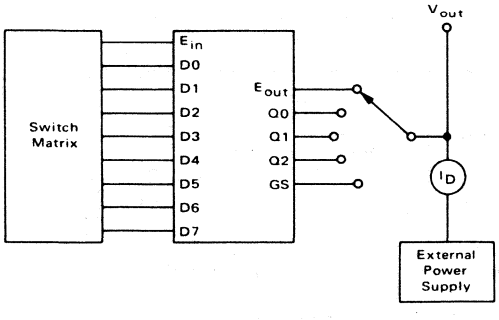
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Ouput Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Progagation Delay Time – E_{in} to E_{out}	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 120 ns		5.0	–	205	410	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 77 ns		10	–	110	220	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 55 ns		15	–	80	160	
Propagation Delay Time (E_{in} to GS	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} - (0.5 ns/pF) C_L + 40 ns		15	–	65	130	
Propagation Delay Time – E_{in} to Q_n	t_{PHL}, t_{PLH}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 195 ns		5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 107 ns		10	–	140	280	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
Propagation Delay Time – D_n to Q_n	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 137 ns		10	–	170	340	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	
Propagation Delay Time – D_n to GS	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 195 ns		5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 107 ns		10	–	140	280	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	

*The formulae given are for the typical characteristics only.

3

FIGURE 1 – TYPICAL SINK AND SOURCE CURRENT CHARACTERISTICS



Output Under Test	V_{GS} = V_{DD} V_{DS} = V_{out} Sink Current		V_{GS} = -V_{DD} V_{DS} = V_{out} -V_{DD} Source Current		
	D0 thru D7	E_{in}	D0 thru D6	D7	E_{in}
E_{out}	X	0	0	0	1
Q0	X	0	0	1	1
Q1	X	0	0	1	1
Q2	X	0	0	1	1
GS	X	0	0	1	1

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT

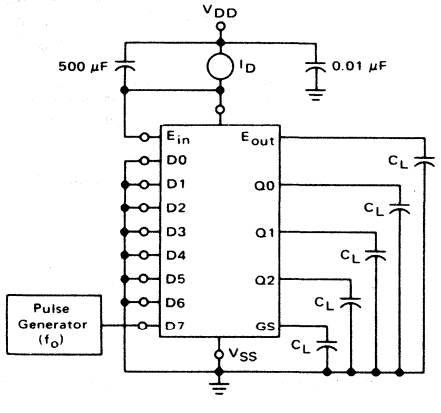
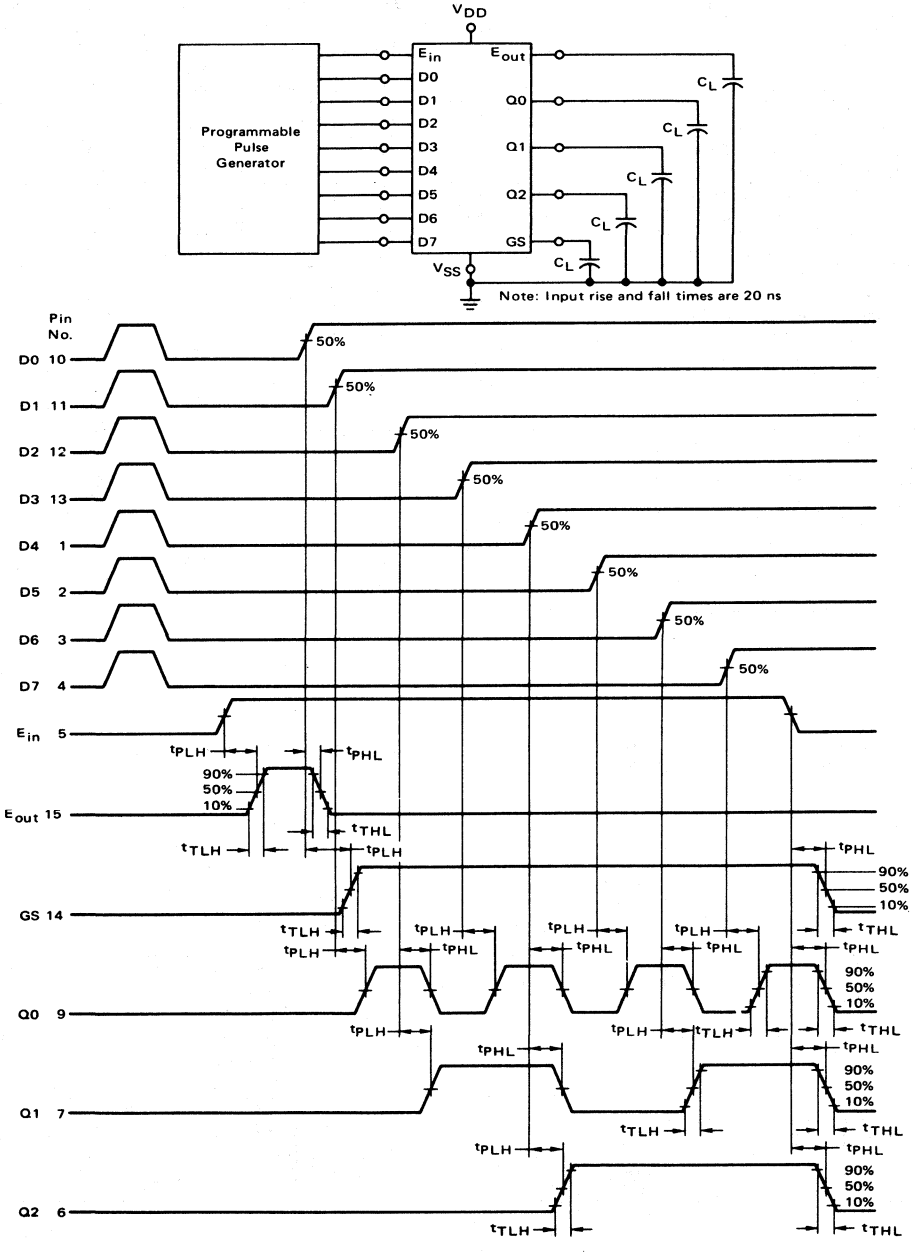


FIGURE 3 – AC TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAM
(Positive Logic)

LOGIC EQUATIONS

$E_{out} = E_{in} \bullet \overline{D0} \bullet \overline{D1} \bullet \overline{D2} \bullet \overline{D3} \bullet \overline{D4} \bullet \overline{D5} \bullet \overline{D6} \bullet \overline{D7}$
$Q0 = E_{in} \bullet (D1 \bullet \overline{D2} \bullet \overline{D4} \bullet \overline{D6} + D3 \bullet \overline{D4} \bullet \overline{D6} + D5 \bullet \overline{D6} + D7)$
$Q1 = E_{in} \bullet (D2 \bullet D4 \bullet \overline{D5} + D3 \bullet \overline{D4} \bullet \overline{D5} + D6 + D7)$
$Q_2 = E_{in} \bullet (D4 + D5 + D6 + D7)$
$GS = E_{in} \bullet (D0 + D1 + D2 + D3 + D4 + D5 + D6 + D7)$

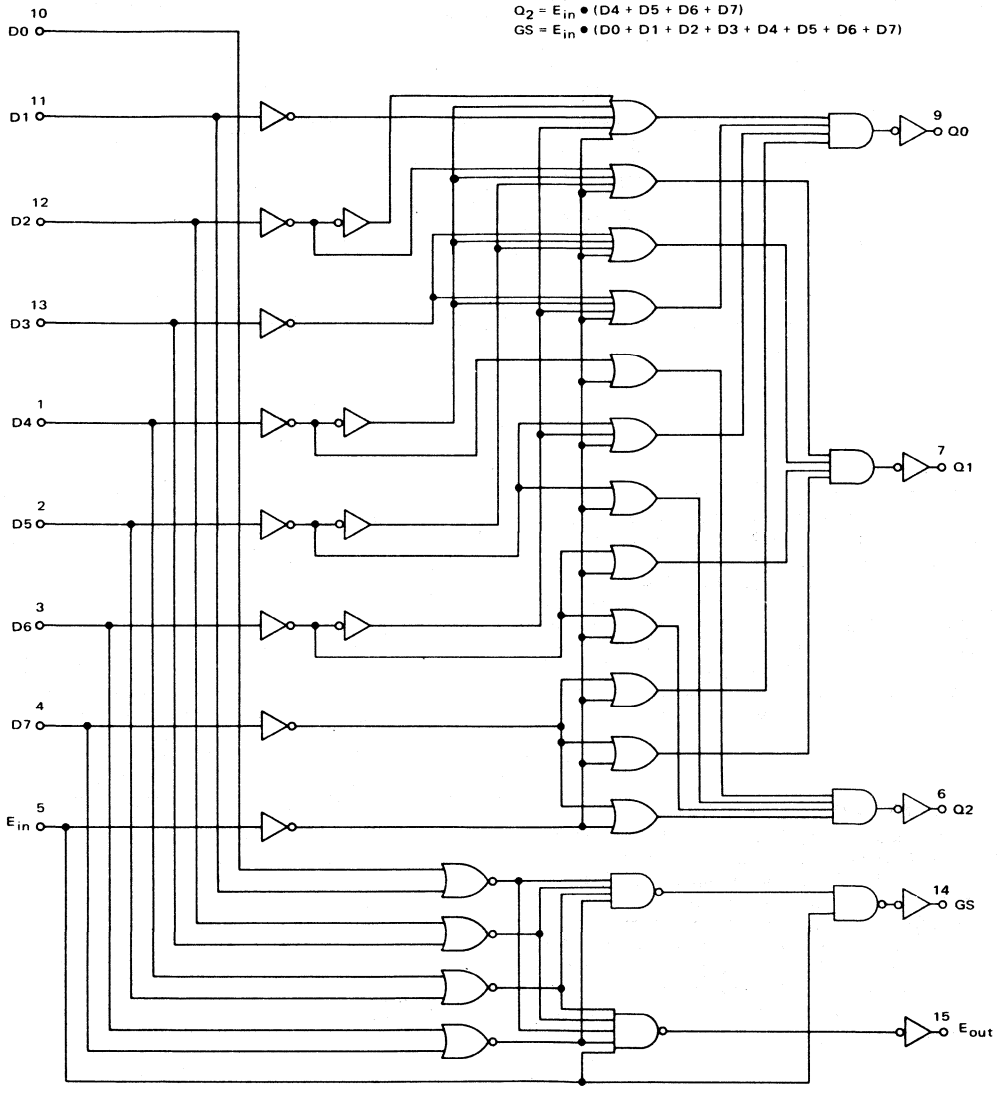


FIGURE 4 – TWO MC14532B's CASCADED FOR 4-BIT OUTPUT

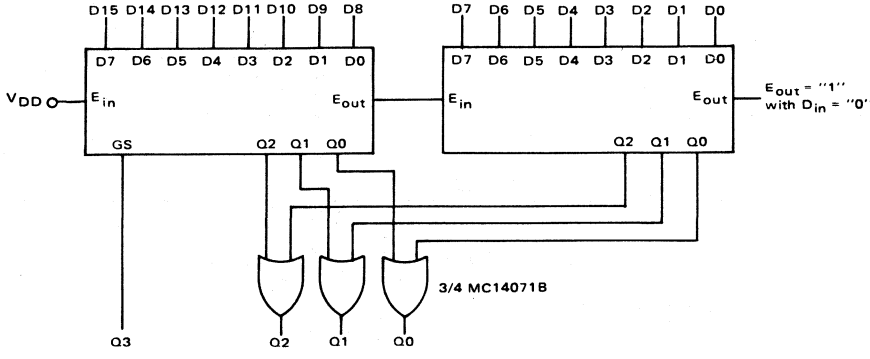


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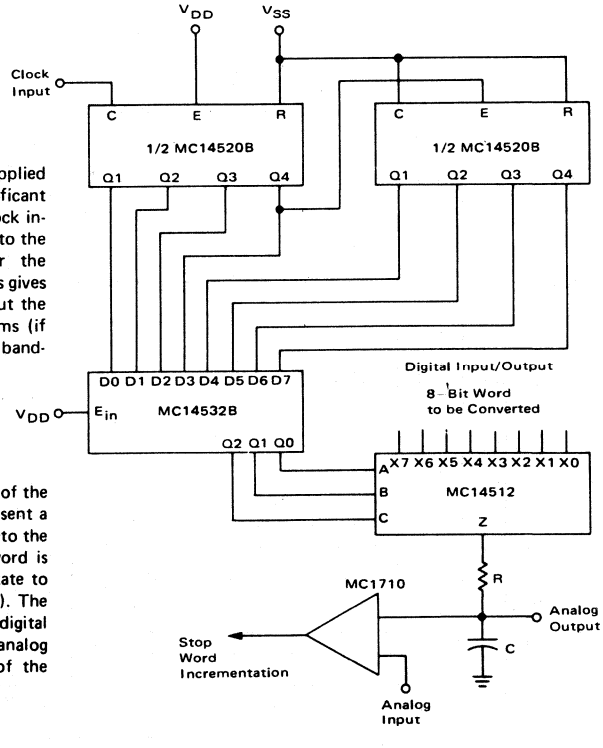
FIGURE 5 – DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTER



DIGITAL TO ANALOG CONVERSION

The digital eight-bit word to be converted is applied to the inputs of the MC14512 with the most significant bit at X7 and the least significant bit at X0. A clock input of up to 2.5 MHz (at V_{DD} = 10 V) is applied to the MC14520B. A compromise between I_{bias} for the MC1710 and ΔR between N and P-channel outputs gives a value of R of 33 k ohms. In order to filter out the switching frequencies, RC should be about 1.0 ms (if R = 33 k ohms, C ≈ 0.03 μF). The analog 3.0 dB bandwidth would then be dc to 1.0 kHz.

ANALOG TO DIGITAL CONVERSION

An analog signal is applied to the analog input of the MC1710. A digital eight-bit word known to represent a digitized level less than the analog input is applied to the MC14512 as in the D to A conversion. The word is incremented at rates sufficient to allow steady state to be reached between incrementations (i.e. 3.0 ms). The output of the MC1710 will change when the digital input represents the first digitized level above the analog input. This word is the digital representation of the analog word.

MOTOROLA

MC14534B

CMOS LSI

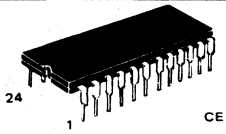
(LOW-POWER COMPLEMENTARY MOS)

5-DECADE COUNTER

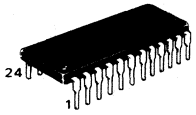
5-DECADE COUNTER

The MC14534B is a complementary MOS circuit composed of five decade ripple counters that have their respective outputs time multiplexed using an internal scanner. Outputs of each counter are selected by the scanner and appear on four BCD pins. The selected decade is indicated by a logic high on the appropriate digit select pin. Both BCD and digit select outputs have three-state controls providing an "open-circuit" when these controls are high and allowing time multiplexing. Cascading may be accomplished by using the carry-out pin. The counters and scanner can be independently reset by applying a high to the counter master reset (MR) and the scanner reset (SR). The MC14534B was specifically designed for application in real time or event counters where continual updating and multiplexed displays are used.

- Four Operating Modes (See truth table)
- Input Error Detection Circuit
- Clock Conditioning Circuits for Slow Transition Inputs
- Counter Sequences on Positive Transition of Clock A
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 623



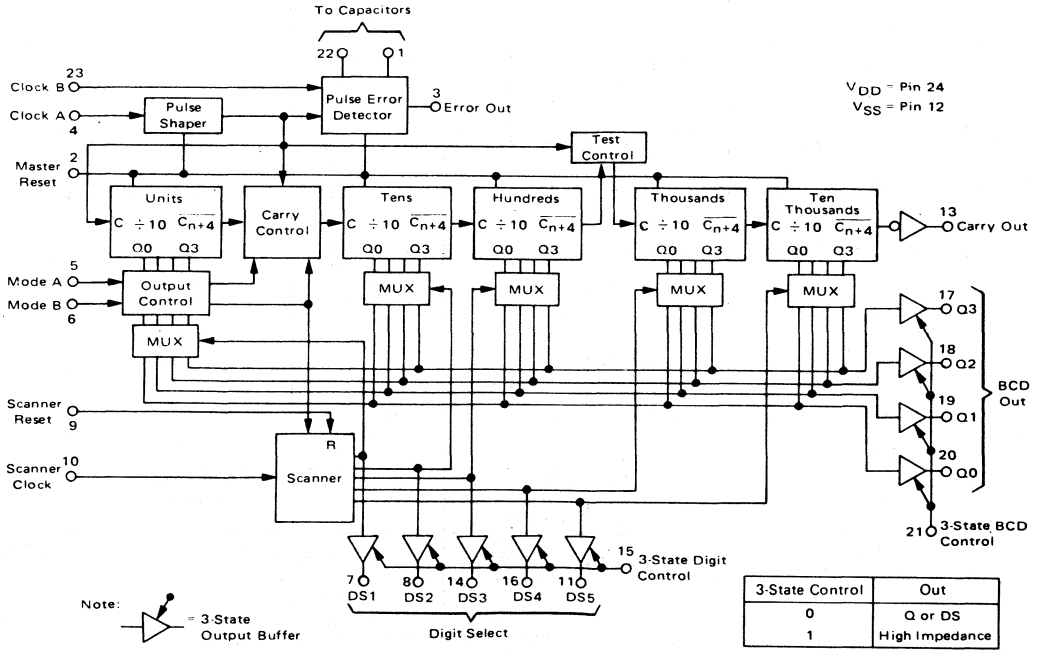
P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

3

BLOCK DIAGRAM



3-State Control	Out
0	Q or DS
1	High Impedance

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.0	–	1.5	1.0	–	1.0	
(V_O = 9.0 or 1.0 Vdc)		10	–	2.0	–	3.0	2.0	–	2.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	3.0	–	4.5	3.0	–	3.0	
(V_O = 0.5 or 4.5 Vdc) "1" Level	V_{IH}	5.0	4.0	–	4.0	3.5	–	4.0	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	8.0	–	8.0	7.0	–	8.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	12	–	12	11	–	12	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.2	–	-1.0	-1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	-1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.2	–	-0.16	-0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Output Drive Current — Pins 1 and 22 (AL Device)										mAdc
(V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.31	–	-0.25	-0.8	–	-0.17	–	
(V_{OH} = 9.5 Vdc)		10	-0.31	–	-0.25	-0.4	–	-0.17	–	
(V_{OH} = 13.5 Vdc)		15	-0.9	–	-0.75	-1.6	–	-0.51	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.024	–	0.02	0.03	–	0.014	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.06	–	0.05	0.09	–	0.035	–	
(V_{OL} = 1.5 Vdc)		15	1.3	–	0.25	1.63	–	0.175	–	
Output Drive Current — Pins 1 and 22 (CL/CP Device)										mAdc
(V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.11	–	-0.10	-0.8	–	-0.08	–	
(V_{OH} = 9.5 Vdc)		10	-0.11	–	-0.10	-0.4	–	-0.08	–	
(V_{OH} = 13.5 Vdc)		15	-0.33	–	-0.30	-1.6	–	-0.24	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.012	–	0.01	0.02	–	0.008	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.03	–	0.025	0.05	–	0.02	–	
(V_{OL} = 1.5 Vdc)		15	0.14	–	0.12	1.35	–	0.10	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0 10 15	– – –	5.0 10 20	– – –	0.010 0.020 0.030	5.0 10 20	– – –	150 300 600	μAdc
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0 10 15	– – –	50 100 200	– – –	0.010 0.020 0.030	50 100 200	– – –	375 750 1500	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	$I_T = (0.5\ \mu A/kHz)\ f + I_{DD}$ $I_T = (1.0\ \mu A/kHz)\ f + I_{DD}$ $I_T = (1.5\ \mu A/kHz)\ f + I_{DD}$				Scan Oscillator Frequency = 1 kHz			μAdc
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$ where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

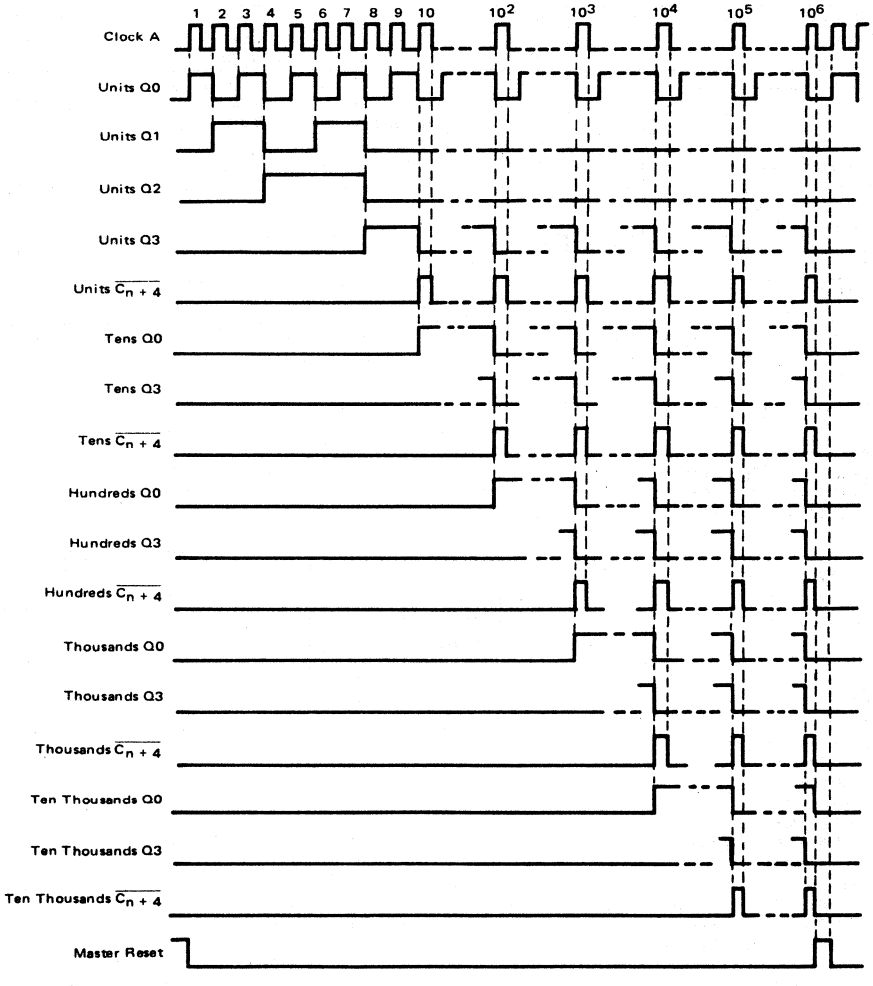
3

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 95 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 78 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 68 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 117 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 89 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 67 ns		15	–	40	80	
Propagation Delay Time, Clock to Q	t_{PLH}, t_{PHL}					μs
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 4.0 μs		5.0	–	4.0	8.0	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 1.5 μs		10	–	1.5	3.0	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 1.0 μs		15	–	1.0	2.25	
Clock to Carry Out	t_{PLH}					μs
t_{PLH} = (1.8 ns/pF) C_L + 3.3 μs		5.0	–	3.3	6.6	
t_{PLH} = (0.8 ns/pF) C_L + 1.1 μs		10	–	1.1	2.2	
t_{PLH} = (0.6 ns/pF) C_L + 0.8 μs		15	–	0.8	1.7	
Master Reset to Q	t_{PHL}					μs
t_{PHL} = (1.8 ns/pF) C_L + 1.8 μs		5.0	–	1.8	3.6	
t_{PHL} = (0.8 ns/pF) C_L + 0.6 μs		10	–	0.6	1.2	
t_{PHL} = (0.6 ns/pF) C_L + 0.5 μs		15	–	0.5	0.9	
Master Reset to Error Out	t_{PHL}					μs
t_{PHL} = (1.8 ns/pF) C_L + 0.57 μs		5.0	–	0.6	1.5	
t_{PHL} = (0.8 ns/pF) C_L + 0.19 μs		10	–	0.2	.5	
t_{PHL} = (0.6 ns/pF) C_L + 0.11 μs		15	–	0.12	0.38	
Scanner Clock to Q	t_{PLH}, t_{PHL}					μs
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 1.8 μs		5.0	–	1.8	3.6	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 0.6 μs		10	–	0.6	1.2	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 0.5 μs		15	–	0.5	0.9	
Scanner Clock to Digit Select	t_{PLH}, t_{PLH},					μs
t_{PHL}, t_{PLH} = (1.8 ns/pF) C_L + 1.5 μs		5.0	–	1.5	3.0	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 0.5 μs		10	–	0.5	1.0	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 0.4 μs		15	–	0.4	0.75	
Clock Pulse Frequency	f_{cl}	5.0	–	1.0	0.5	MHz
		10	–	3.0	1.0	
		15	–	5.0	1.2	
Clock or Scanner Clock Pulse Width	t_{WH}	5.0	1000	500	–	ns
		10	500	190	–	
		15	375	125	–	
Master Reset Pulse Width	$t_{WH(R)}$	5.0	2000	900	–	ns
		10	600	300	–	
		15	450	250	–	

*The formulae given are for the typical characteristics only.

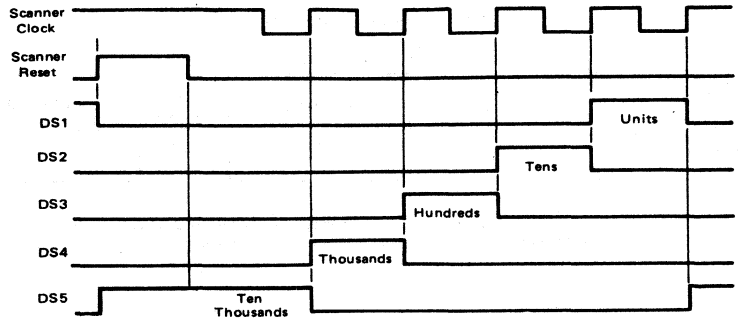
COUNTER TIMING DIAGRAM



MODE CONTROL TRUTH TABLE

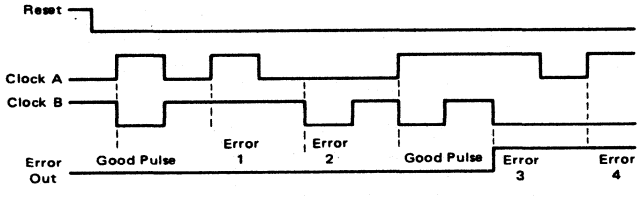
Mode A	Mode B	First Decade Output	Carry to Second Stage	Application
0	0	Normal Count and Display	At 9 to 0 transition of first decade	5-Decade Counter
0	1	Inhibited	Input Clock	Test Mode: Clock directly into stages 1, 2, and 4.
1	1	Inhibited	At 4 to 5 transition of first decade	4-decade counter with ÷ 10 and roundoff at front end.
1	0	Counts 3,4,5,6,7 = 5 Counts 8,9,0,1,2 = 0	At 7 to 8 transition of first decade	4-decade counter with 1/2 pence capability.

SCANNER TIMING DIAGRAM



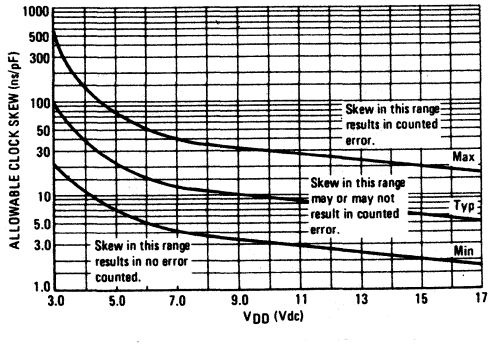
Note: If Mode B = 1, the first decade is inhibited and S1 will not go high, and the cycle will be shortened to four stages.
DS5 is selected automatically when Scanner Reset goes high.

ERROR DETECTION TIMING DIAGRAM



Note: Error detector looks for inverted pulse on Clock B. Whenever a positive edge at Clock A is not accompanied by a negative pulse at Clock B (or vice-versa) within a time period of the one-shots an error is counted. Three errors result in Error Out to go to a "1". If error detection is not needed, tie Clock B high or low and leave Pins 1 and 22 unconnected.

CLOCK SKEW RANGE

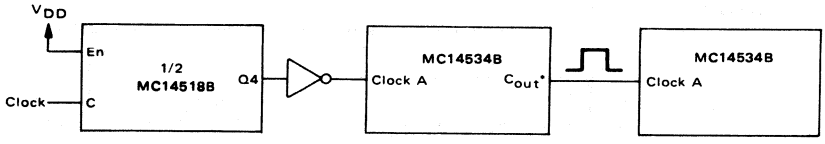


Notes:

1. The skew is the time difference between the low-to-high transition of C_A to the high-to-low transition of C_B or vice-versa. Capacitors C1 = C22 tied from pins 1 and 22 to V_{SS}.
2. This graph is accurate for C1 = C22 $\geq$ 100 pF.
3. When the error detection circuitry is not used, pins 1 and 22 are left open.

APPLICATIONS INFORMATION

FIGURE 1 – CASCADE OPERATION



*Carry Out is high for a single clock period when all five BCD decades go to zero. (Carry Out also goes high when MR is applied.)

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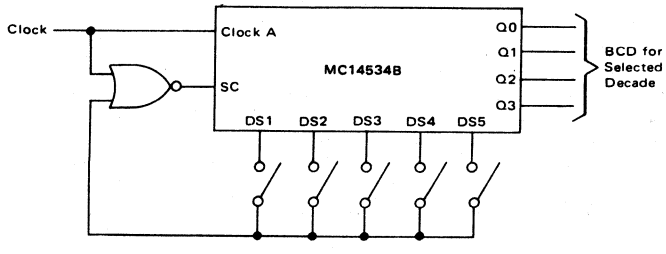
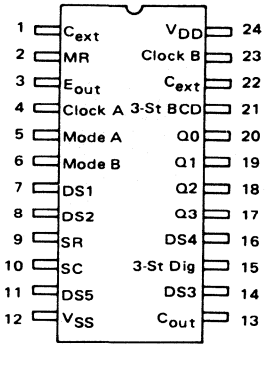
FIGURE 2 – FORCING A DECADE TO THE Q OUTPUTS



When the Q outputs of a given decade are required, this configuration will lock up the selected decade within four clock cycles. The select line feedback may be hardwired or switched.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

MOTOROLA

MC14536B

PROGRAMMABLE TIMER

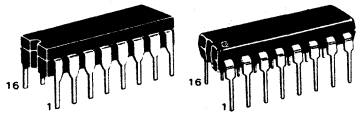
The MC14536B programmable timer is a flexible 24-stage ripple binary counter with 16 stages selectable by a binary code. Provisions for an on-chip RC oscillator, or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has also been included. By selecting the appropriate output in conjunction with the correct input clock frequency, a variety of timing can be achieved.

- 24 Flip-Flop Stages – Will Count From 2^0 to 2^{24}
- Last 16 Stages Selectable By Four-Bit Select Code
- Input Allows Bypassing of First Eight Stages
- Set and Reset Inputs
- Clock Inhibit Input
- On-Chip RC Oscillator Provisions
- On-Chip Monostable Output Provisions
- Clock Conditioning Circuit Permits Operation With Very Long Rise and Fall Times
- Clock Input f_{max} = 3.0 MHz typical @ V_{DD} = 10 Vdc
- Counter Advances On Negative Going Edge of Clock
- Test Mode Allows Fast Test Sequence
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

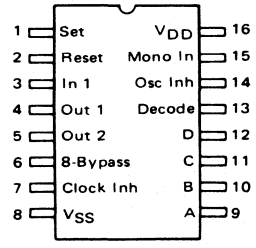
PROGRAMMABLE TIMER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

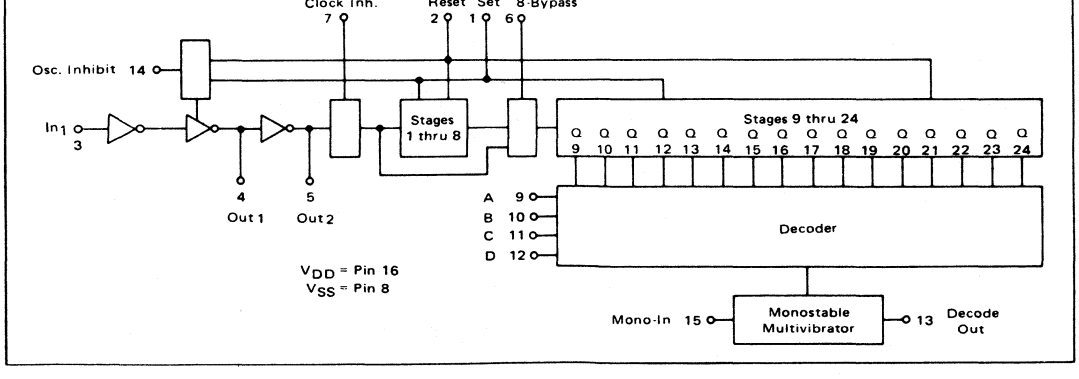
PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage # "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	
(V_{OH} = 4.6 Vdc) Pins 4 & 5		5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
(V_{OH} = 9.5 Vdc)		10	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OH} = 13.5 Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	mAdc
(V_{OH} = 4.6 Vdc) Pin 13		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	−0.8	−1.7	–	−0.6	–	
(V_{OH} = 4.6 Vdc) Pins 4 & 5		5.0	−0.2	–	−0.16	−0.36	–	−0.12	–	
(V_{OH} = 9.5 Vdc)		10	−0.5	–	−0.4	−0.9	–	−0.3	–	
(V_{OH} = 13.5 Vds)		15	−1.4	–	−1.2	−3.5	–	−1.0	–	
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	mAdc
(V_{OH} = 4.6 Vdc) Pin 13		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	± 0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	± 0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.15 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.3 µA/kHz) f + I_{DD}							
		15	I_T = (3.55 µA/kHz) f + I_{DD}							

* T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

\# Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

† To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pf) + 3 \times 10^{-3} (C_L\text{-}50) V_{DD} f$.
where: I_T is in µA (Per Package) C_L in pF, V_{DD} in Vdc and f in kHz is input frequency.

** The formulae given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time (Counter Outputs)	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time (Counter Outputs)	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q1, 8-Bypass (Pin 6) High	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1715 ns		5.0	–	1800	3600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 617 ns		10	–	650	1300	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	–	450	1000	
Clock to Q1, 8-Bypass (Pin 6) Low	t_{PLH},					µs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3715 ns	t_{PHL}	5.0	–	3.8	7.6	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1467 ns		10	–	1.5	3.0	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 1075 ns		15	–	1.1	2.3	
Clock to Q16	t_{PLH},					µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 6915 ns	t_{PHL}	5.0	–	7.0	14	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 2967 ns		10	–	3.0	6.0	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2175 ns		15	–	2.2	4.5	
Reset to Q_n	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 1415 ns		5.0	–	1500	3000	
t_{PHL} = (0.66 ns/pF) C_L + 567 ns		10	–	600	1200	
t_{PHL} = (0.5 ns/pF) C_L + 425 ns		15	–	450	900	
Clock Pulse Width	t_{WH}	5.0	600	300	–	ns
		10	200	100	–	
		15	170	85	–	
Clock Pulse Frequency	f_{cl}	5.0	–	1.2	0.4	MHz
(50% Duty Cycle)		10	–	3.0	1.5	
		15	–	5.0	2.0	
Clock Rise and Fall Time	t_{TLH},	5.0				–
	t_{THL}	10		No Limit		
		15				
Reset Pulse Width	t_{WH}	5.0	1000	500	–	ns
		10	400	200	–	
		15	300	150	–	

* The formulae given are for the typical characteristics only.

IN_1	Set	Reset	Clock Inh	Osc Inh	Out 1	Out 2	Decode Out
⌐¯	0	0	0	0	⌐¯	¯⌐	No Change
¯⌐	0	0	0	0	¯⌐	⌐¯	Advance to next state
X	1	0	0	0	0	1	1
X	0	1	0	0	0	1	0
X	0	0	1	0			No Change
0	0	0	0	X	0	1	No Change
1	0	0	0	⌐¯	¯⌐	⌐¯	Advance to next state

X = Don't Care

TRUTH TABLE

D	C	B	A	8-Bypass 0	8-Bypass 1
0	0	0	0	9	1
0	0	0	1	10	2
0	0	1	0	11	3
0	0	1	1	12	4
0	1	0	0	13	5
0	1	0	1	14	6
0	1	1	0	15	7
0	1	1	1	16	8
1	0	0	0	17	9
1	0	0	1	18	10
1	0	1	0	19	11
1	0	1	1	20	12
1	1	0	0	21	13
1	1	0	1	22	14
1	1	1	0	23	15
1	1	1	1	24	16

OPERATING CHARACTERISTICS

Set input initializes output to a "1". This is accomplished by setting an output conditioning latch to a 1 while at the same time resetting the 24 flip-flop stages. With the occurence of the first negative transition of the clock, the output will change to a "0". When the circuit is in the Set condition, the counter flip-flop stages will start counting on the second negative transition. The resulting behavior is the same as if each of the 24 flip-flop stages were set.

Reset inputs resets all stages to a logical "0". Reset or Set also disables the on-chip RC oscillator to allow very low power standby operation. In_1 input is used as the external Clock input or as the input to the on-chip RC oscillator.

Out 1, Out 2 outputs are used in the on-chip RC oscillator configuration.

8-Bypass input bypasses the first eight stages resulting in a 16-stage counter with all 16 stages selectable, one at a time. Clock Inhibit input disconnects the first counter stage from the input circuit, therefore inhibiting counting. This Clock Inhibit input is independent of the state of the Clock input. When the Clock Inhibit input is disabled, the counter will start counting only with the occurrence of the first negative edge of the Clock.

Binary Select inputs A, B, C, and D select the flip-flop stage to be connected to the output. Decode Out output can either be connected directly to a flip-flop output or to the monostable output. Osc Inhibit input can be used to disable the on-chip RC oscillator to allow very low power standby operation. Mono In input is used as the timing pin for the on-chip monostable oscillator. If the Mono In input is grounded through a resistor, the monostable circuit is disabled and the output is connected directly to the selected flip-flop. The monostable circuit is enabled if a resistor is connected between this pin and V_{DD} and a capacitor connected between this pin and ground. Any desired pulse width can be achieved depending upon the value of the R and C selected.

The test mode configuration divides the 24 flip-flop stages into three 8-stage sections to facilitate a fast test sequence. This test mode is enabled when 8-Bypass, Set and Reset are at a "1"

APPLICATIONS

FIGURE 1 – TIME INTERVAL CONFIGURATION USING EXTERNAL CLOCK; SET AND CLOCK INHIBIT FUNCTIONS

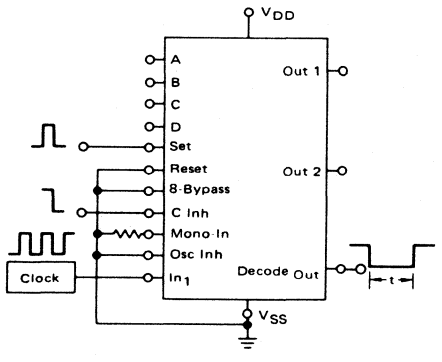


FIGURE 2 – TIME INTERVAL CONFIGURATION USING EXTERNAL CLOCK; RESET AND OUTPUT MONOSTABLE TO ACHIEVE A PULSE OUTPUT

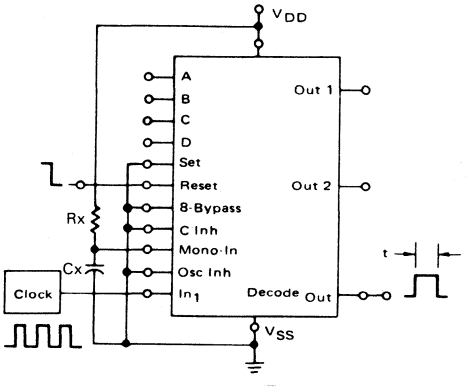
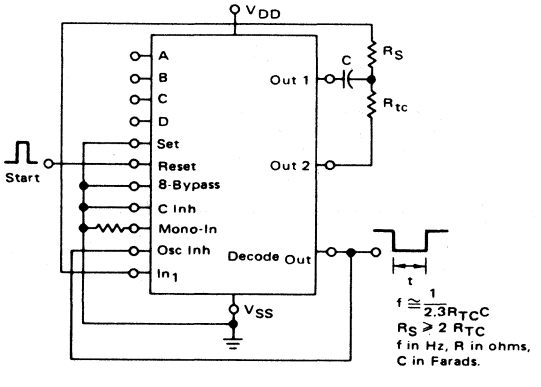
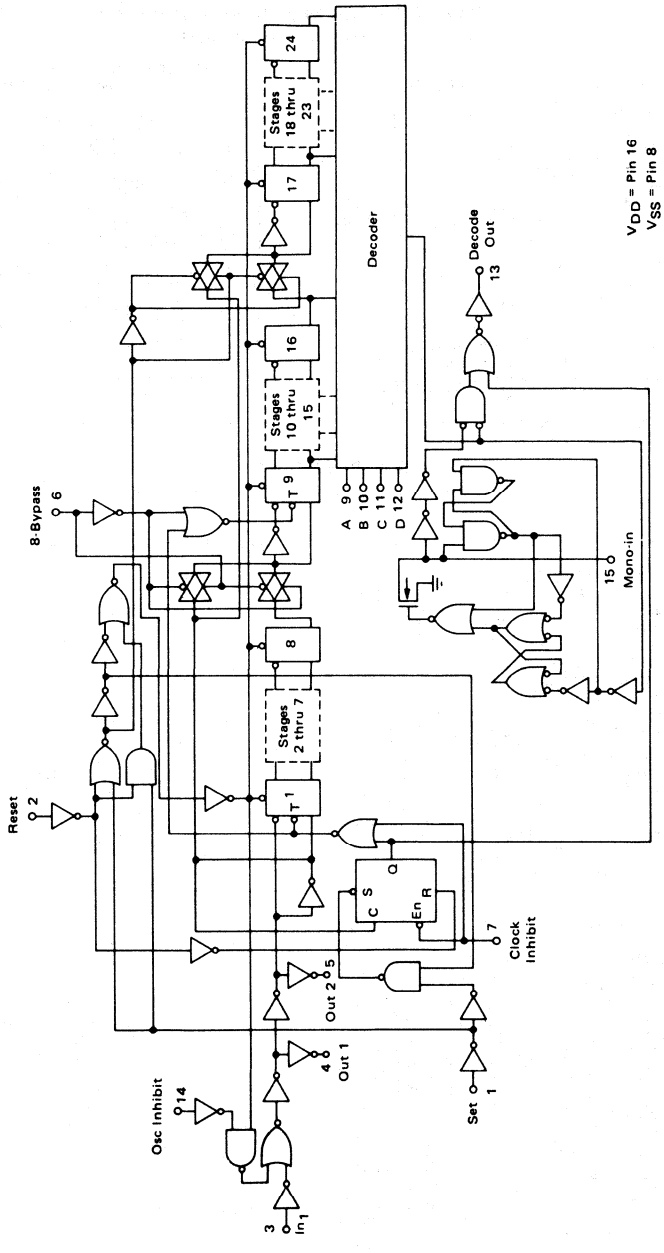


FIGURE 3 – TIME INTERVAL CONFIGURATION USING ON-CHIP RC OSCILLATOR AND RESET INPUT TO INITIATE TIME INTERVAL



LOGIC DIAGRAM



TYPICAL RC OSCILLATOR CHARACTERISTICS

(For Circuit Diagram See Figure 3 in Application)

FIGURE 4 – RC OSCILLATOR STABILITY

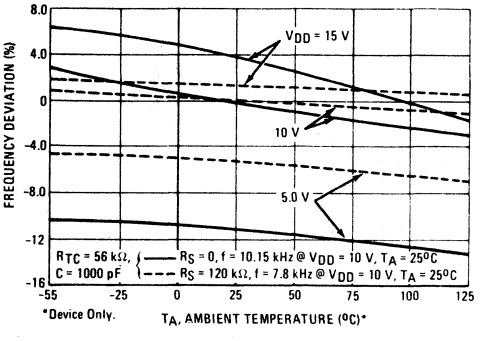
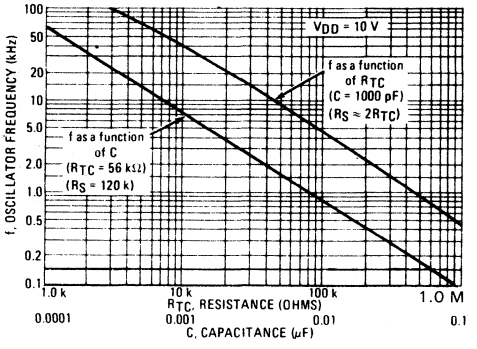


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C



3

MONOSTABLE CHARACTERISTICS

(For Circuit Diagram See Figure 2 in Application)

FIGURE 6 – TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 5.0 V

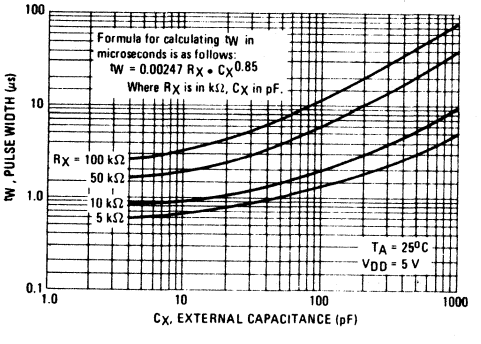


FIGURE 7 – TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 10 V

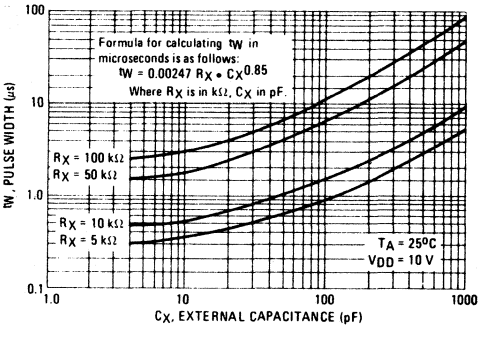
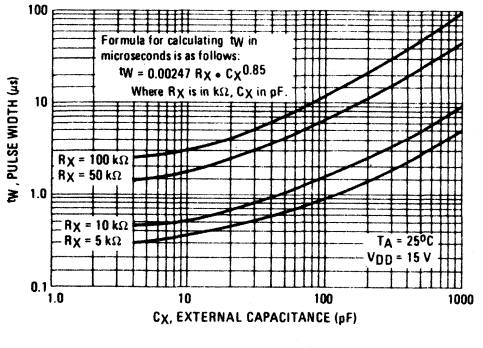


FIGURE 8 – TYPICAL C_X versus PULSE WIDTH @ V_{DD} = 15 V



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 9 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

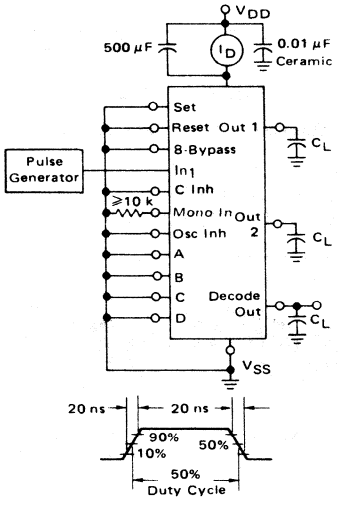
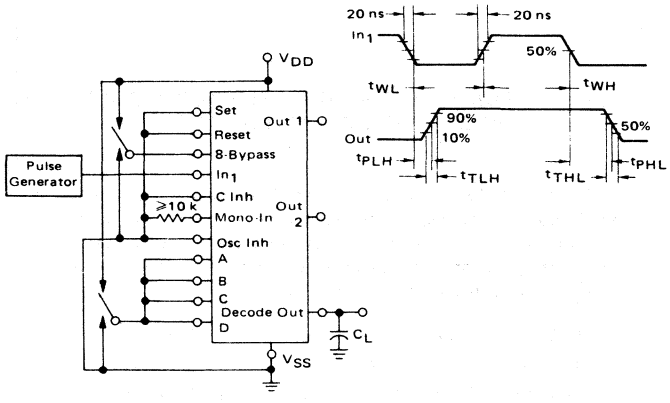


FIGURE 10 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

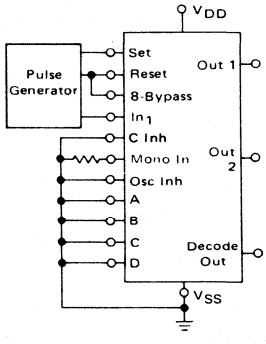


3

FUNCTIONAL TEST SEQUENCE

Test function (Figure 11) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into In_1 which will cause the counter to ripple from an all "1" state to an all "0" state.

FIGURE 11 – FUNCTIONAL TEST CIRCUIT



FUNCTIONAL TEST SEQUENCE

INPUTS				OUTPUTS	COMMENTS
In_1	Set	Reset	8-Bypass	Decade Out Q1 thru Q24	
1	0	1	1	0	All 24 stages are in Reset mode.
1	1	1	1	0	Counter is in three 8-stage sections in parallel mode.
0	1	1	1	0	First "1" to "0" transition of clock.
1 0 – – –	1	1	1		255 "1" to "0" transitions are clocked in the counter.
0	1	1	1	1	The 255 "1" to "0" transition.
0	0	0	0	1	Counter converted back to 24 stages in series mode. Set and Reset must be connected together and simultaneously go from "1" to "0".
1	0	0	0	1	In_1 Switches to a "1".
0	0	0	0	0	Counter Ripples from an all "1" state to an all "0" state.

MOTOROLA

MC14538B

CMOS MSI

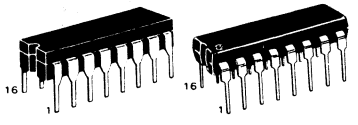
(LOW-POWER COMPLEMENTARY MOS)

DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

DUAL PRECISION RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR

The MC14538B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

- ±1.0% Typical Pulsewidth Variation from Part to Part
- ±0.5% Typical Pulsewidth Variation over Temperature Range
- New Formula: T = RC (T in seconds, R in ohms, C in farads)
- Pulse Width Range = 10 μs to ∞
- Symmetrical Output Sink and Source Capability
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- Quiescent Current (Standby) = 5.0 nA/package typical @ 5 Vdc
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive or Negative-Going Edge
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Pin-for-pin Compatible with MC14528B and CD4528B (CD4098)
- For new designs, the MC14548B is recommended for pulse widths greater than 1.0 μS and the MC14528B for pulse widths less than 1.0 μS.



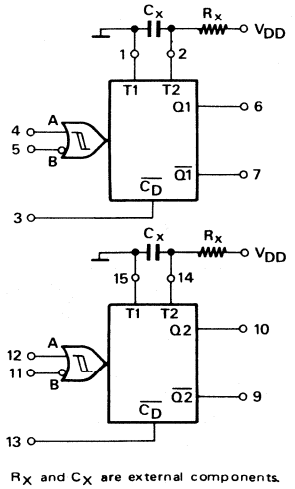
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



R_X and C_X are external components.

V_{DD} = Pin 16
V_{SS} = Pin 8, Pin 1, Pin 15

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current, Pin 2 or 14	I_{in}	15	–	±0.05	–	±0.00001	±.05	–	±0.5	μAdc
Input Current, Other Inputs (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current, Other Inputs (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance, Pin 2 or 14	C_{in}	–	–	–	–	25	–	–	–	pF
Input Capacitance, Other Inputs (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Quiescent Current, Active State	I_{DD}	5.0	–	–	–	35	–	–	–	μAdc
(Q1 = Logic 1)		10	–	–	–	80	–	–	–	
(Q2 = Logic 0)		15	–	–	–	125	–	–	–	
**Total Supply Current at an external load capacitance (C_L) and at external timing network (R_X, C_X)	I_T	5.0	$I_T = (3.5 \times 10^{-2}) R_X C_X f + 4 C_X f + 1 \times 10^{-5} C_L f$							
		10.0	$I_T = (8 \times 10^{-2}) R_X C_X f + 9 C_X f + 2 \times 10^{-5} C_L f$							
		15.0	$I_T = (1.25 \times 10^{-1}) R_X C_X f + 12 C_X f + 3 \times 10^{-5} C_L f$							
			where: I_T in μA (one monostable switching only), C_X in μF, C_L in pF, R_X in k ohms, and f in Hz is the input frequency.							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{TLH} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	–	100	200	
t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	–	50	100	
t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
A or B to Q or $\overline{Q}$						
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 255 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns		10	–	150	300	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 97 ns		15	–	100	220	
$\overline{C_D}$ to Q or $\overline{Q}$						ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 205 ns		5.0	–	250	500	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns		10	–	125	250	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 82 ns		15	–	95	190	
Input Pulse Width	t_{WH},	5.0	170	85	–	ns
A, B or C_D	t_{WL}	10	90	45	–	
		15	80	40	–	
Retrigger Time	t_{rr}	5.0	0	–	–	ns
		10	0	–	–	
		15	0	–	–	
Output Pulse Width — Q or $\overline{Q}$	T					µs
Refer to Figures 8 and 9 for other values of R_X and C_X.						
C_X = 0.002 µF, R_X = 100 kΩ		5.0	198	210	222	
		10	200	212	224	
		15	202	214	226	
C_X = 0.1 µF, R_X = 100 kΩ		5.0	9.3	9.86	10.4	ms
		10	9.5	10	10.5	
		15	9.6	10.14	10.7	
C_X = 10 µF, R_X = 100 kΩ		5.0	0.915	0.965	1.015	s
		10	0.93	0.98	1.03	
		15	0.94	0.99	1.04	
Pulse Width Match between circuits in	$100\frac{(T_1 - T_2)}{T_1}$	5.0	–	±5	±10	%
the same package.		10	–	±7.5	±15	
C_X = 0.1 µF, R_X = 100 kΩ		15	–	±7.5	±15	

* The formulae given are for the typical characteristics only.

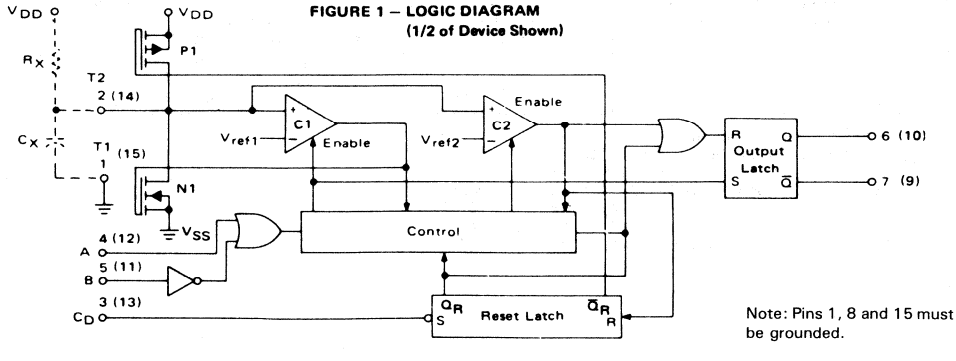
OPERATING CONDITIONS

External Timing Resistance	R_X	–	5.0	–	*	kΩ
External Timing Capacitance	C_X	–	0	–	No Limit†	µF

* The maximum usable resistance R_X is a function of the leakage of the capacitor C_X, leakage of the MC14538B, and leakage due to board layout and surface resistance. Susceptability to externally induced noise signals may occur for $R_X \geq$ 1 MΩ.

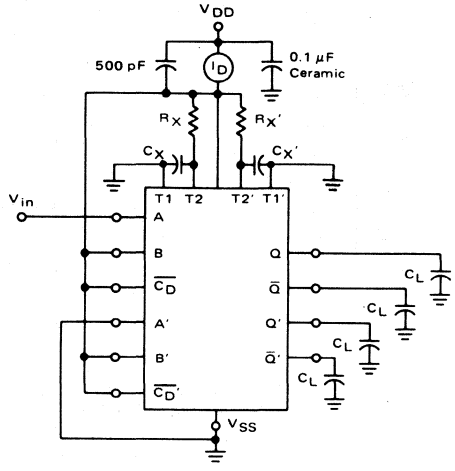
† If $C_X \geq$ 15 µF, use discharge protection diode per Fig. 11.

FIGURE 1 – LOGIC DIAGRAM
(1/2 of Device Shown)



Note: Pins 1, 8 and 15 must be grounded.

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



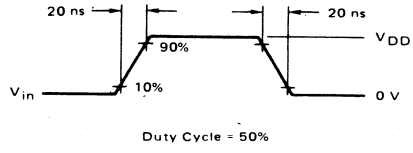
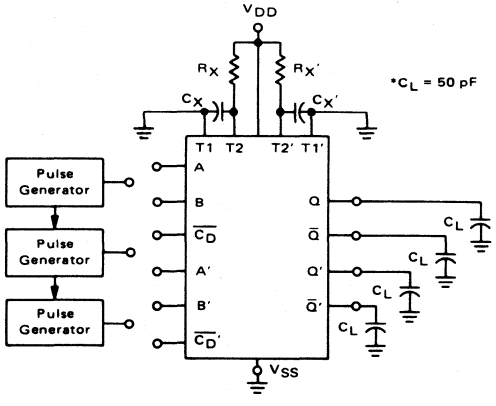


FIGURE 3 – SWITCHING TEST CIRCUIT



INPUT CONNECTIONS

CHARACTERISTICS	$\overline{C_D}$	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_{WH}, t_{WL}	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: Switching test waveforms for PG1, PG2, PG3 are shown in Figure 4.

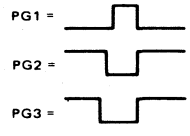


FIGURE 4 – SWITCHING TEST WAVEFORMS

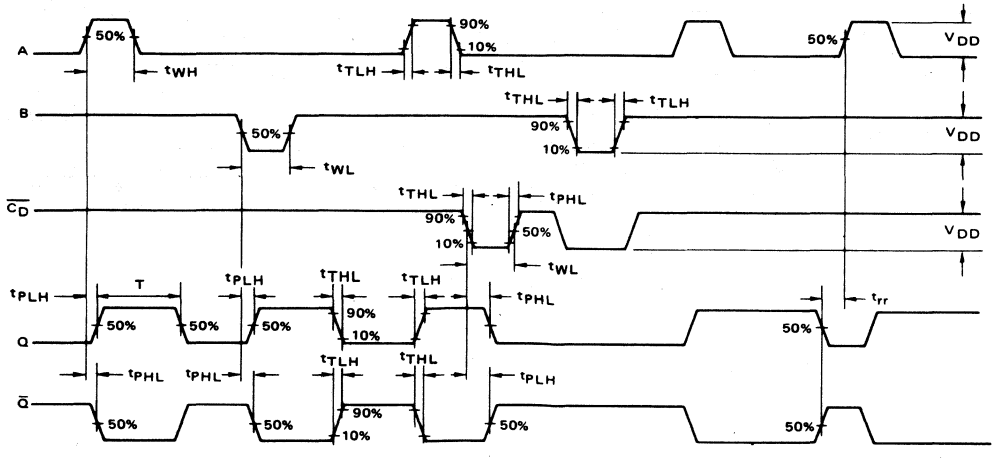


FIGURE 5 — TYPICAL NORMALIZED DISTRIBUTION OF UNITS FOR OUTPUT PULSE WIDTH

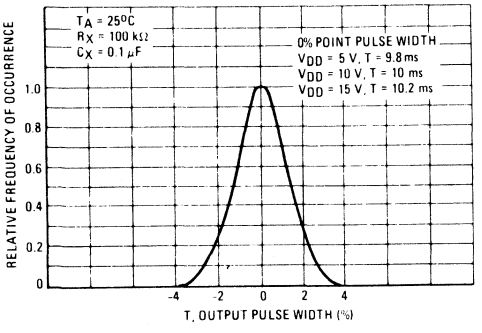


FIGURE 6 — TYPICAL PULSE WIDTH VARIATION AS A FUNCTION OF SUPPLY VOLTAGE V_{DD}

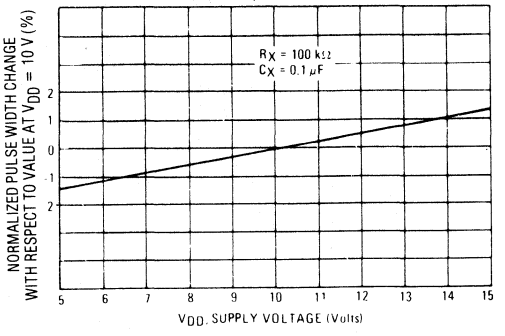


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FIGURE 7 — TYPICAL TOTAL SUPPLY CURRENT versus OUTPUT DUTY CYCLE

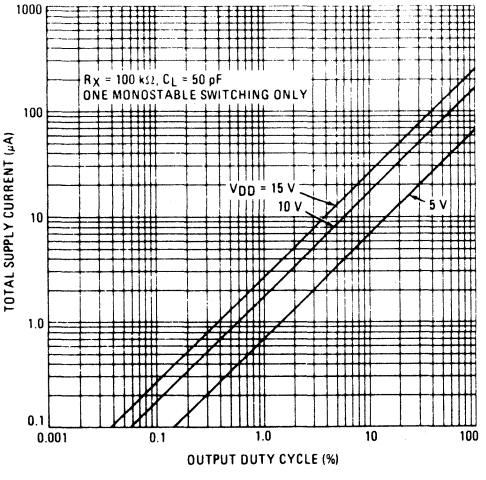
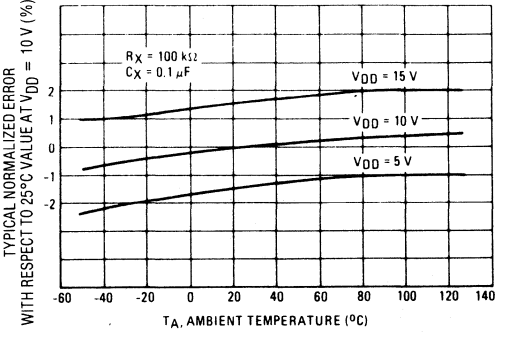


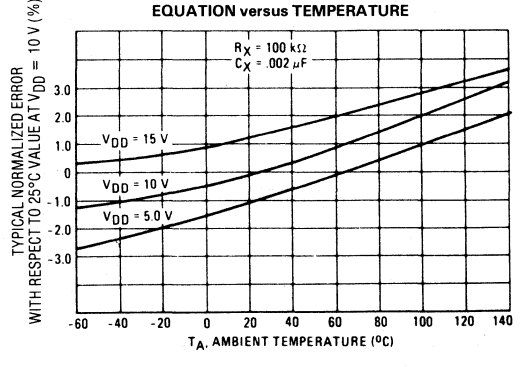
FIGURE 8 — TYPICAL ERROR OF PULSE WIDTH EQUATION versus TEMPERATURE



FUNCTION TABLE

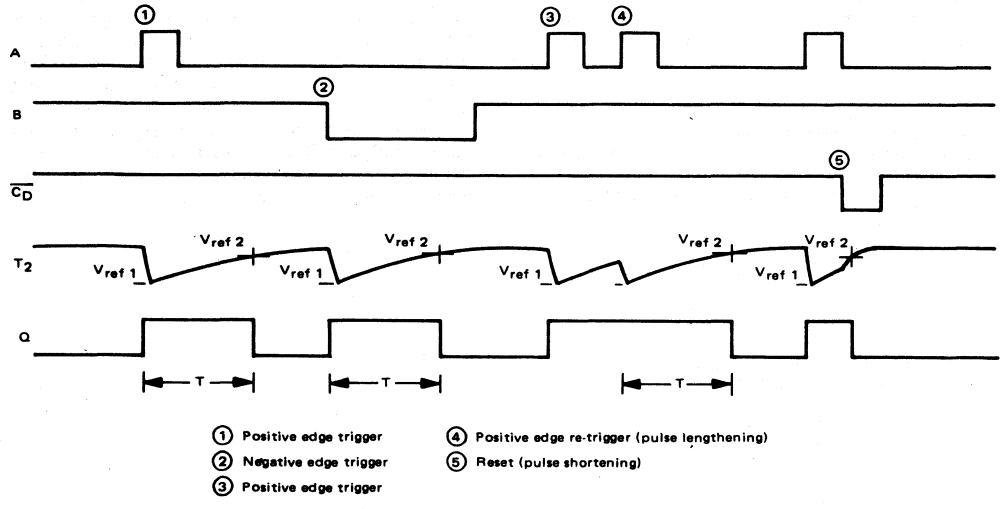
Inputs			Outputs	
Reset	A	B	Q	$\overline{Q}$
H	⌐	H	⌐⌐	⌐⌐
H	L	¬	⌐⌐	⌐⌐
H	⌐, ¬	L	Not Triggered	
H	H	⌐, ¬	Not Triggered	
H	L, H, ¬	H	Not Triggered	
H	L	L, H, ⌐	Not Triggered	
¬	X	X	L	H
¬⌐	X	X	Not Triggered	

FIGURE 9 — TYPICAL ERROR OF PULSE WIDTH EQUATION versus TEMPERATURE



THEORY OF OPERATION

FIGURE 10 – Timing Operation



TRIGGER OPERATION

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figures 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and $\overline{C_D}$ are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1①. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until $V_{ref\ 1}$ is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals $V_{ref\ 2}$, comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2②. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

It should be noted that in the quiescent state C_X is fully charged to V_{DD} causing the current through resistor R_X to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

RETRIGGER OPERATION

The MC14538B is retriggered if a valid trigger occurs ③followed by another valid trigger④before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from $V_{ref\ 1}$, but has not yet reached $V_{ref\ 2}$, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at T2 will again drop to $V_{ref\ 1}$ before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on $\overline{C_D}$ sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor P1⑤. When the voltage on the capacitor reaches $V_{ref\ 2}$, the

reset latch will clear, and will then be ready to accept another pulse. If the C_D input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

POWER-DOWN CONSIDERATIONS

Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the MC14538B (or MC14528B) is powered down, the capacitor voltage may discharge from V_{DD} through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the V_{DD} supply must not be faster than $(V_{DD})(C)/(10\ mA)$. For example, if V_{DD} = 10 V and C_X = 10 μF, the V_{DD} supply should discharge no faster than (10 V) × (10 μF)/(10 mA) = 10 ms. This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{DD} to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility use an external clamping diode, D_X, connected as show in Fig. 11.

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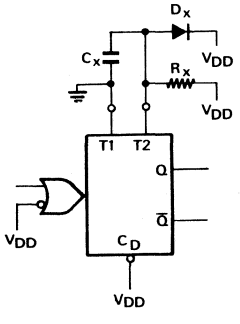
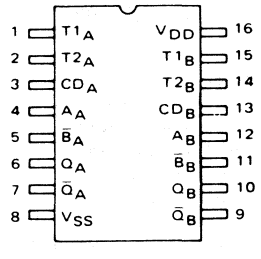
FIGURE 11 – USE OF A DIODE TO LIMIT POWER DOWN CURRENT SURGE



PIN ASSIGNMENT



TYPICAL APPLICATIONS

FIGURE 12 — RETRIGGERABLE MONOSTABLES CIRCUITRY

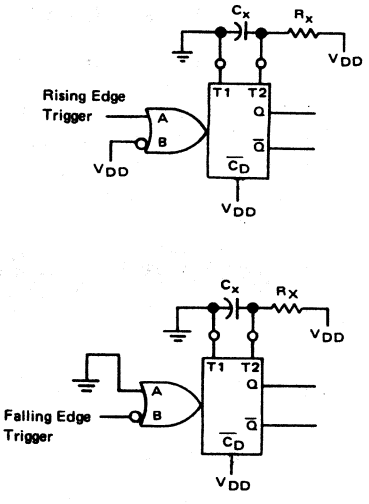


FIGURE 13 — NON-RETRIGGERABLE MONOSTABLES CIRCUITRY

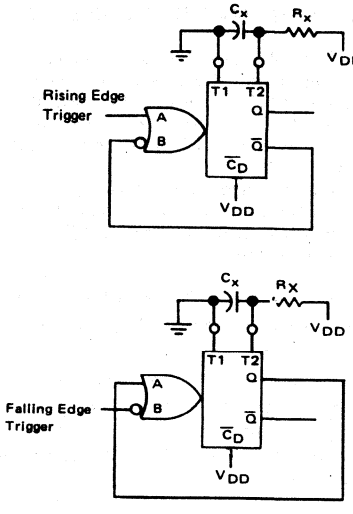


FIGURE 14 — REDUCTION OF POWER-UP OUTPUT PULSE WIDTH

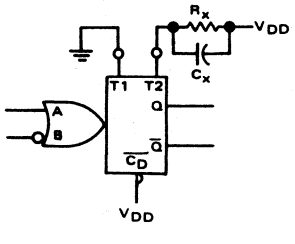
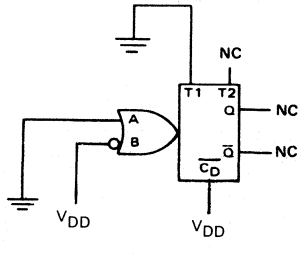


FIGURE 15 — CONNECTION OF UNUSED SECTIONS



MOTOROLA

MC14539B

DUAL 4-CHANNEL DATA SELECTOR/MULTIPLEXER

The MC14539B data selector/multiplexer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of two sections of four inputs each. One input from each section is selected by the address inputs A and B. A "high" on the Strobe input will cause the output to remain "low".

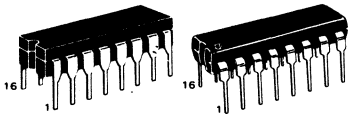
This device finds primary application in signal multiplexing functions. It permits multiplexing from N-lines to I-line, and can also perform parallel-to-serial conversion. The Strobe input allows cascading of n-lines to n-lines.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- High Fanout >50
- Input Impedance = 10^{12} ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-CHANNEL
DATA SELECTOR/MULTIPLEXER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

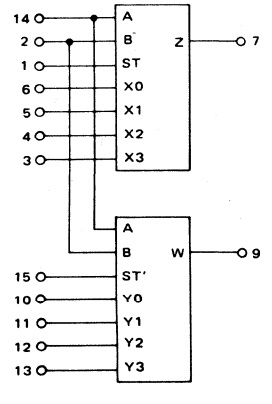
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range -- AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS					
		X3	X2	X1	X0		OUTPUTS
B	A	Y3	Y2	Y1	Y0	ST,ST'	Z, W
X	X	X	X	X	X	1	0
0	0	X	X	X	0	0	0
0	0	X	X	X	1	0	1
0	1	X	X	0	X	0	0
0	1	X	X	1	X	0	1
1	0	X	0	X	X	0	0
1	0	X	1	X	X	0	1
1	1	0	X	X	X	0	0
1	1	1	X	X	X	0	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–			–	5.0	7.5	–		pF
Quiescent Current (AL Device)	I_{DD}	5.0		5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10		10	–	0.010	10	–	300	
		15		20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.85\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (1.7\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (2.6\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

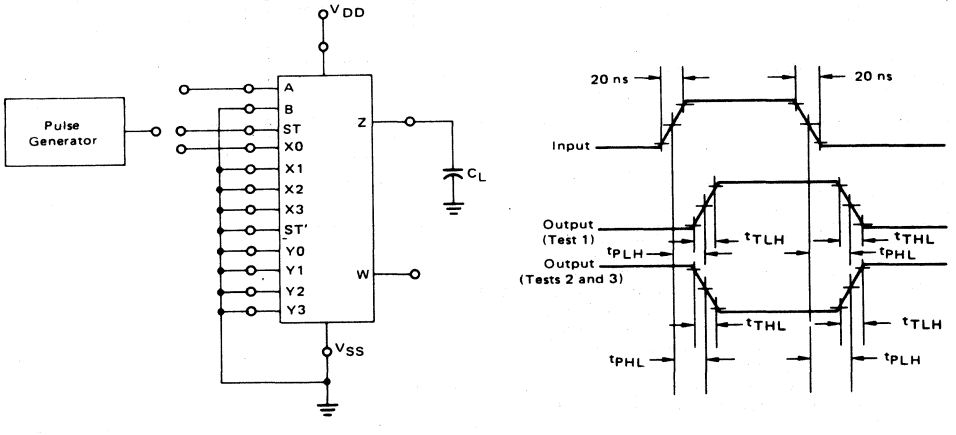
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
X, Y Input to Output						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 125 ns		5.0	–	210	420	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{PLH}, t_{PHL} = (0.55 ns/pF) C_L + 45 ns		15	–	70	140	
A Input to Output	t_{PLH}					ns
t_{PLH} = (1.7 ns/pF) C_L + 140 ns		5.0	–	225	450	
t_{PLH} = (0.66 ns/pF) C_L + 77 ns		10	–	110	220	
t_{PLH} = (0.5 ns/pF) C_L + 60 ns		15	–	85	170	
t_{PHL} = (1.7 ns/pF) C_L + 160 ns	t_{PHL}	5.0	–	245	490	ns
t_{PHL} = (0.66 ns/pF) C_L + 82 ns		10	–	115	230	
t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	–	90	180	
Strobe Input to Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 60 ns		5.0	–	145	290	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns		15	–	60	120	

* The formulae given are for the typical characteristics only.

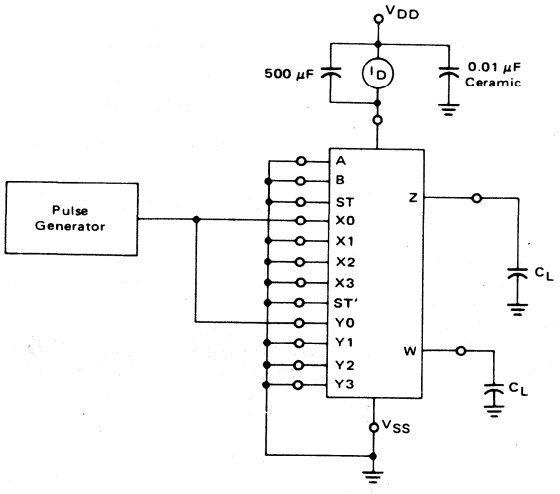
FIGURE 1 – AC TEST CIRCUIT AND WAVEFORMS

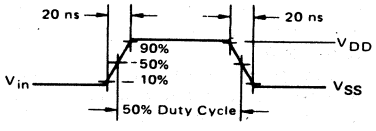


Input Connections for t_{TLH}, t_{THL}, t_{PHL}, t_{PLH}

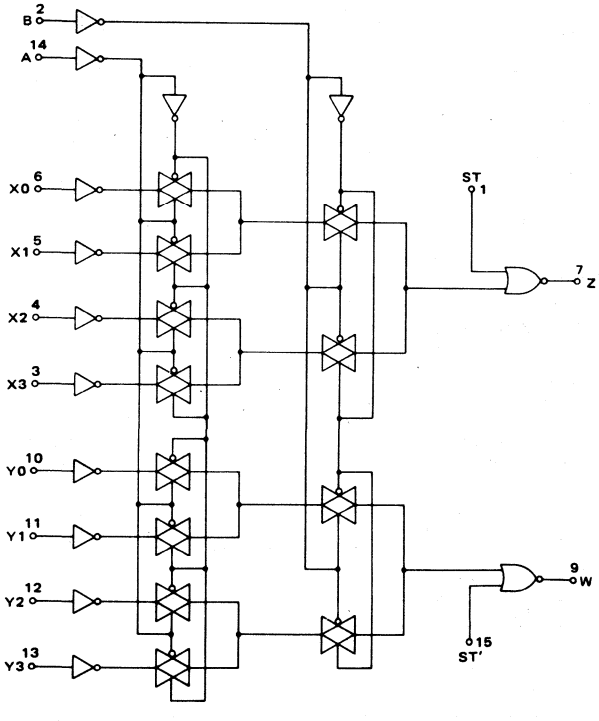
TEST	STROBE	A	X0
1	Gnd	Gnd	P. G
2	P. G.	Gnd	V_{DD}
3	Gnd	P. G.	V_{DD}

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

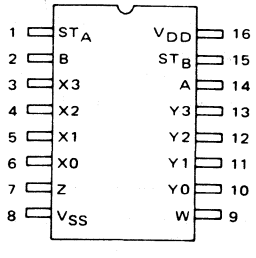




LOGIC DIAGRAM



PIN ASSIGNMENT



MOTOROLA

MC14541B

PROGRAMMABLE TIMER

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

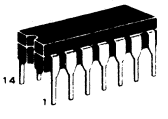
OSCILLATOR/TIMER

3

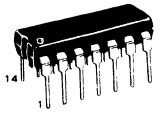
The MC14541B programmable timer consists of a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the power-on reset is enabled and initializes the counter, within the specified V_{DD} range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency (f_{osc}) with the n^{th} stage frequency being $f_{osc}/2^n$.

- Available Outputs 2^8, 2^{10}, 2^{13} or 2^{16}
- Increments on Positive Edge Clock Transitions
- Low Symmetrical Output Resistance (typically 100 Ω at 15 Vdc)
- Built-in Low Power RC Oscillator (± 2% accuracy over temperature range and ± 20% supply and ± 3% over processing at < 10 kHz)
- Oscillator Frequency Range ≈ DC to 100 kHz
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as 2^n Frequency Divider or Single Transition Timer
- Q/$\overline{Q}$ Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow CLock Rise and Fall Times
- Automatic Reset Initializes All Counters When Power Turns On (Limits – V_{DD} from 8.5 Vdc to 18 Vdc when enabled)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc with Auto Reset Disables (Pin 5 = V_{DD})
  = 8.5 Vdc to 18 Vdc with Auto Reset Enabled (Pin 5 = GND)



L SUFFIX
CERAMIC PACKAGE
CASE 632

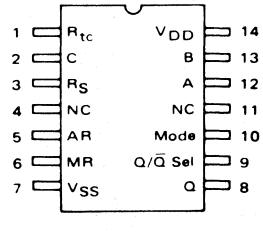


P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



NC = No Connection

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Input	I	10	mAdc
DC Current Drain per Output	I	45	mAdc
Operating Temperature Range Al Device CL/CP Device	T_A	 −55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	7.96	–	6.42	12.83	–	4.49	–	
(V_{OH} = 9.5 Vdc)		10	4.19	–	3.38	6.75	–	2.37	–	
(V_{OH} = 13.5 Vdc)		15	16.3	–	13.2	26.33	–	9.24	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.93	–	1.56	3.12	–	1.09	–	mAdc
(V_{OL} = 0.5 Vdc)		10	4.96	–	4.0	8.0	–	2.8	–	
(V_{OL} = 1.5 Vdc)		15	19.3	–	15.6	31.2	–	10.9	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	5.1	–	4.27	12.83	–	3.5	–	
(V_{OH} = 9.5 Vdc)		10	2.69	–	2.25	6.75	–	1.85	–	
(V_{OH} = 13.5 Vdc)		15	10.5	–	8.8	26.33	–	7.22	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.24	–	1.04	3.12	–	0.85	–	
(V_{OL} = 0.5 Vdc)		10	3.18	–	2.66	8.0	–	2.18	–	
(V_{OL} = 1.5 Vdc)		15	12.4	–	10.4	31.2	–	8.50	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)										µAdc
		5.0	–	5.0	–	0.005	5.0	–	150	
(Pin 5 is High)	I_{DD}	10	–	10	–	0.010	10	–	300	
Auto Reset Disabled		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)										µAdc
		5.0	–	20	–	0.005	20	–	150	
(Pin 5 is High)	I_{DD}	10	–	40	–	0.010	40	–	300	
Auto Reset Disabled		15	–	80	–	0.015	80	–	600	
Auto Reset Quiescent Current										µAdc
	I_{DDR}	10	–	250	–	30	250	–	1500	
(Pin 5 is low)		15	–	500	–	82	500	–	2000	
Supply Current**† (Dynamic plus Quiescent)	I_D	5.0	I_D = (0.4 µA/kHz) f + I_{DD}							µAdc
		10	I_D = (0.8 µA/kHz) f + I_{DD}							
		15	I_D = (1.2 µA/kHz) f + I_{DD}							

*T_{low} = –55°C for AL Device, –40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†When using the on chip oscillator the total supply current (in µAdc) becomes : $I_T = I_D + 2\ C_{tc}\ V_{DD}\ f \times 10^{-3}$ where I_D is in µA, C_{tc} is in pF, V_{DD} in Volts DC, and f in kHz. (see fig. 3)
Dissipation during power-on with automatic reset enabled is typically 50µA @ V_{DD} = 10Vdc.
**The formula given is for the typical characteristics only.

SWITCHING CHARACTERISITCS* (C_L = 50 pF, T_A = 25°C)

Characteristic	V_{DD} Symbol	Typical Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay, Clock to Q (2^8 Output)	t_{PLH}					µs
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 3415 ns	t_{PHL}	5.0	–	3.5	10.5	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 1217 ns		10	–	1.25	3.8	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 875 ns		15	–	0.9	2.9	
Propagation Delay, Clock to Q (2^{16} Output)	t_{PHL}					µs
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 5915 ns	t_{PLH}	5.0	–	6.0	18	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 3467 ns		10	–	3.5	10	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 2475 ns		15	–	2.5	7.5	
Clock Pulse Width	$t_{WH(cl)}$	5.0	900	300	–	ns
		10	300	100	–	
		15	225	85	–	
Clock Pulse Frequency (50% Duty Cycle)	f_{cl}	5.0	–	1.5	–	MHz
		10	–	4.0	–	
		15	–	6.0	–	
MR Pulse Width	$t_{WH(R)}$	5.0	900	300	–	ns
		10	300	100	–	
		15	225	85	–	

* The formulae given are for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

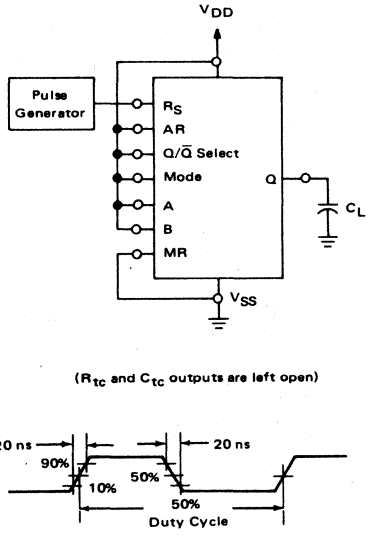
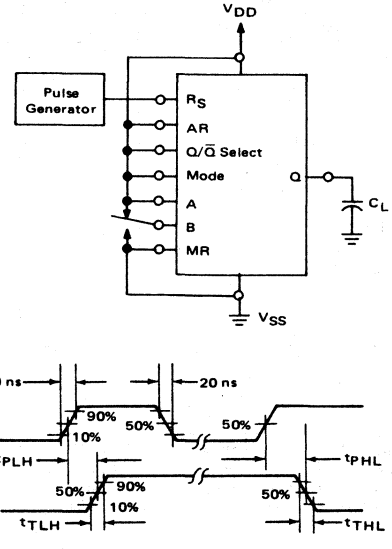
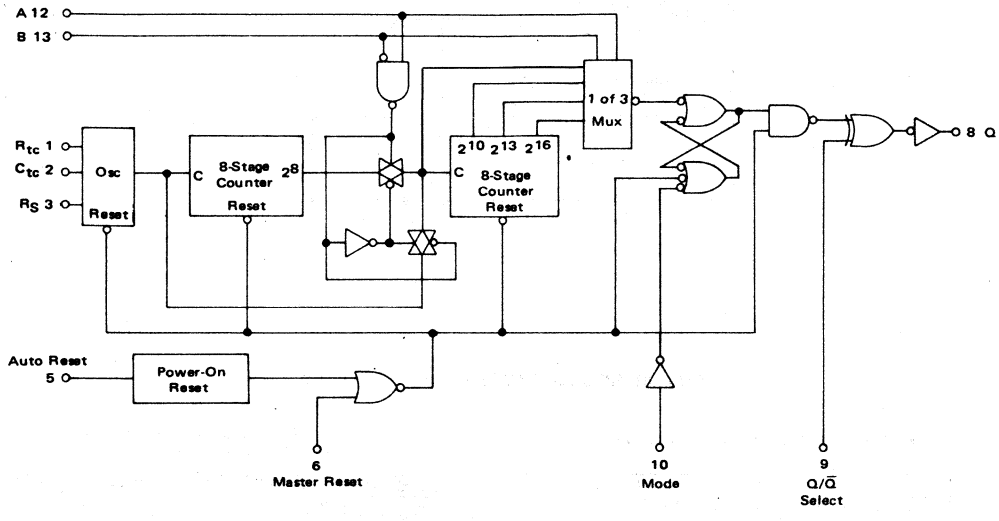


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



EXPANDED BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

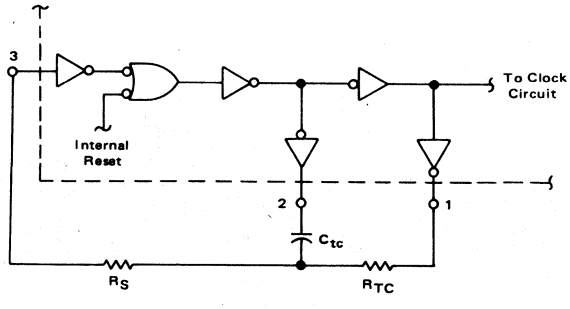
FREQUENCY SELECTION TABLE

A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

TRUTH TABLE

Pin	State	
	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset On
9	Output Initially Low After Reset	Output Initially High After Reset
10	Single Cycle Mode	Recycle Mode

FIGURE 3 – OSCILLATOR CIRCUIT USING RC CONFIGURATION



3

TYPICAL RC OSCILLATOR CHARACTERISTICS

FIGURE 4 – RC OSCILLATOR STABILITY

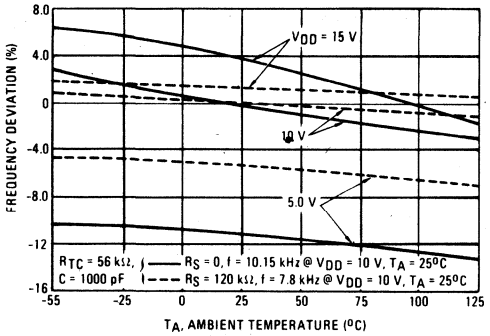
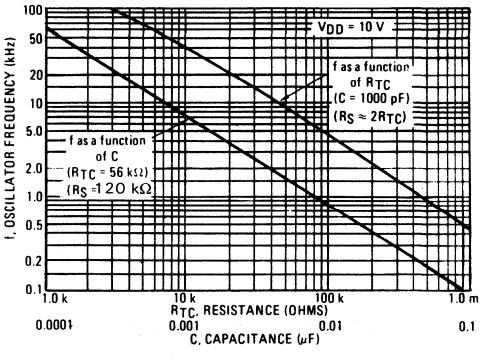


FIGURE 5 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C_{TC}



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

OPERATING CHARACTERISTICS

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a "1" provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

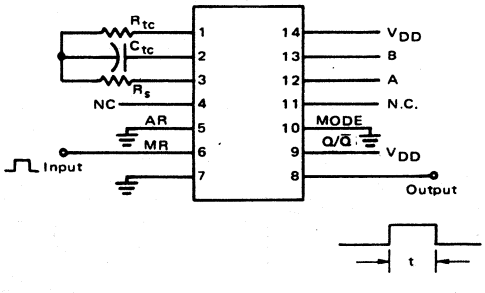
$$f = \frac{1}{2.3\,R_{tc}C_{tc}} \quad \text{if } (1\ \text{kHz} \leqslant f \leqslant 100\ \text{kHz})$$

and $R_S \approx 2\,R_{tc}$ where $R_S \geqslant 10\ \text{k}\Omega$

The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13} and 2^{16}). The 2^n counts as shown in the Frequency Selection Table represents the Q output of the N^{th} stage of the counter. When A is "1", 2^{16} is selected for both states of B. However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputing 2^8).

The $Q/\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and $Q/\overline{Q}$ select pin is set to a "0" the Q output is a "0", correspondingly when $Q/\overline{Q}$ select pin is set to a "1" the Q output is a "1".

When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop (see Expanded Block Diagram) resets, counting commences, and after 2^{n-1} counts the RS flip-flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.



DIGITAL TIMER APPLICATION

When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high until the selected (via A and B) number of clock pulses are counted, the Q output then goes low and remains low until another input pulse is received.

This "one shot" is fully retriggerable and as accurate as the input frequency. An external clock can be used (pin 3 is the clock input, pins 1 and 2 are outputs) if additional accuracy is needed.

Notice that a setup time equal to the desired pulse width output is required immediately following initial power up, during which time Q output will be high.

MOTOROLA

MC14548B

Advance Information

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL (RETRIGGERABLE, RESETTABLE) MONOSTABLE MULTIVIBRATOR

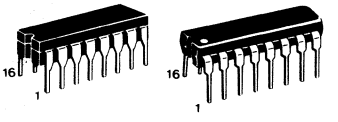
3

DUAL MONOSTABLE MULTIVIBRATOR (RETRIGGERABLE, RESETTABLE)

The MC14548B is identical in pinout to the MC14538B and the MC14528B.

This dual monostable multivibrator may be triggered by either the positive or the negative edge of an input pulse, and will produce an output pulse over a wide range of pulse widths. Because the device has conditioned trigger inputs, there are no trigger-input rise and fall time restrictions. The output pulse width is determined by the external timing components, R_X and C_X. The device has a reset function which forces the $\overline{Q}$ output low and Q output high, regardless of the state of the output pulse circuitry.

- Unlimited Rise and Fall Times Allowed on the Trigger Inputs
- Output Pulse Width is Independent of the Trigger Pulse Width
- Latched Trigger and Reset Inputs
- Supply Voltage Range = 3.0 to 18.0 Vdc
- Recommended for all new designs in lieu of the 14528B and 14538B
- For pulse widths < 1 µs, use the HC4538 or MC14528B



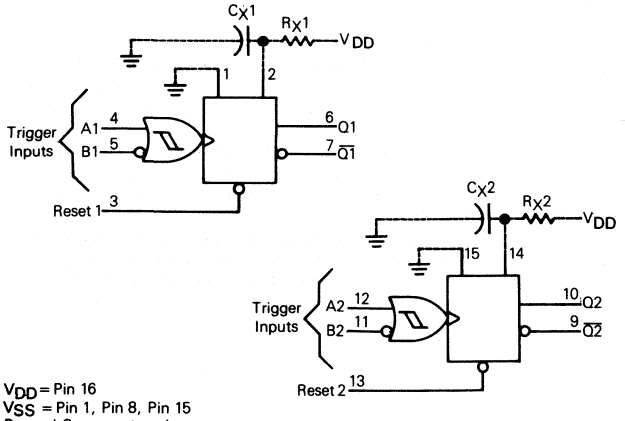
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

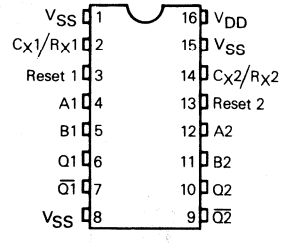
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 1, Pin 8, Pin 15
R_X and C_X are external components

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs	
Reset	A	B	Q	$\overline{Q}$
H	↓	H	⊓	⊔
H	L	↓	⊓	⊔
H	↓,↑	L	Not Triggered	
H	H	↓,↑	Not Triggered	
H	L, H, ↑	H	Not Triggered	
H	L	L, H, ↓	Not Triggered	
L	X	X	L	H
↓,↑	X	X	Not Triggered	

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Oct. 1983 EUR

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range L Device P Device	T_A	 −55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended than V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD}	T_{low}*		25°C			T_{high}*		Unit
			Vdc	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage V_{in} = V_{DD} or 0	"0" Level	V_{OL}	5.0 10 15	– – –	0.05 0.05 0.05	– – –	0 0 0	0.05 0.05 0.05	– – –	0.05 0.05 0.05	V
V_{in} = 0 or V_{DD}	"1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.0 10 15	– – –	4.95 9.95 14.95	– – –	V
Input Voltage**	"0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									V
(V_O = 0.5 or 4.5 Vdc)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current		I_{OH}									mA
(V_{OH} = 2.5 Vdc)	Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)			5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)			10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)			15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mA
(V_{OL} = 0.5 Vdc)			10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	8.8	–	2.4	–	
Input Current, Pin 2 or 14		I_{in}	15	–	±0.05	–	± 0.00001	±0.05	–	±0.5	µA
Input Current, Other Inputs		I_{in}	15	–	±0.1	–	± 0.00001	±0.1	–	±1.0	µA
Input Capacitance, Pin 2 or 14		C_{in}	–	–	–	–	25	–	–	–	pF
Input Capacitance, Other Inputs (V_{in} = 0)		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current, Standby State		I_{DD}	5.0	–		–	10	20	–		µA
(Q = Logic 0)			10	–		–	25	40	–		
($\overline{Q}$ = Logic 1)			15	–		–	50	80	–		
Quiescent Current, Active State		I_{DD}	5.0	–	–	–		–	–	–	µA
(Q = Logic 1)			10	–	–	–		–	–	–	
($\overline{Q}$ = Logic 0)			15	–	–	–		–	–	–	

* T_{low} = −55°C for L Device, −40°C for P Device.
T_{high} = +125°C for L Device, +85°C for P Device.

** Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min at V_{DD} = 5.0 Vdc
2.0 Vdc min at V_{DD} = 10 Vdc
2.5 Vdc min at V_{DD} = 15 Vdc

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Output Transition Time Q or $\overline{Q}$	t_{TLH}, t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Propagation Delay Time A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	5.0	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
Reset to Q or $\overline{Q}$		5.0	–	185	370	ns
		10	–	90	180	
		15	–	75	150	
Input Pulse Width A, B or Reset	PW_{in}	5.0	50	25	–	ns
		10	30	15	–	
		15	20	10	–	
Retrigger Time Input A or B	t_{rr}	5.0			–	ns
		10			–	
		15			–	
Recovery Time Reset Inactive to A or B	t_{rec}	5.0			–	ns
		10			–	
		15			–	
Input Rise and Fall Time Reset	t_r, t_f	5	–	–	15	µs
		10	–	–	5	
		15	–	–	4	
Input A or B		–	no limit			µs
Output Pulse Width – Q or $\overline{Q}$ C_X = 15 pF, R_X = 5 KΩ	T	5.0		1340		µs
		10		710		
		15		540		
C_X = 0.01 µF, R_X = 10 KΩ		5.0		90.5		ms
		10		77		
		15		73		
C_X = 1.0 µF, R_X = 100 KΩ		5.0		58		s
		10		56		
		15		49		
Pulse Width Match between circuits in the same package C_X = 0.1 µF, R_X = 100 kΩ	$\frac{T_1 - T_2}{T_1}$	5.0	–	±1	–	%
		10	–	±1	–	
		15	–	±1	–	

OPERATING CONDITIONS

External Timing Resistance	R_X	–	5.0	–	*	kΩ
External Timing Capacitance	C_X	–	0	–	*	pF

* The maximum allowable values of R_X and C_X are a function of the leakage of capacitor C_X, the leakage of the MC14548B, and leakage due to board layout and surface resistance. Values of R_X and C_X should be chosen so that the maximum current into pin 2 or pin 14 is 10 mA. Susceptibility to externally induced noise signals may occur for R_X > 1 MΩ.

PIN DESCRIPTIONS

INPUTS

A1, A2 (Pins 4, 12) — Positive-edge trigger inputs. A rising-edge signal on either of these pins will trigger the corresponding multivibrator when there is a high voltage level on the B1 or B2 input.

B1, B2 (Pins 5, 11) — Negative-edge trigger inputs. A falling-edge signal on either of these pins will trigger the corresponding multivibrator when there is a low voltage level on the A1 or A2 input.

Reset 1, Reset 2 (Pins 3, 13) — Reset inputs (active low). When a low voltage is applied to one of these pins, the Q output of the corresponding multivibrator is reset to a low voltage and the $\overline{Q}$ output is set to a high voltage.

C_X1/R_X1 and C_X2/R_X2 (Pins 2 and 14) — External timing components. These pins are tied to the common points of the external timing resistors and capacitors (see the Block Diagram).

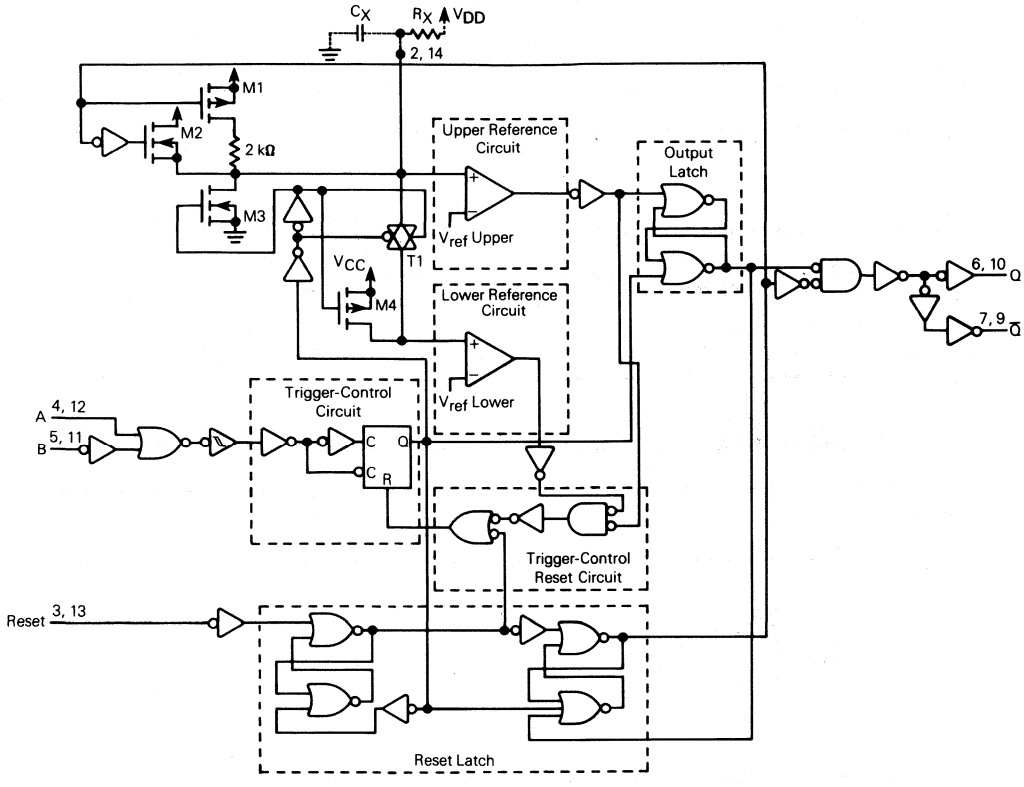
V_{SS} (Pins 1 and 15) — External ground. The external timing capacitors discharge to ground through these pins.

OUTPUTS

Q1, Q2 (Pins 6, 10) — Noninverted monostable outputs. These pins (normally low) pulse high when the multivibrator is triggered at either the A or the B input. The width of the pulse is determined by the external timing components, R_X and C_X.

$\overline{Q}1$, $\overline{Q}2$ (Pins 7, 9) — Inverted monostable outputs. These pins (normally high) pulse low when the multivibrator is triggered at either the A or the B input. These outputs are the inverse of Q1 and Q2.

FIGURE 1 — FUNCTION DIAGRAM
(½ the device)



CIRCUIT OPERATION

Figure 4 shows the 14548B configured in the retriggerable mode. Briefly, the device operates as follows (refer to Figure 1). In the quiescent state, the external timing capacitor, C_X, is charged to V_{DD}. When a trigger occurs, the Q output goes high and C_X discharges quickly to the lower reference voltage (V_{ref} Lower $\approx$ 1/3 V_{DD}). C_X then charges, through R_X, back up to the upper reference voltage (V_{ref} Upper $\approx$ 2/3 V_{DD}), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the function diagram (Figure 1) and the timing diagram (Figure 2).

QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (# 1 in Figure 2). Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (# 2, Figure 2).

The output of the trigger-control is low (# 3), and transistors M1, M2, and M3 are turned off. The external timing capacitor, C_X, is charged to V_{DD} (# 4), and the upper reference circuit has a low output (# 5). Transistor M4 is turned on and transmission gate T1 is turned off. Thus the lower reference circuit has V_{DD} at the noninverting input and a resulting low output (# 6).

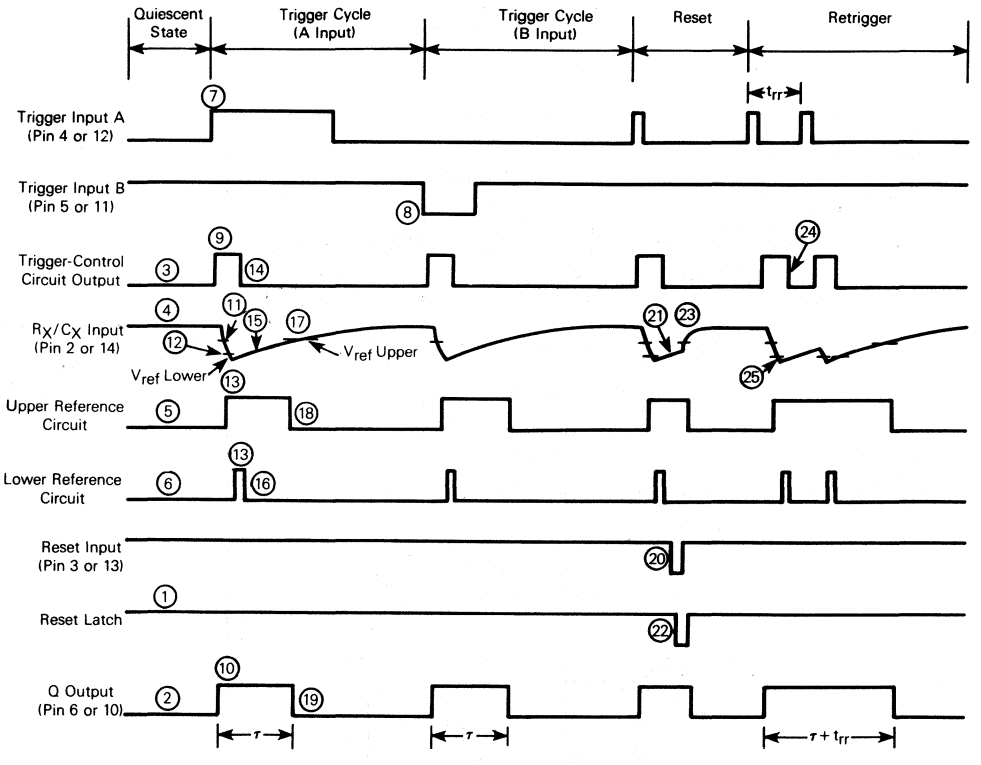
In addition, the output of the trigger-control reset circuit is low.

TRIGGER OPERATION

The 14548B is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (# 8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

The trigger-control circuit going high simultaneously in-

FIGURE 2 – TIMING DIAGRAM



tiates three events. First, the output latch goes low, thus taking the Q output of the 14548B to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, C_X, to rapidly discharge toward ground (#11). (Note that the voltage across C_X appears at the input of the upper reference circuit comparator). Third, transistor M4 is turned off and transmission gate T1 is turned on, thus allowing the voltage across C_X to also appear at the input of the lower reference circuit comparator.

When C_X discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing C_X to begin to charge back up toward V_{DD}, with a time constant $t = R_X C_X$ (#15). In addition, transistor M4 is turned on and transmission gate T1 is turned off. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go low (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes low.

When C_X charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the 14548B to a low state (#19), and completing the time-out cycle.

RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the 14548B to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while C_X is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus C_X is allowed to quickly charge up to V_{DD} (#23) to await the next trigger signal.

RETRIGGER OPERATION

When used in the retriggerable mode (Figure 4), the 14548B may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time, t_{rr} (Figure 1) is a function of internal propagation delays and the discharge time of C_X.

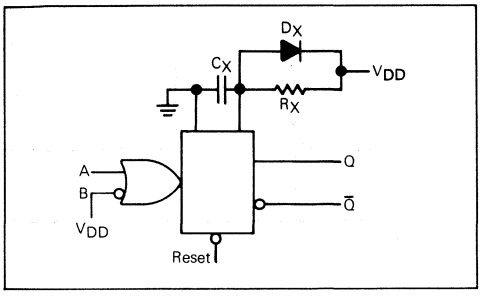
Figure 5 shows the device configured in the non-retriggerable mode.

POWER-DOWN CONSIDERATIONS

Large values of C_X may cause problems when powering down the 14548B because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{DD} through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 10 mA, therefore, the turn-off time of the V_{DD} power supply must not be faster than $t = V_{DD} \cdot C_X/(10\ mA)$. For example, if $V_{DD} = 5$ V and $C_X = 15\ \mu F$, the V_{DD} supply must turn off no faster than $t = (5\ V) \bullet (15\ \mu F)/10\ mA = 7.5$ ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{DD} to zero volts occurs, the 14548B may sustain damage. To avoid this possibility, use an external clamping diode, D_X, connected as shown in Figure 3.

FIGURE 3 — LATCH-UP PROTECTION DURING POWER DOWN



3

TYPICAL APPLICATIONS

FIGURE 4 — RETRIGGERABLE MONOSTABLE CIRCUITRY

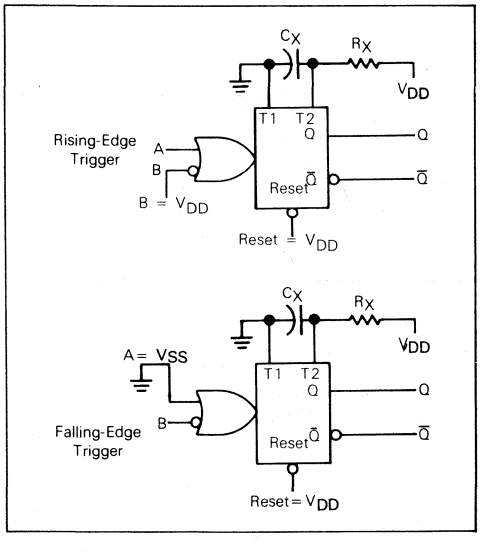
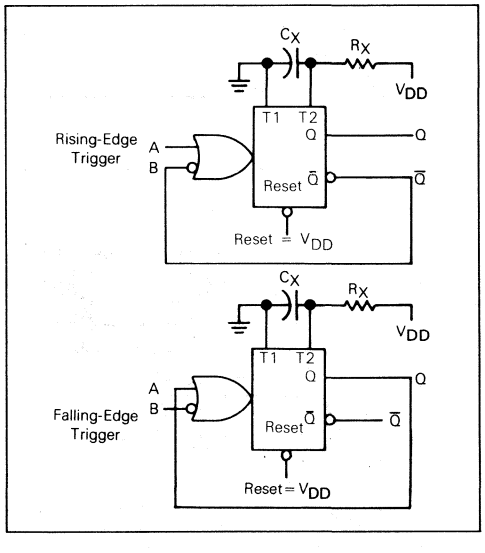


FIGURE 5 — NONRETRIGGERABLE MONOSTABLE CIRCUITRY



SWITCHING WAVEFORMS

FIGURE 6

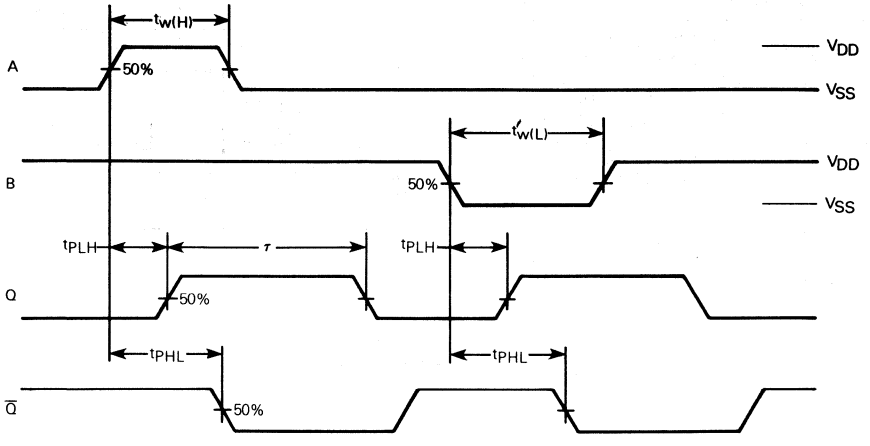


FIGURE 7

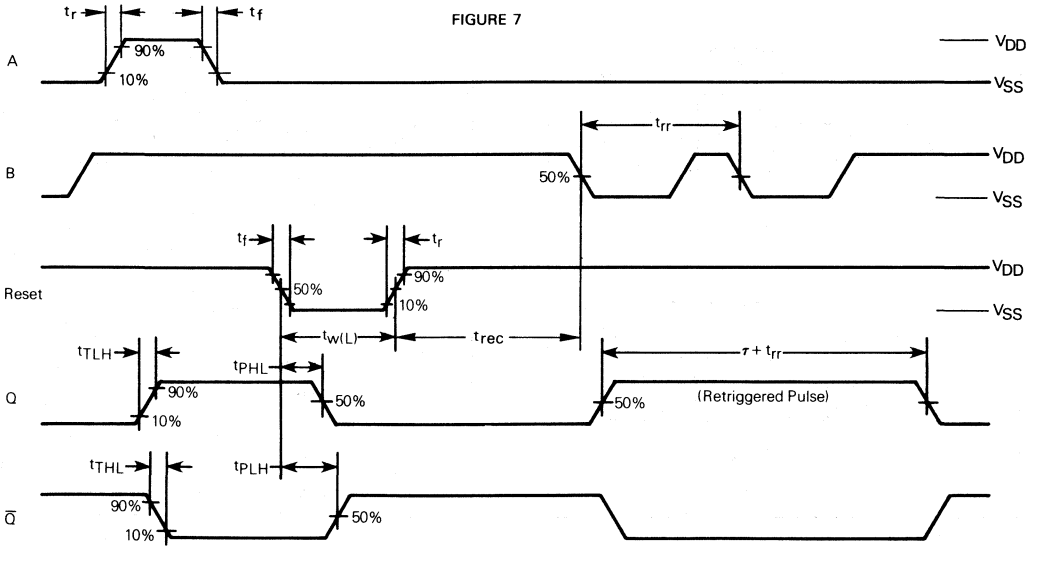
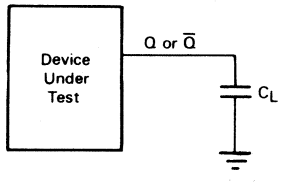


FIGURE 8 — TEST CIRCUIT



MOTOROLA

MC14551B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

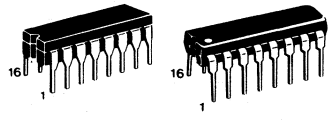
QUAD 2-INPUT ANALOG MULTIPLEXER/ DEMULTIPLEXER

3

QUAD 2-INPUT ANALOG MULTIPLEXER/DEMULTIPLEXER

The MC14551B is a digitally controlled analog switch. It is an effective 4 PDT switch with low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

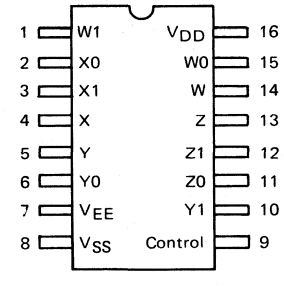
- High On/Off Output Ratio — 65 dB typical
- Quiescent Current = 5.0 nA/Package typical at 5 Vdc
- Low Crosstalk Between Switches — 80 dB typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range (V_{DD}-V_{EE}) = 3 to 18 V
  Note: V_{EE} must be ≤ V_{SS}
- Transmits Frequencies Up To 65 MHz
- Linearized Transfer Characteristics, $\Delta R_{ON} < 60\ \Omega$ for V_{in} at V_{DD} to V_{EE} at 15 Vdc
- Low Noise — 12 nV $\sqrt{Cycle}$, f ≥ 1 kHz typical



L SUFFIX
CERAMIC PACKAGE
CASE 620

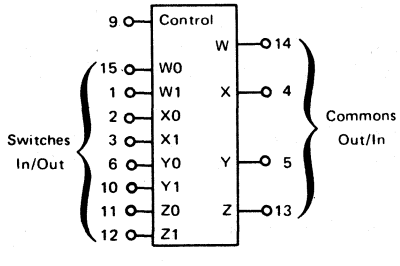
P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage V_{DD} – V_{EE}	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
Through Current	I	25	mAdc
Operating Temperature Range AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



Control	ON
0	W0 X0 Y0 Z0
1	W1 X1 Y1 Z1

V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

Note: Control Input referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be ≤ V_{SS}.

ELECTRICAL CHARACTERISTICS ($V_{EE} = V_{SS}$)

Characteristic	Symbol	V_{DD}	T_{low}*		25°C			T_{high}*		Unit
		Vdc	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage (Control) "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Input Current (Control) (AL Device)	I_{in}	15	–	±0.1	–	± 0.00001	±0.1	–	±1.0	µAdc
Input Current (Control) (CL/CP Device)	I_{in}	15	–	±0.3	–	± 0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}									pF
Control, Inhibit		–	–	–	–	5.0	7.5	–	–	
Switch Inputs (Inhibit = 1)		–	–	–	–	10	21.0	–	–	
Output Capacitance	C_{out}	10	–	–	–	17	–	–	–	pf
Feedthrough Capacitance	$C_{in\text{-}out}$	10	–	–	–	0.10	–	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package)	I_T	5.0	I_T = (0.07 µA/kHz) f + I_Q							µAdc
		10	I_T = (0.20 µA/kHz) f + I_Q							
		15	I_T = (0.36 µA/kHz) f + I_Q							
On Resistance (AL Device)	R_{ON}	5.0	–	800	–	250	1050	–	1300	Ω
		10	–	400	–	120	500	–	550	
		15	–	220	–	80	280	–	320	
On Resistance (CL/CP Device)	R_{ON}	5.0	–	880	–	250	1050	–	1200	Ω
		10	–	450	–	120	500	–	520	
		15	–	250	–	80	280	–	300	
Δ ON resistance Between Any Two Channels	ΔR_{ON}	5.0	–	–	–	25	–	–	–	Ω
		10	–	–	–	10	–	–	–	
		15	–	–	–	5.0	–	—	–	
OFF Channel Leakage Current (AL Device)	–									nAdc
Any Channel		15	–	±100	–	±0.01	±100	–	±1000	
All Channels OFF:		15	–	±100	–	±0.02	±100	–	±1000	
OFF Channel Leakage Current (CL/CP Device)	–									nAdc
Any Channel		15	–	±300	–	±0.01	±300	–	±1000	
All Channels OFF:		15	–	±300	–	±0.02	±300	–	±1000	

* T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
Noise immunity is defined as the control input voltage coincident with the specified change, ΔV_{out}, at an output in the OFF State.

** The formulae given are for the typical characteristics only at 25°C.

† Total Supply Current, I_T, is the current drawn at device terminals V_{DD} and V_{SS} for total current through the device. The channel component $(V_{in}\text{-}V_{out})/R_{ON}$, should not be included.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}-V_{SS} Vdc	Min	Typ	Max	Unit
Propagation Delay Times Switch Input to Switch Output (R_L = 10kΩ)	t_{PLH},t_{PHL}					ns
t_{PLH},t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns		5.0	–	35	90	
t_{PLH},t_{PHL} = (0.08 ns/pF) C_L + 11 ns		10	–	15	40	
t_{PLH},t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns		15	–	12	30	
Inhibit to Output (R_L = 10 kΩ): Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level	t_{PHZ},t_{PLZ} t_{PZH},t_{PZL}					ns
		5.0	–	360	900	
		10	–	160	375	
		15	–	120	300	
Control Input to Output (R_L = 10 kΩ)	t_{PLH},t_{PHL}					ns
		5.0	–	350	875	
		10	–	140	350	
		15	–	100	250	
Sine Wave Distortion (R_L = 1 kΩ, f = 1 kHz)	–	10	–	0.04	–	%
Bandwidth (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD} – V_{EE}) p-p, $20 \log_{10} \frac{V_{out}}{V_{in}}$ = –3 dB)	BW	10	–	55	–	MHz
Feedthrough Attenuation, Input to Output (R_L = 1 kΩ, V_{in} = ½ (V_{DD}-V_{EE}) p-p, $20 \log_{10} \frac{V_{out}}{V_{in}}$ = –50 dB)	–	10	–	3.0	–	MHz
Channel Separation (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD} – V_{EE}) p-p, $20 \log_{10} \frac{V_{out(B)}}{V_{in(A)}}$ = –50 dB)	–	10	–	3.0	–	MHz
Feedthrough Control, Input to Output (R1 = 1 kΩ, R_L = 10 kΩ, Control/Inhibit t_r = t_f = 20 ns	–	10	–	30	–	mV
Maximum Control Frequency (R_L = 1 kΩ, V_{out} = 1/2 V_{in})	–	10	–	10	–	MHz

*The formulas given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC

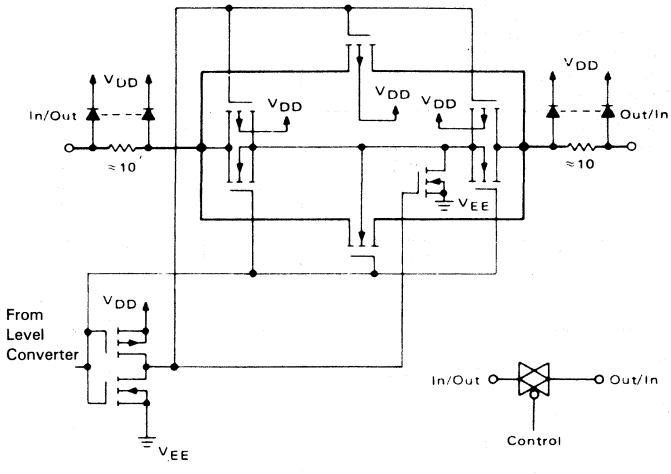
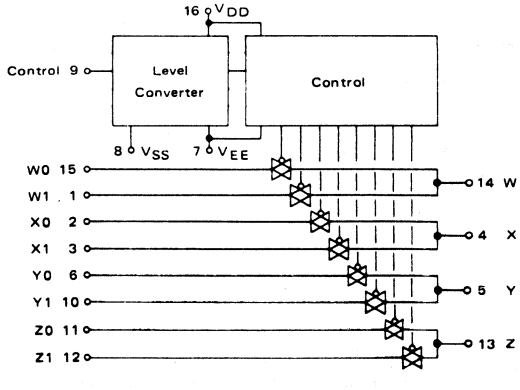


FIGURE 2 – MC14551B FUNCTIONAL DIAGRAM



TEST CIRCUITS

FIGURE 3 – INPUT VOLTAGE

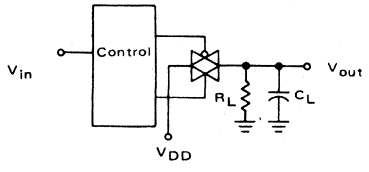


FIGURE 4 – PROPAGATION DELAY TIMES, CONTROL AND INHIBIT TO OUTPUT

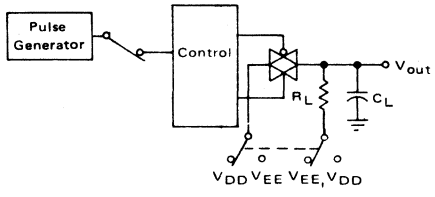


FIGURE 5 – BANDWIDTH AND FEEDTHROUGH ATTENUATION

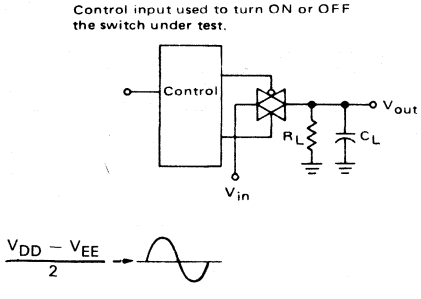


FIGURE 6 – CROSSTALK BETWEEN ANY TWO SWITCHES

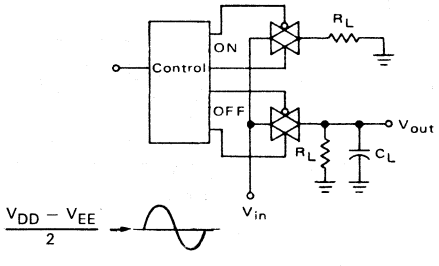


FIGURE 7 – FEEDTHROUGH, CONTROL TO SIGNAL OUTPUT

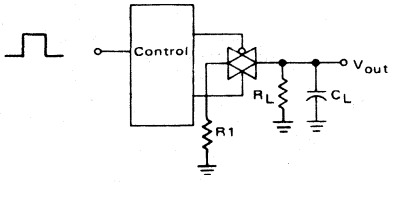


FIGURE 8 – MAXIMUM CONTROL FREQUENCY

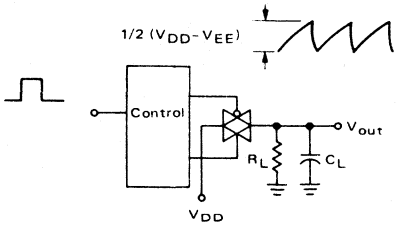
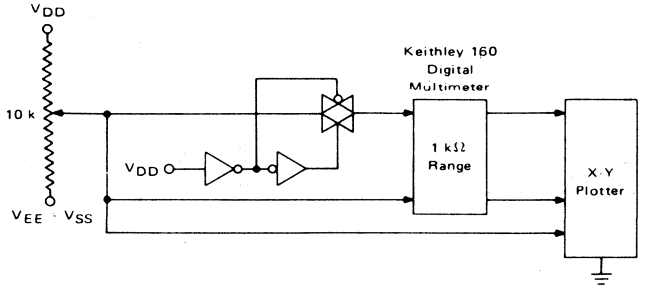


FIGURE 9 – CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



3

TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 10 – V_{DD} @ 7.5 V, V_{EE} @ –7.5V

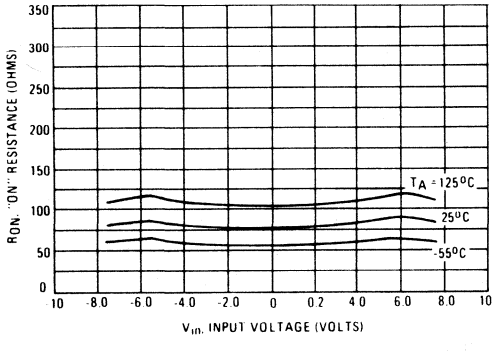


FIGURE 11 – V_{DD} @ 5.0V, V_{EE} @ –5.0 V

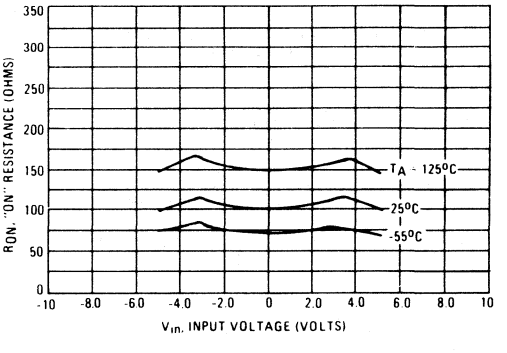


FIGURE 12 – V_{DD} @ 2.5 V, V_{EE} @ –2.5 V

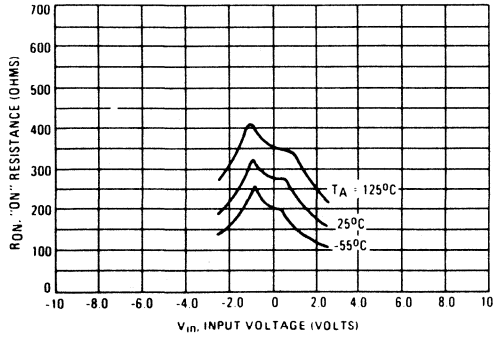
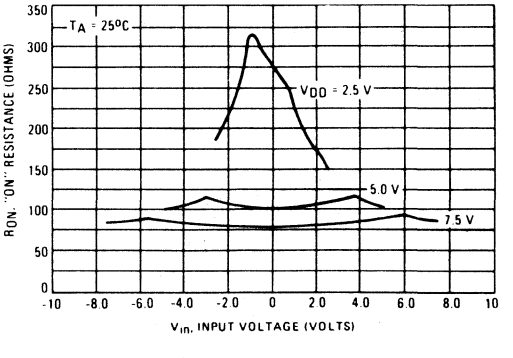


FIGURE 13 – COMPARISON at 25°C, V_{DD} @ $-V_{EE}$



MOTOROLA

MC14553B

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

THREE-DIGIT BCD COUNTER

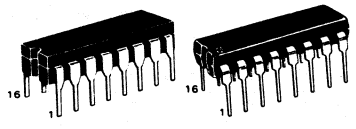
THREE-DIGIT BCD COUNTER

The MC14553B three-digit BCD counter consists of three negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on-chip oscillator provides the low-frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

- TTL Outputs
- On-Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

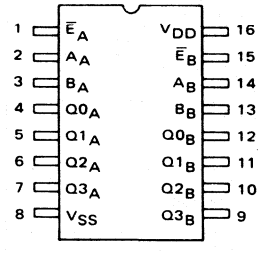
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
DC Current per Pin, All Outputs	I	20	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN ASSIGNMENT



TRUTH TABLE

INPUTS				
MASTER RESET	CLOCK	DISABLE	LE	OUTPUTS
0	⌐¬	0	0	No Change
0	¬⌐	0	0	Advance
0	X	1	X	No Change
0	1	⌐¬	0	Advance
0	1	¬⌐	0	No Change
0	0	X	X	No Change
0	X	X	⌐	Latched
0	X	X	1	Latched
1	X	X	0	Q0 = Q1 = Q2 = Q3 = 0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 4.6 Vdc) Source		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink-Pin 3	I_{OL}	5.0	0.5	–	0.4	0.88	–	0.28	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.9	2.25	–	0.65	–	
(V_{OL} = 1.5 Vdc)		15	1.80	–	1.5	8.8	–	1.20	–	
(V_{OL} = 0.4 Vdc) Sink-Other Outputs	I_{OL}	5.0	3.0	–	2.5	4.0	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	6.0	–	5.0	8.0	–	3.5	–	
(V_{OL} = 1.5 Vdc)		15	18	–	15	20	–	10	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 4.6 Vdc) Source		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink-Pin 3	I_{OL}	5.0	0.23	–	0.2	0.88	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	0.60	–	0.5	2.25	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	1.80	–	1.5	8.8	–	1.20	–	
(V_{OL} = 0.4 Vdc) Sink-Other Outputs	I_{OL}	5.0	2.4	–	2.0	4.0	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	3.8	–	3.0	8.0	–	2.5	–	
(V_{OL} = 1.5 Vdc)		15	10	–	8.4	20	–	7.0	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.35 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.85 µA/kHz) f + I_{DD}							
		15	I_T = (1.50 µA/kHz) f + I_{DD}							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	3a	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns			5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns			10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns			15	–	40	80	
Output Fall Time	3a	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns			5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns			10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns			15	–	40	80	
Clock to BCD Out	3a	t_{PLH}, t_{PHL}	5.0	–	900	1800	ns
			10	–	500	1000	
			15	–	300	600	
Clock to Overflow	3a	t_{PHL}	5.0	–	600	1200	ns
			10	–	400	800	
			15	–	200	400	
Reset to BCD Out	3b	t_{PHL}	5.0	–	900	1800	ns
			10	–	500	1000	
			15	–	300	600	
Clock to Latch Enable Setup Time Latch Enable to Master Reset Setup Time	3b	t_{su}	5.0	600	300	–	ns
			10	400	200	–	
			15	200	100	–	
Clock Pulse Width	3a	$t_{WH(cl)}$	5.0	550	275	–	ns
			10	200	100	–	
			15	150	75	–	
Reset Pulse Width	3b	$t_{WH(R)}$	5.0	1200	600	–	ns
			10	600	300	–	
			15	450	225	–	
Input Clock Frequency	3a	f_{cl}	5.0	–	1.5	0.9	MHz
			10	–	5.0	2.5	
			15	–	7.0	3.5	
Input Clock Rise Time	3b	t_{TLH}	5.0	No Limit			ns
			10				
			15				
Scan Oscillator Frequency	2	f_{osc}	5.0	–	1.5/C	–	Hz
			10	–	4.2/C	–	
(C1 measured in μF)			15	–	7.0/C	–	

* The formulae given are for the typical characteristics only.

FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING

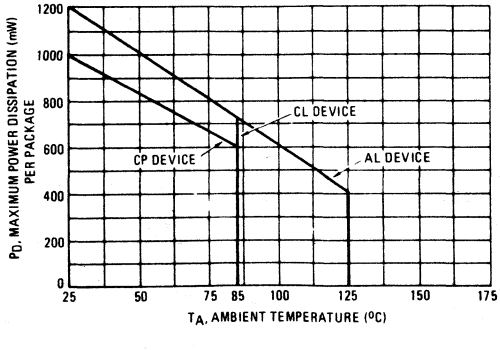


FIGURE 2 – 3-DIGIT COUNTER TIMING DIAGRAM (Reference Figure 4)

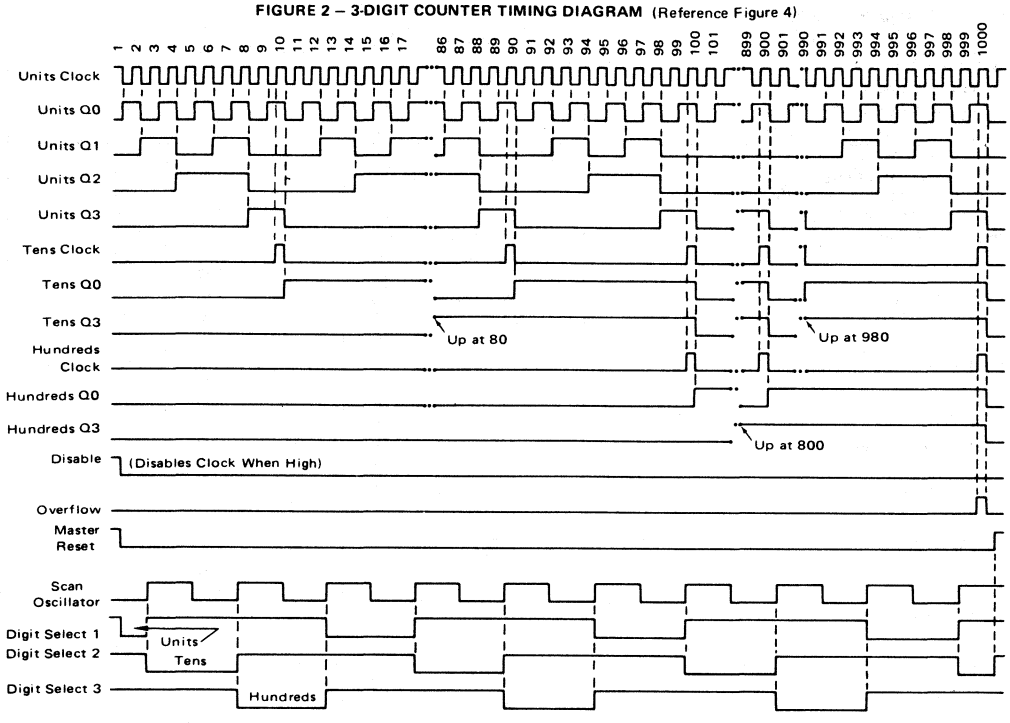
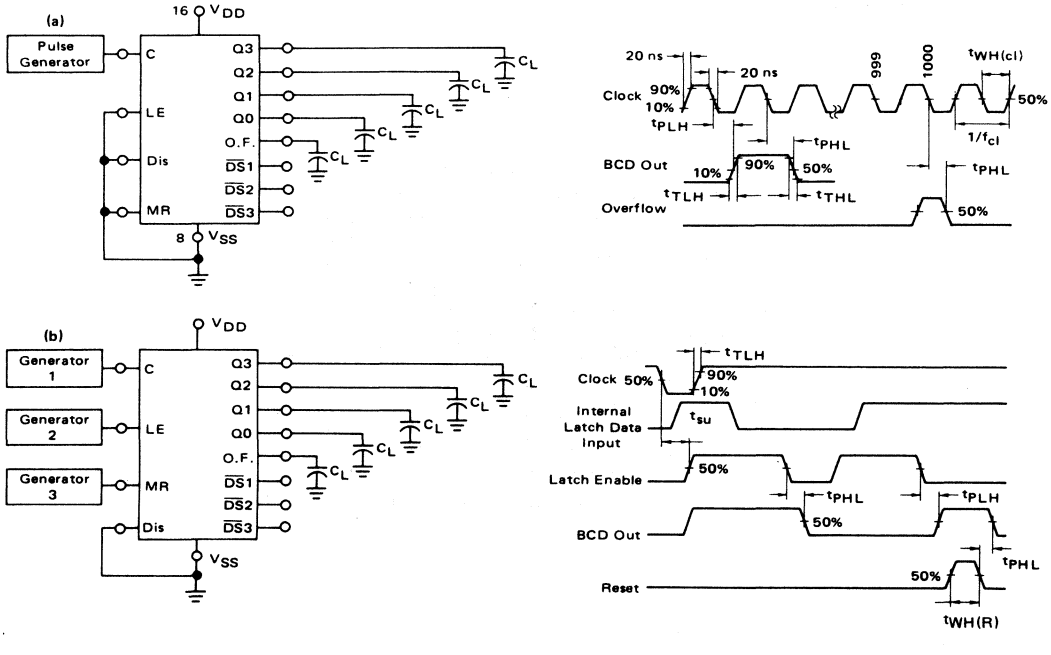


FIGURE 3 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



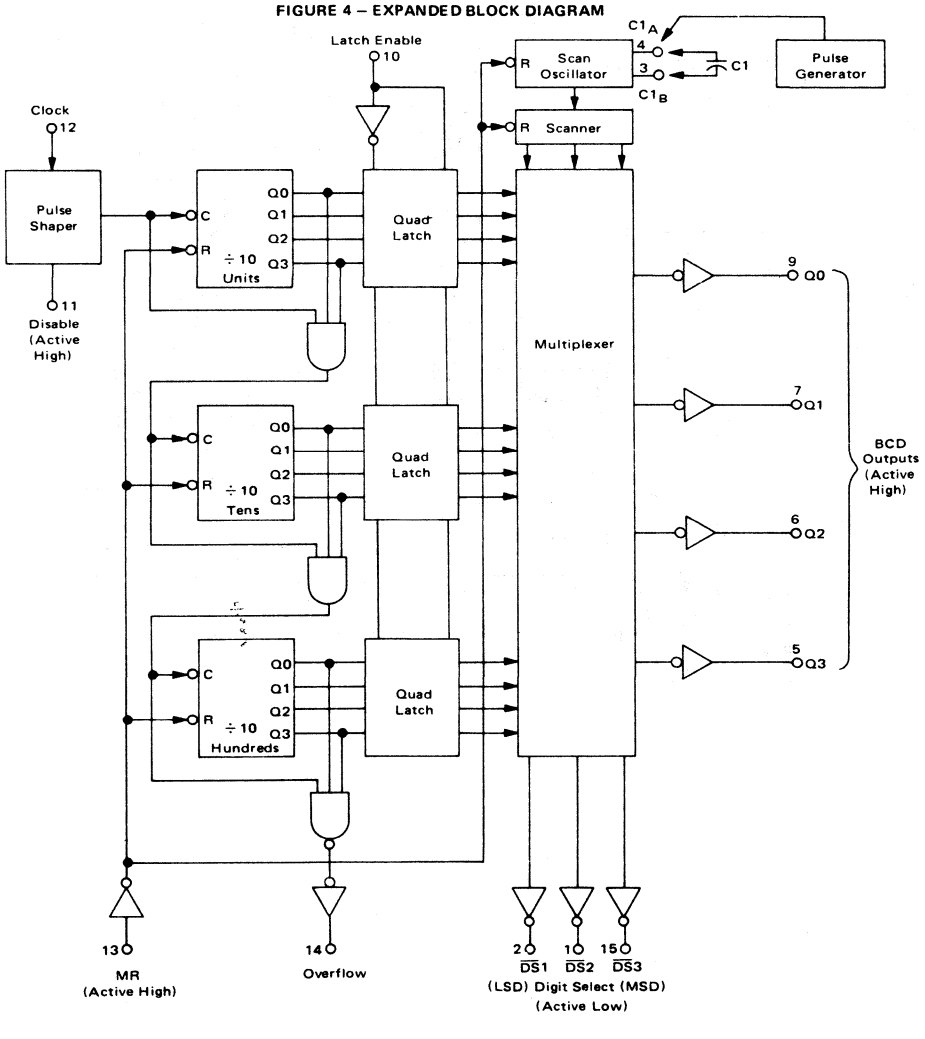
OPERATING CHARACTERISTICS

The MC14553B three-digit counter, shown in Figure 4, consists of three negative edge-triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible.

An on-chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4, or it can be overridden and driven with an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is high the digit scanner is set to digit one; but all three digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch input is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.

FIGURE 4 – EXPANDED BLOCK DIAGRAM



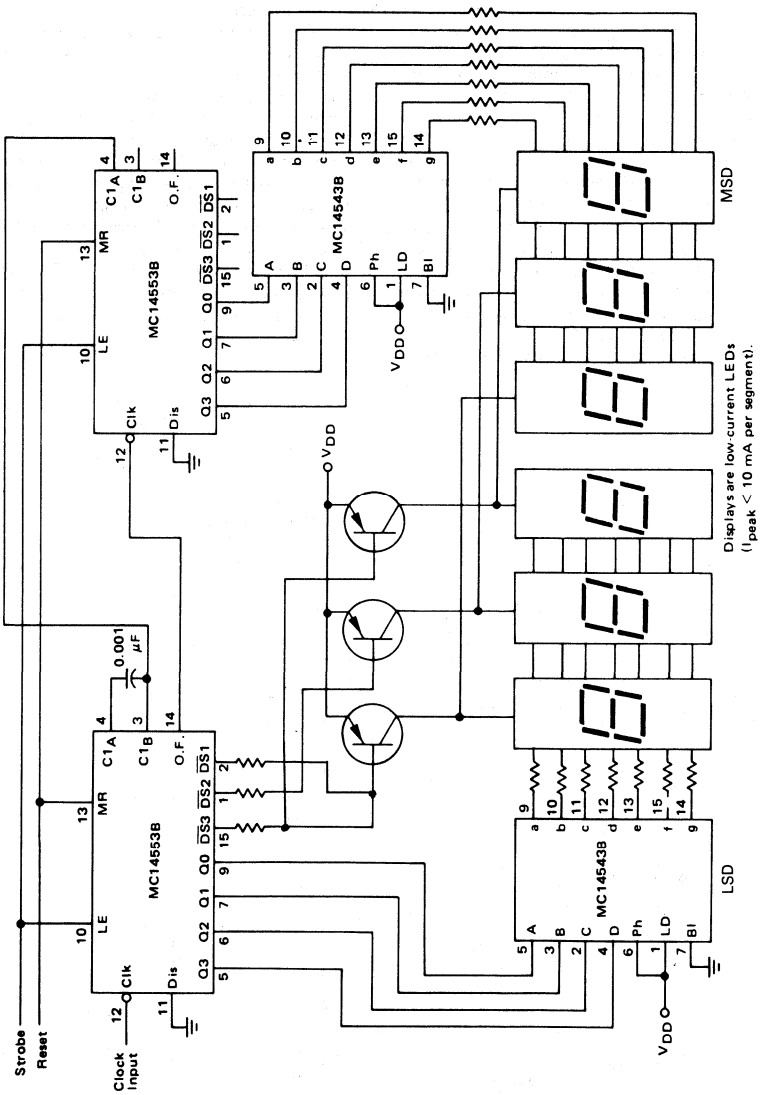


FIGURE 5 – SIX-DIGIT DISPLAY

MOTOROLA

MC14554B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

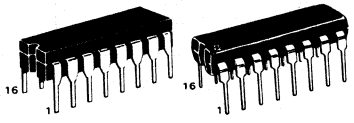
2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER

2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER

The MC14554B 2 x 2-bit parallel binary multiplier is constructed with complementary MOS (CMOS) enhancement mode devices. The multiplier can perform the multiplication of two binary numbers and simultaneously add two other binary numbers to the product. The MC14554B has two multiplicand inputs (X0 and X1), two multiplier inputs (Y0 and Y1), five cascading or adding inputs (K0, K1, M0, M1, and M2), and five sum and carry outputs (S0, S1, S2, C1 [S3], and C0). The basic multiplier can be expanded into a straightforward m-bit by n-bit parallel multiplier without additional logic elements.

Application areas include arithmetic processing (multiplying/adding, obtaining square roots, polynomial evaluation, obtaining reciprocals, and dividing), Fast Fourier Transform processing, digital filtering, communications (convoluation and correlation), and process and machine controls.

- Diode Protection on All Inputs
- All Outputs Buffered
- Quiescent Current = 5.0 nA typical @ 5 Vdc
- Straight-forward m-Bit By n-Bit Expansion
- No Additional Logic Elements Needed for Expansion
- Multiplies and Adds Simultaneously
- Positive Logic Design
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

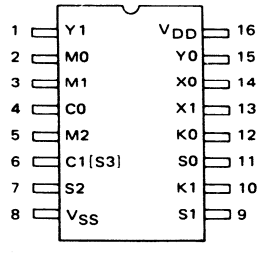
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN ASSIGNMENT



EQUATIONS

$S = (X \times Y) + K + M$

Where:
x Means Arithmetic Times.
+ Means Arithmetic Plus.
S = S3 S2 S1 S0, X = X1X0, Y = Y1Y0,
K = K1 K0, M = M1 M0 (Binary Numbers).

Example:
Given: X = 2(10), Y = 3(11)
K = 1(01), M = 2(10)

Then: S = (2 x 3) + 1 + 2 = 9
S = (10 x 11) + 01 + 10 = 1001

Note: C0 connected to M2 for this size multiplier.
See general expansion diagram for other size multipliers.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.0\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (2.0\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (3.0\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

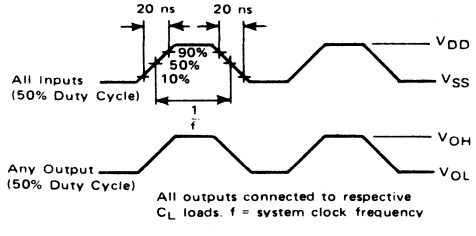
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
K0 to C0						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 185 ns		5.0	–	270	675	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 82 ns		10	–	115	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	–	85	215	
M0 to S2						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 595 ns		5.0	–	680	1700	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 247 ns		10	–	280	750	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns		15	–	210	570	

* The formulae given are for the typical characteristics only.

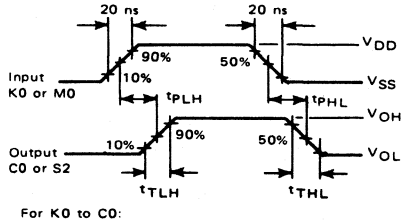
3

FIGURE 1 – DYNAMIC POWER DISSIPATION WAVEFORMS



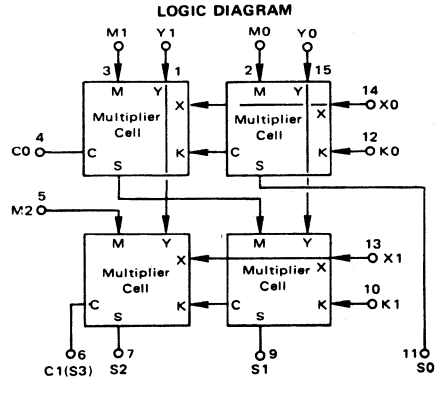
All outputs connected to respective C_L loads. f = system clock frequency

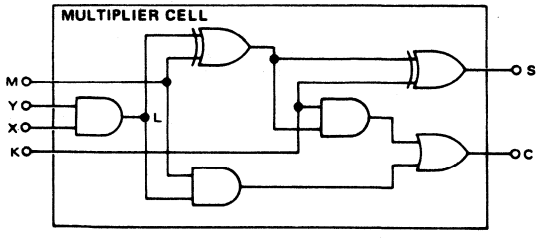
FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



For K0 to C0:
Inputs X0, X1, Y0, Y1, K1, and M2 low, and inputs M0 and M1 high.
For M0 to S2:
Inputs X1, Y1, and K0 low, and inputs X0, Y0, K1, M1, and M2 high.

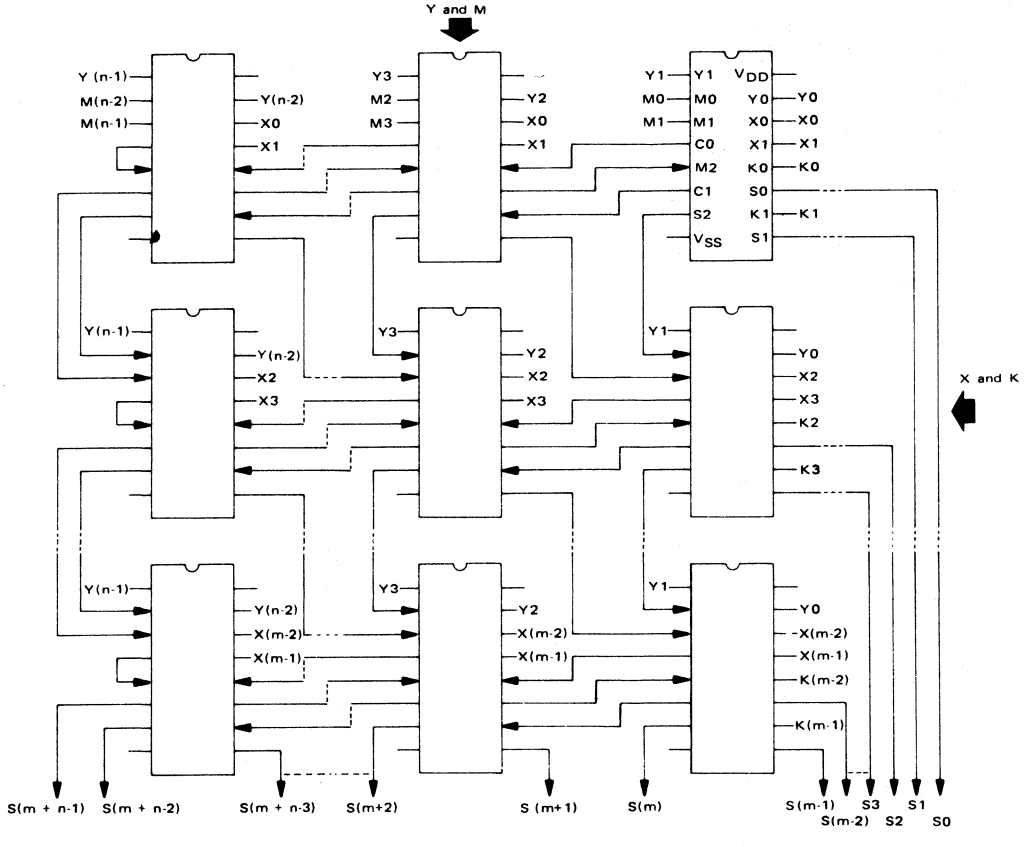
LOGIC DIAGRAM





EXPANSION DIAGRAM

m-Bit by n-Bit Parallel Binary Multiplier (Top View)



S = (X x Y) + K + M Where: x means Arithmetic Times.
+ means Arithmetic Plus.

S = S(m + n-1) S(m + n-2) - - - S2 S1 S0
X = X(m-1) X (m-2) - - - X2 X1 X0, Y = Y(n-1) Y(n-2) - - - Y2 Y1 Y0
K = K(m-1) K(m-2) - - - K2 K1 K0 and M = M(n-1) M(n-2) - - - M2 M1 M0
(Binary Numbers).

Number of output binary digits = m + n
Number of packages = mxn/4 (For m or n or both odd select next highest even number.)

MOTOROLA

MC14555B
MC14556B

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the "high" state, and the MC14556B has the selected output go to the "low" state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other MC14555B or MC14556B devices.

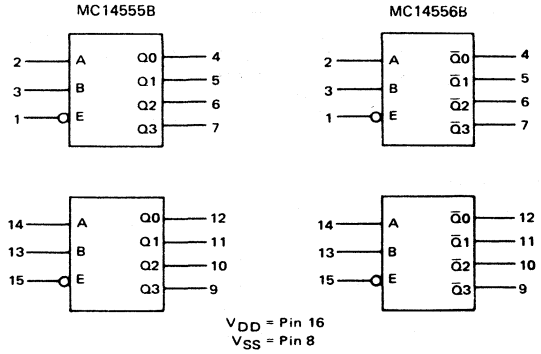
Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- Active High or Active Low Outputs
- Low Quiescent Current - 5.0 nA/package typical @ 5 Vdc
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



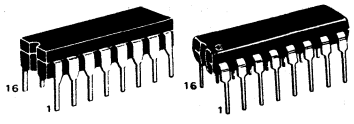
V_{DD} = Pin 16
V_{SS} = Pin 8

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

Active High Outputs — MC14555B
Active Low Outputs — MC14556B



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

TRUTH TABLE

INPUTS			OUTPUTS MC14555B				OUTPUTS MC14556B			
ENABLE	SELECT									
$\bar{E}$	B	A	Q3	Q2	Q1	Q0	$\bar{Q}3$	$\bar{Q}2$	$\bar{Q}1$	$\bar{Q}0$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.85 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.7 µA/kHz) f + I_{DD}							
		15	I_T = (2.6 µA/kHz) f + I_{DD}							

* T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

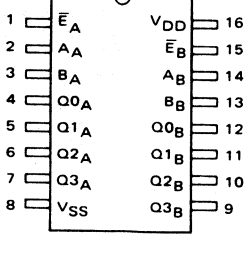
Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

† To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pf) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$.
where: I_T is in µA (Per Package) C_L in pF, V_{DD} in Vdc and f in kHz is input frequency.

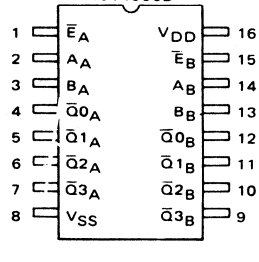
** The formulae given are for the typical characteristics only at 25°C.

PIN ASSIGNMENTS

MC14555B



MC14556B



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time – A, B to Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns		5.0	–	220	440	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 62 ns		10	–	95	190	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 45 ns		15	–	70	140	
Propagation Delay Time – E to Output	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 115 ns		5.0	–	200	400	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 52 ns		10	–	85	170	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 40 ns		15	–	65	130	

* The formulae given are for the typical characteristics only.

3

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

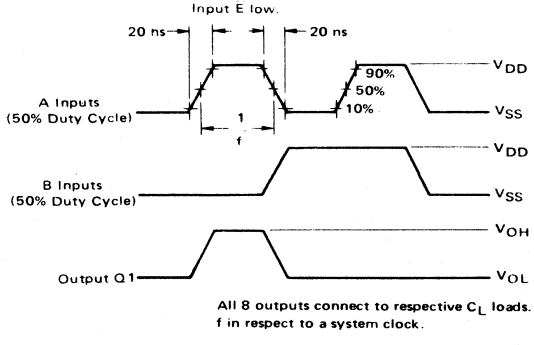
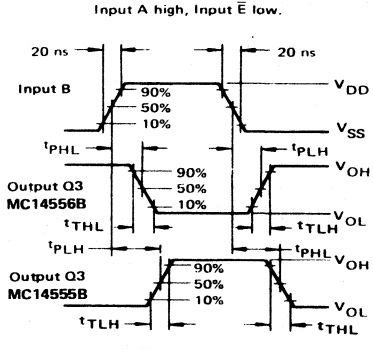
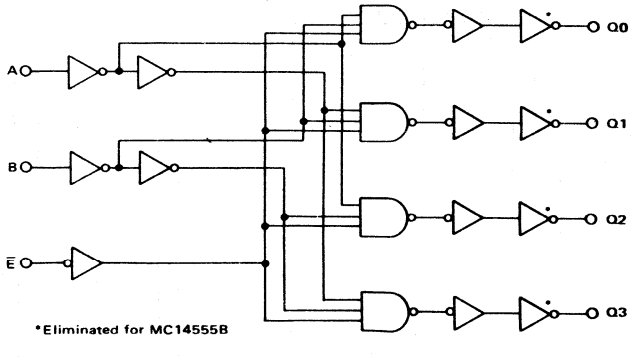


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



LOGIC DIAGRAM
(1/2 of Dual)



MOTOROLA

MC14557B

1-TO-64 BIT VARIABLE LENGTH SHIFT REGISTER

The MC14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers. characteristics can be found on the Family Data Sheet.

- Quiescent Current = 10 nA/package typical @ 5 Vdc
- 1-64 Bit Programmable Length
- Q and $\overline{Q}$ Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- 8 MHz Operation @ V_{DD} = 10 Vdc Typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LENGTH SELECT TRUTH TABLE

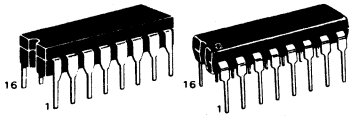
L32	L16	L8	L4	L2	L1	Register Length
0	0	0	0	0	0	1-Bit
0	0	0	0	0	1	2-Bits
0	0	0	0	1	0	3-Bits
0	0	0	0	1	1	4-Bits
0	0	0	1	0	0	5-Bits
0	0	0	1	0	1	6-Bits
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	0	0	0	0	0	33-Bits
1	0	0	0	0	1	34-Bits
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	0	0	61-Bits
1	1	1	1	0	1	62-Bits
1	1	1	1	1	0	63-Bits
1	1	1	1	1	1	64-Bits

Note: Length equals the sum of the binary length control subscripts plus one.

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

1-TO-64 BIT
VARIABLE LENGTH
SHIFT REGISTER



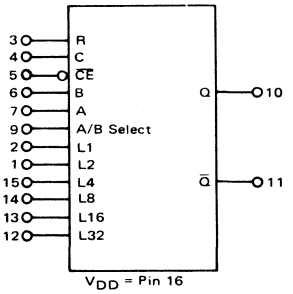
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

Inputs				Output
R	A/B	Clock	$\overline{CE}$	Q
0	0	⌐	0	B
0	1	⌐	0	A
0	0	1	⌐	B
0	1	1	⌐	A
1	X	X	X	0

Q is the output of the first selected shift register stage.
X = Don't Care.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	µAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.75\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (3.5\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (5.25\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Minimum No. of Bits Selected	Typical Setup Time $B \rightarrow \overline{CE}$ ns	Length Select Lines = 1
1	180	None
2	120	L1
3	90	L2
5	60	L4
9	30	L8
17	0	L16
33	-30	L32

SETUP TIME CHART

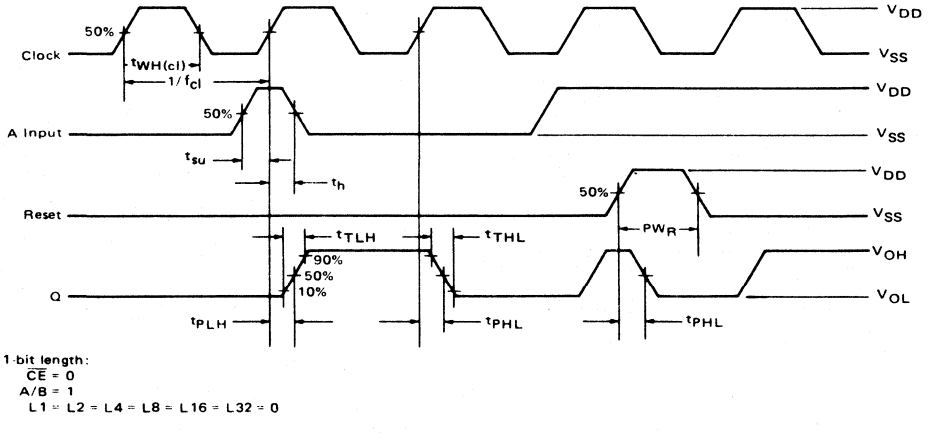
The nature of the length select logic causes the setup time to vary with the number of bits selected. The following table summarizes the typical variation at V_{DD} = 10 V, T_A = 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time						ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns	t_{TLH}	5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time						ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
(C or CE to Q or Q)	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	300	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 167 ns		10	–	200	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
(R to Q or Q)						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 390 ns		5.0	–	475	550	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 157 ns		10	–	190	380	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 115 ns		15	–	140	280	
Clock Pulse Width	$t_{WH(C)}$	5.0	440	220	–	ns
		10	136	68	–	
		15	100	50	–	
Reset Pulse Width	$t_{WH(R)}$	5.0	600	300	–	ns
		10	180	90	–	
		15	120	60	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.7	MHz
		10	–	8.0	5.0	
		15	–	10.5	6.7	
Clock Pulse Rise and Fall Time	t_{TLH},	5.0				–
	t_{THL}	10		No Limit		
		15				
Data to Clock Setup Time (A or B to C or $\overline{CE}$)	t_{su}	5.0	900	250	–	ns
L1, L2, L4, L8, L16, L32 = 0		10	360	180	–	
		15	170	135	–	
Data to Clock Hold Time (A or B to C or $\overline{CE}$)	t_h	5.0	-225	-450	–	ns
L1, L2, L4, L8, L16, L32 = 0		10	- 90	-180	–	
		15	- 60	-135	–	
Reset Fall Time	t_{THL}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	

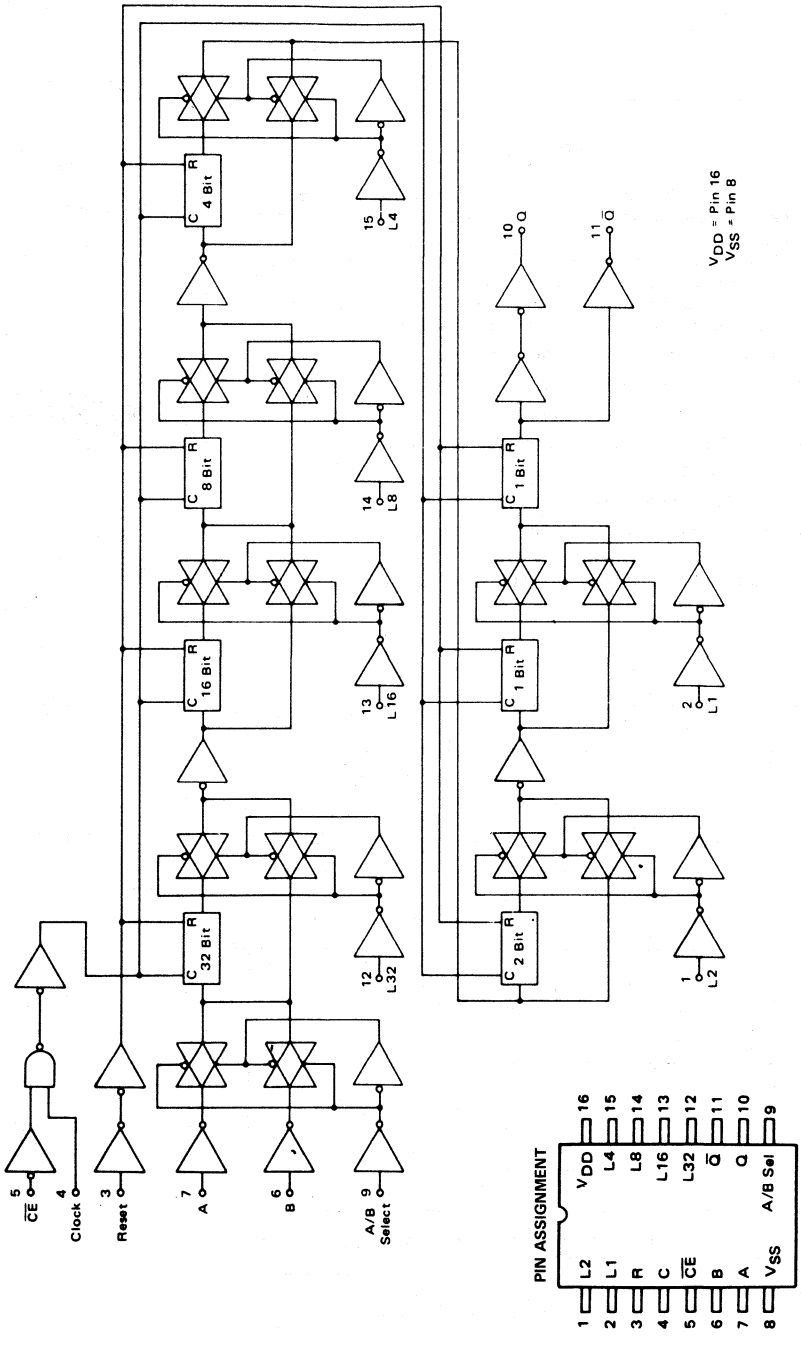
* The formulae given are for the typical characteristics only.

TIMING DIAGRAM



1-bit length:
$\overline{CE}$ = 0
A/B = 1
L1 = L2 = L4 = L8 = L16 = L32 = 0

LOGIC DIAGRAM



PIN ASSIGNMENT

MOTOROLA

MC14560B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

NBCD ADDER

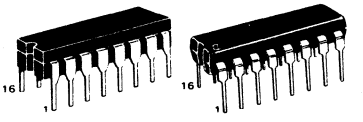
NBCD ADDER

The MC14560B adds two 4-bit numbers in NBCD (natural binary coded decimal) format, resulting in sum and carry outputs in NBCD code.

This device can also subtract when one set of inputs is complemented with a 9's Complementer (MC14561B).

All inputs and outputs are active high. The carry input for the least significant digit is connected to V_{SS} for no carry in.

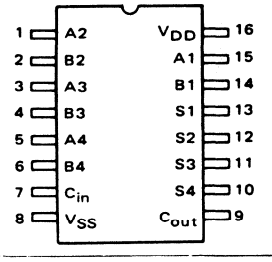
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Single Supply Operation – Positive or Negative
- Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE*

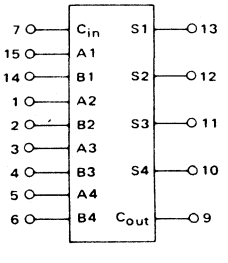
INPUT									OUTPUT				
A4	A3	A2	A1	B4	B3	B2	B1	C_{in}	C_{out}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	1	1	1	1	0	0	1

*Partial truth table to show logic operation for representative input values.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	**0.005**	5.0	–	150	μAdc
(Per Package)		10	–	10	–	**0.010**	10	–	300	
		15		20	–	**0.015**	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	**0.005**	20	–	150	μAdc
(Per Package)		10	–	40	–	**0.010**	40	–	300	
		15	–	80	–	**0.015**	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.68 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.35 μA/kHz) f + I_{DD}							
		15	I_T = (5.03 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$$

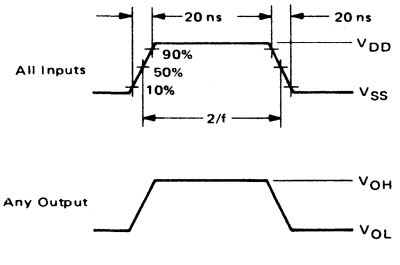
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
A or B to S	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns		5.0	–	750	2100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 297 ns		10	–	330	900	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 195 ns		15	–	220	675	
A or B to C_{out}						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	–	650	1800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	450	
C_{in} to C_{out}						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	–	550	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 187 ns		10	–	220	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	–	160	450	
Turn-Off Delay Time	t_{PLH}					ns
C_{in} to S						
t_{PLH} = (1.7 ns/pF) C_L + 715 ns		5.0	–	800	2250	
t_{PLH} = (0.66 ns/pF) C_L + 197 ns		10	–	350	975	
t_{PLH} = (0.5 ns/pF) C_L + 215 ns		15	–	240	750	
Turn-On Delay Time	t_{PHL}					ns
C_{in} to S						
t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	–	650	1800	
t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	600	
t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	450	

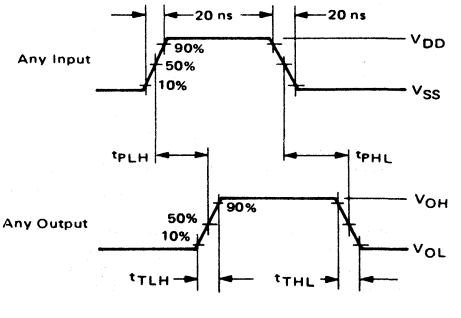
* The formulae given are for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION WAVEFORMS



Duty Cycle = 50%
All outputs connected to respective C_L loads
f = System clock frequency

FIGURE 2 – SWITCHING TIME WAVEFORMS



FUNCTIONAL EQUIVALENT LOGIC DIAGRAM

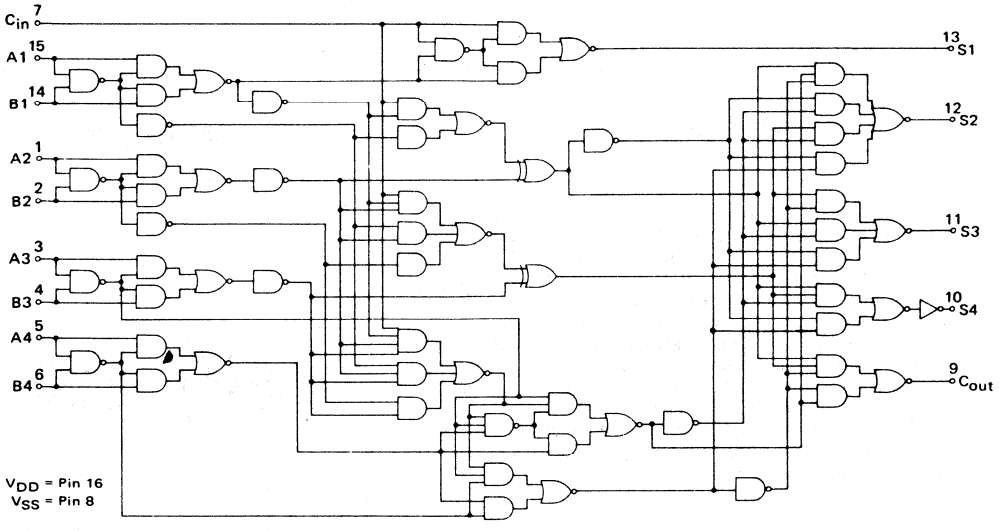
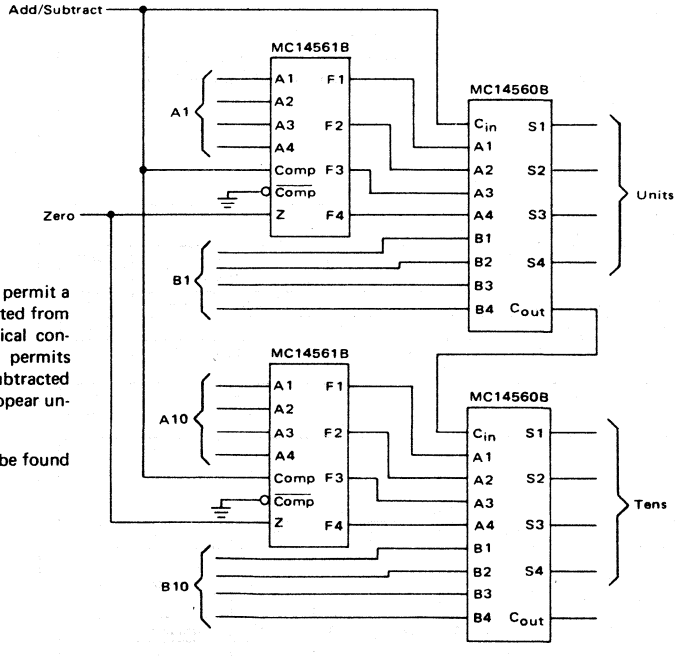


FIGURE 3 – PARALLEL ADD/SUBTRACT CIRCUIT



One MC14560B and MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in this typical configuration. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

Additional applications data may be found in Application Note AN-738.

TRUTH TABLE

Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	B

X = Don't Care

MOTOROLA

MC14561B

9's COMPLEMENTER

The MC14561B 9's complementer is a companion to the MC14560B NBCD adder to allow BCD subtraction. A BCD number (8-4-2-1 code) is applied to the inputs ($A1 = 2^0$, $A2 = 2^1$, $A3 = 2^2$, $A4 = 2^3$). If the complement control (Comp) is low, the BCD number appears at the outputs unmodified. The complement disable ($\overline{Comp}$) allows the complement control to be gated, or an inverted control signal to be used. If the complement input is high and the disable input low, the 9's complement of the number is displayed at the outputs. The zero control (Z), when high, forces the outputs low regardless of the state of the other inputs.

When the MC14561B is used to perform BCD subtraction in conjunction with the MC14560B NBCD adder, the complement control becomes an add/subtract control.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Propagation Delay = 160 ns typical at V_{DD} = 10 Vdc
- All Inputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range -- AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

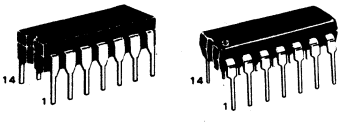
Z	Comp	$\overline{Comp}$	F1	F2	F3	F4	Mode
0	0	0	A1	A2	A3	A4	Straight-through
0	0	1					
0	1	1					
0	1	0	$\overline{A1}$	A2	$A2\overline{A3} + \overline{A2}A3$	$\overline{A2}\overline{A3}\overline{A4}$	Complement
1	X	X	0	0	0	0	Zero

X = Don't Care.

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

9's COMPLEMENTER



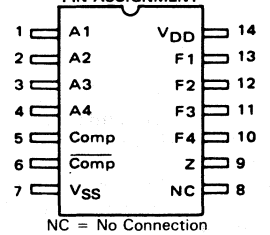
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



NC = No Connection

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	**0.005**	5.0	–	150	μAdc
		10	–	10	–	**0.010**	10	–	300	
		15	–	20	–	**0.015**	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	**0.005**	20	–	150	μAdc
		10	–	40	–	**0.010**	40	–	300	
		15	–	80	–	**0.015**	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.5 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.0 μA/kHz) f + I_{DD}							
		15	I_T = (4.5 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

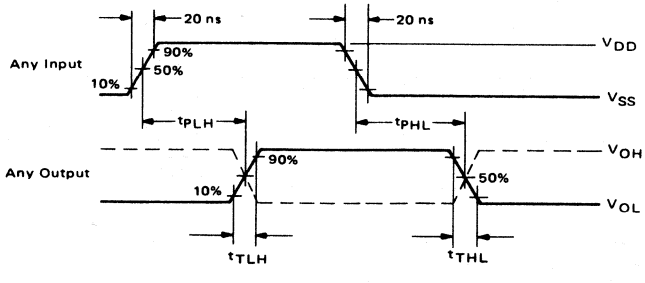
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns	t_{PHL}	5.0	–	400	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 127 ns		10	–	160	400	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 95 ns		15	–	120	300	

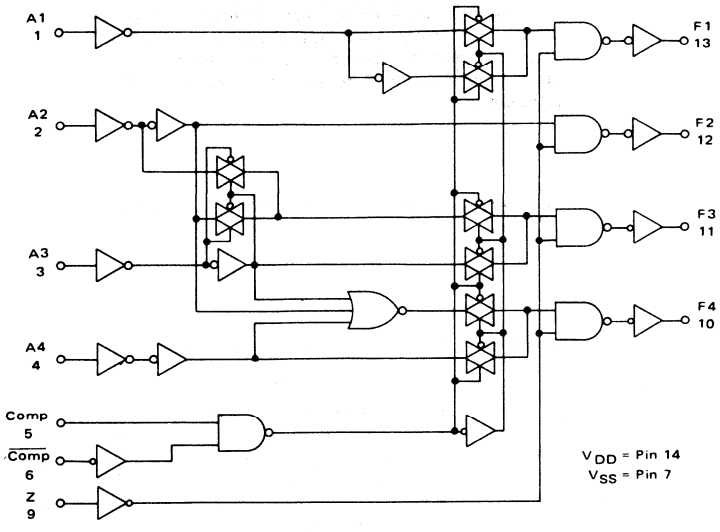
* The formulae given are for the typical characteristics only.

3

FIGURE 1 – SWITCHING TIME WAVEFORMS



LOGIC DIAGRAM



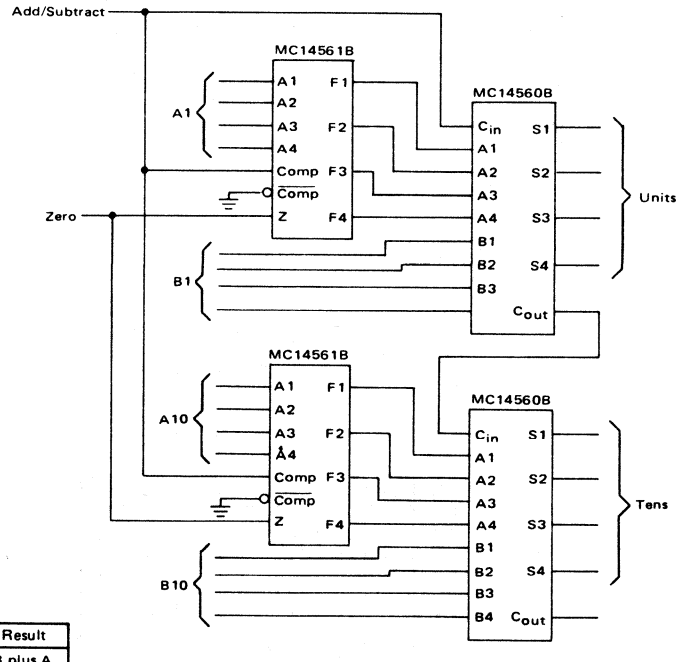
TRUTH TABLE – COMPLEMENT MODE
(Z = 0, Comp = 1, $\overline{\text{Comp}}$ = 0)

	Decimal Equivalent Input	Inputs				Decimal Equivalent Output	Outputs			
		A4	A3	A2	A1		F4	F3	F2	F1
	0	0	0	0	0	9	1	0	0	1
	1	0	0	0	1	8	1	0	0	0
	2	0	0	1	0	7	0	1	1	1
	3	0	0	1	1	6	0	1	1	0
	4	0	1	0	0	5	0	1	0	1
	5	0	1	0	1	4	0	1	0	0
	6	0	1	1	0	3	0	0	1	1
	7	0	1	1	1	2	0	0	1	0
	8	1	0	0	0	1	0	0	0	1
	9	1	0	0	1	0	0	0	0	0
Illegal BCD Input Codes	10	1	0	1	0	7	0	1	1	1
	11	1	0	1	1	6	0	1	1	0
	12	1	1	0	0	5	0	1	0	1
	13	1	1	0	1	4	0	1	0	0
	14	1	1	1	0	3	0	0	1	1
	15	1	1	1	1	2	0	0	1	0

TYPICAL APPLICATIONS

One MC14560B and one MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in the typical configurations in Figures 2 and 3. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

FIGURE 2 – PARALLEL ADD/SUBTRACT CIRCUIT (10's COMPLEMENT)

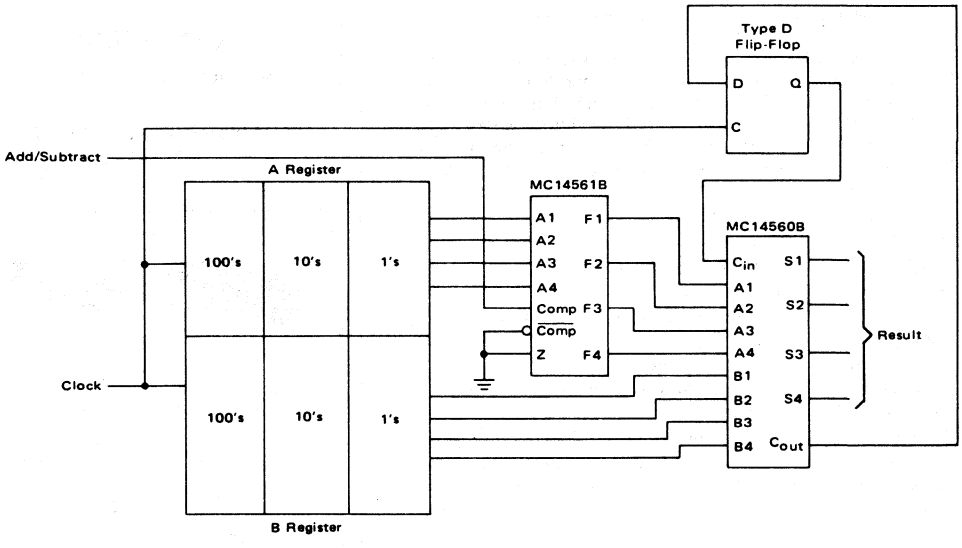


TRUTH TABLE

Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	B

X = Don't Care

FIGURE 3 – SERIAL ADD/SUBTRACT CIRCUIT



MOTOROLA

MC14562B

128-BIT STATIC SHIFT REGISTER

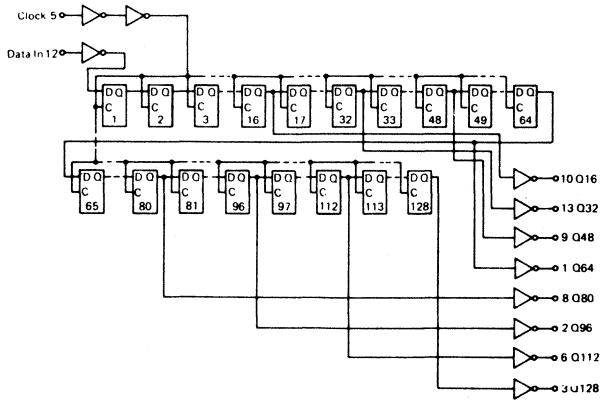
The MC14562B is a 128-bit static shift register constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data is clocked in and out of the shift register on the positive edge of the clock input. Data outputs are available every 16 bits, from 16 through bit 128. This complementary MOS shift register is primarily used where low power dissipation and/or high noise immunity is desired.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- Single Supply Operation – Positive or Negative
- Fully Static Operation
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 5.6 MHz Operation @ V_{DD} = 10 Vdc
- Cascadable to Provide Longer Shift Register Lengths – 1.5 MHz Operation @ V_{DD} = 10 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

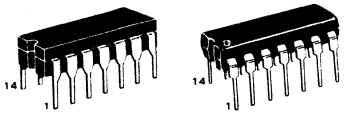
LOGIC DIAGRAM



CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

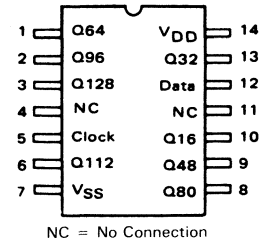
128-BIT STATIC SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

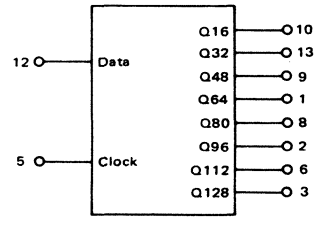
P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN ASSIGNMENT



NC = No Connection

BLOCK DIAGRAM



Pins 4 and 11 not used.

V_{DD} = Pin 14
V_{SS} = Pin 7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	μAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (1.94\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (3.81\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (5.52\ \mu A/kHz)\ f + I_{DD}$							

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

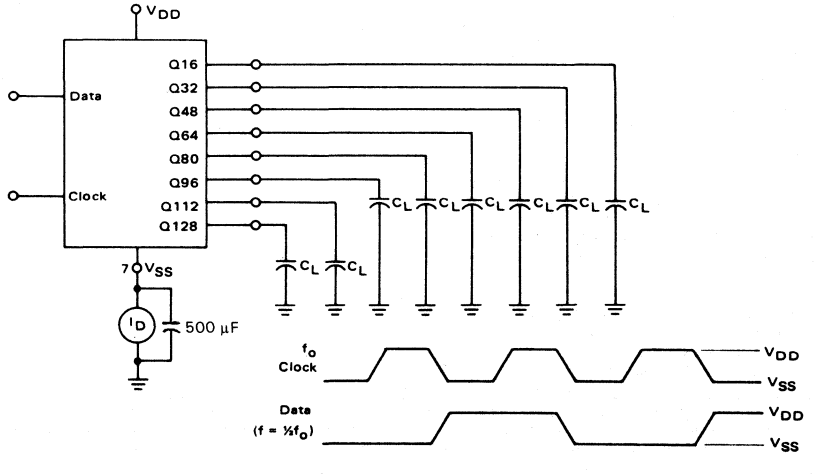
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

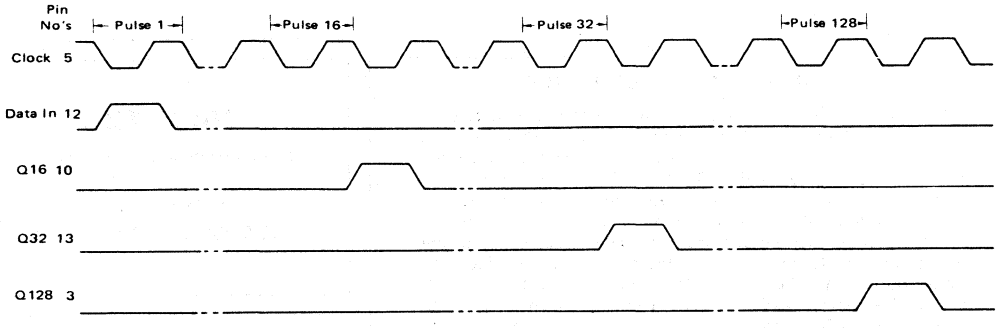
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time Clock to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 515 ns		5.0	–	600	1200	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	–	250	500	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	340	
Clock Pulse Width (50% Duty Cycle)	t_{WH}	5.0	600	300	–	ns
		10	220	110	–	
		15	150	75	–	
Clock Pulse Frequency	f_{cl}	5.0	–	1.9	1.1	MHz
		10	–	5.6	3.0	
		15	–	8.0	4.0	
Data to Clock Setup Time	$t_{su(1)}$	5.0	-20	-170	–	ns
		10	-10	-64	–	
		15	0	-60	–	
	$t_{su(0)}$	5.0	-20	-91	–	ns
		10	-10	-58	–	
		15	0	-48	–	
Data to Clock Hold Time	$t_{h(1)}$	5.0	350	263	–	ns
		10	165	109	–	
		15	155	100	–	
	$t_{h(0)}$	5.0	350	267	–	ns
		10	200	140	–	
		15	140	93	–	

* The formulae given are for the typical characteristics only.

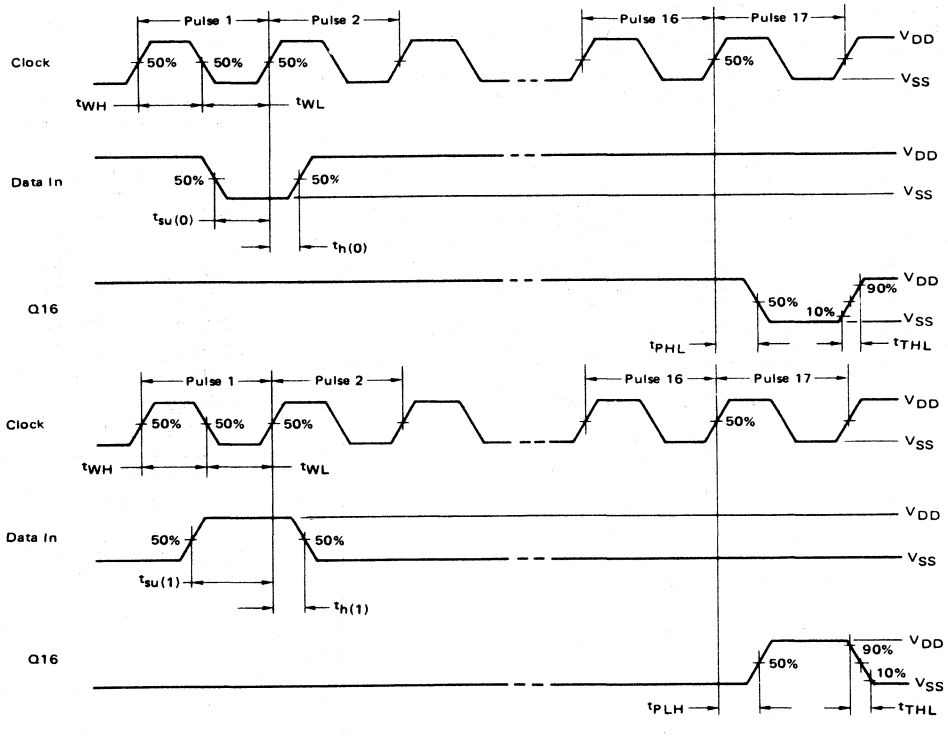
FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



TIMING DIAGRAM



AC TEST WAVEFORMS



Note: The remaining Data-Bit Outputs (Q32, Q48, Q64, Q80, Q96, Q112 and Q128) will occur at Clock Pulse 32, 48, 64, 80, 96, 112, 128 in the same relationship as Q16.

MOTOROLA

MC14566B

INDUSTRIAL TIME BASE GENERATOR

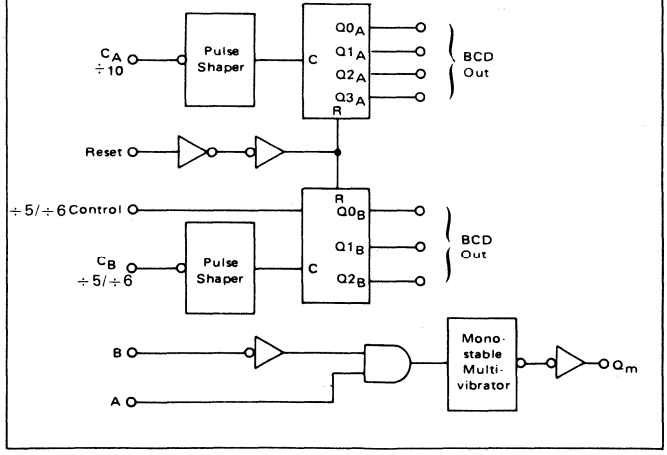
The MC14566B industrial time base generator is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of a divide-by-10 ripple counter and a divide-by-5 or divide-by-6 ripple counter to permit stable time generation from a 50 or 60 Hz line. By cascading this device as divide-by-60 counters, seconds and minutes can be counted and are available in BCD format at the circuit outputs. An internal monostable multivibrator is included whose output can be used as a reset or clock pulse providing additional frequency flexibility. Also a pin has been included to allow divide-by-5 counting for generating 1.0 Hz from European 50 Hz line. Pin 11 = V_{DD} will cause ÷5.

- Negative Edge Triggered Counters for Ease of Cascading
- Pulse Shapers on Counter Inputs Accept Slow Input Rise Times
- Monostable Multivibrator Positive or Negative Edge Triggered
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

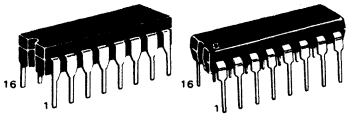
EXPANDED BLOCK DIAGRAM



CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

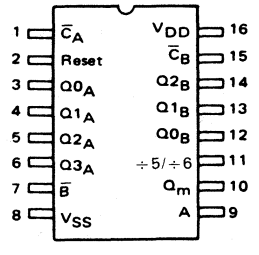
INDUSTRIAL
TIME BASE GENERATOR



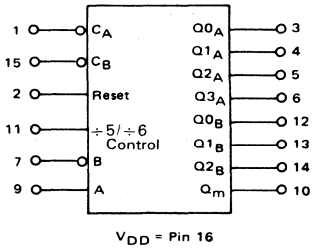
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.0 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.0 μA/kHz) f + I_{DD}							
		15	I_T = (3.0 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time, Clock to $Q3_A$	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1365 ns		5.0	–	1450	4500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 497 ns		10	–	530	1500	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 295 ns		15	–	320	1000	
Propagation Delay Time, Reset to $Q3_A$	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 845 ns		5.0	–	930	3000	
t_{PHL} = (0.66 ns/pF) C_L + 282 ns		10	–	315	1000	
t_{PHL} = (0.5 ns/pF) C_L + 185 ns		15	–	210	750	
Clock Pulse Width	$t_{WH(cl)}$					ns
		5.0	1200	400	–	
		10	400	125	–	
		15	270	90	–	
Reset Pulse Width	$t_{WH(R)}$					ns
		5.0	1200	400	–	
		10	400	125	–	
		15	270	90	–	
Clock Pulse Frequency	f_{cl}					MHz
		5.0	–	1.0	0.3	
		10	–	2.5	1.0	
		15	–	4.2	1.5	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				
		15				
Monostable Multivibrator Pulse Width	$t_{WH(Q_m)}$					ns
		5.0	1200	2800	–	
		10	400	900	–	
		15	300	600	–	

* The formulae given are for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

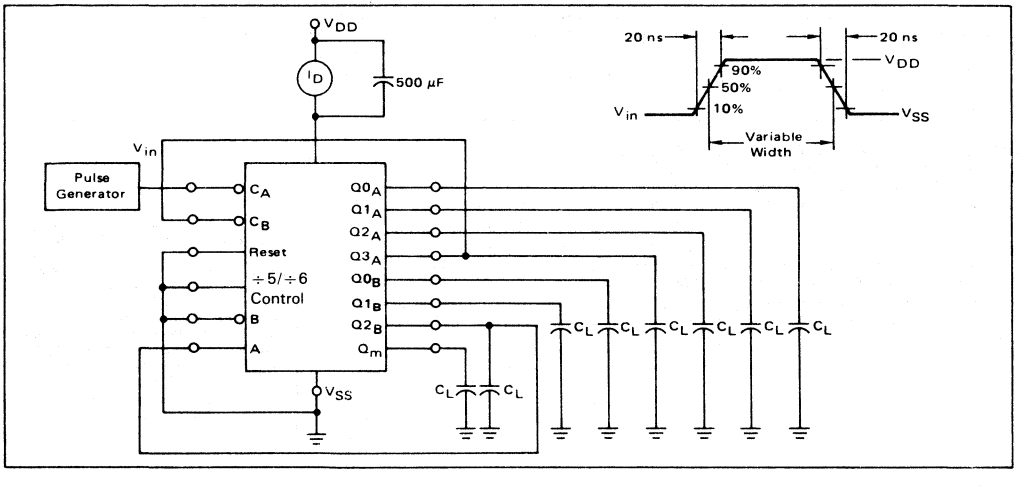
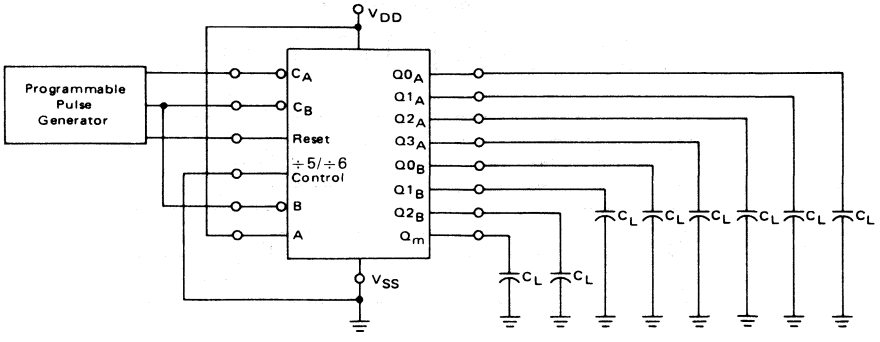
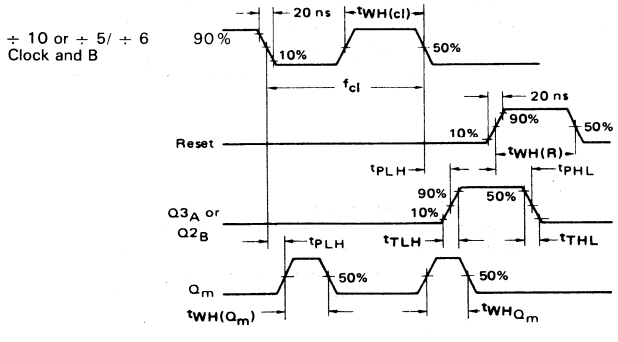


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

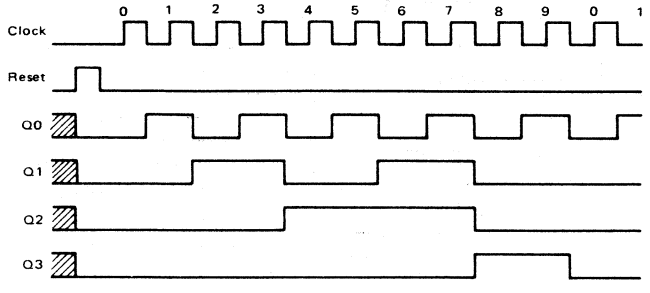


Note: Assume ÷ 10 Counter at "6" and ÷5/÷6 Counter at "2" at beginning of sequence.

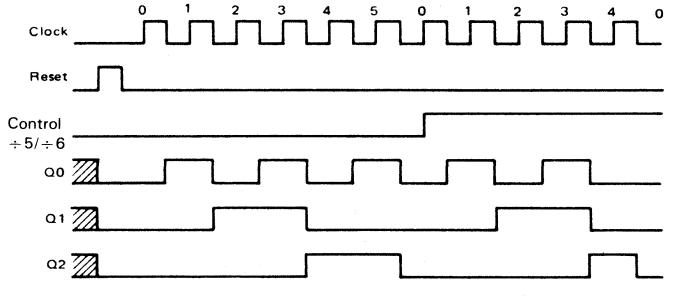


TIMING DIAGRAM

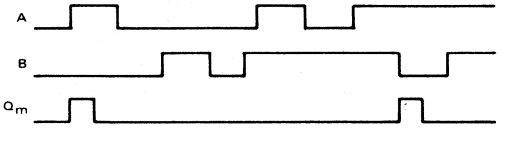
Divide-By-10 Counter



Divide-By-5/Divide-By-6

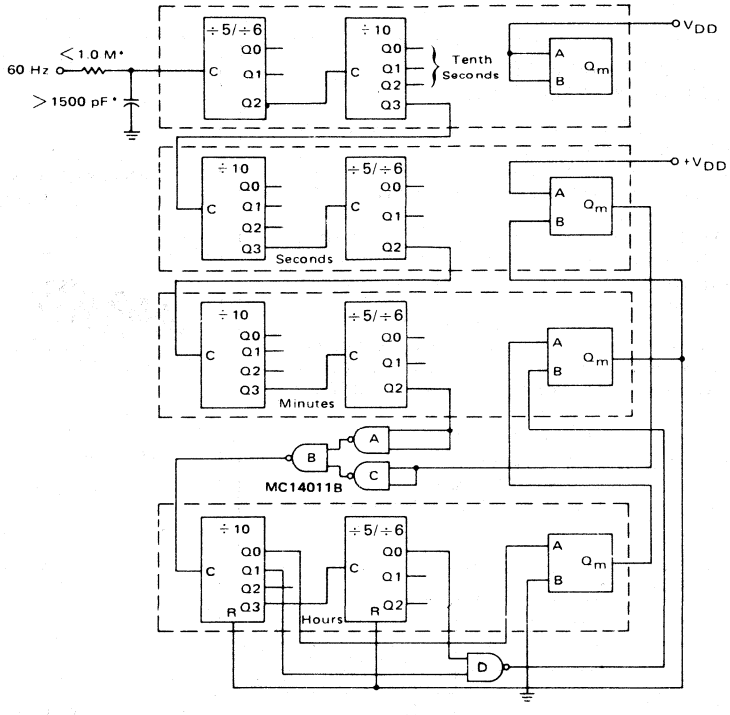


Monostable Multivibrator



▨ = Don't Care

APPLICATION – 12 HOUR CLOCK



÷5/÷6 Control not shown = V_{SS}
Reset pins not shown = V_{SS}

*Care must be taken in the indicated circuit to filter line transients which may cause "false" counting.

MOTOROLA

MC14568B

PHASE COMPARATOR AND PROGRAMMABLE COUNTERS

The MC14568B consists of a phase comparator, a divide-by-4, 16, 64 or 100 counter and a programmable divide-by-N 4-bit binary counter (all positive-edge triggered) constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a single monolithic structure.

The MC14568B has been designed for use in conjunction with a programmable divide-by-N counter for frequency synthesizers and phase-locked loop applications requiring low power dissipation and/or high noise immunity.

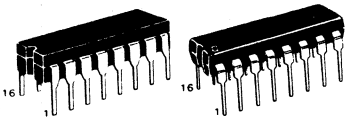
This device can be used with both counters cascaded and the output of the second counter connected to the phase comparator (CTL high), or used separate of the programmable divide-by-N counter, for example cascaded with MC14569B (CTL low), MC14522B or MC14526B.

- Quiescent Current = 5.0 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PHASE COMPARATOR AND PROGRAMMABLE COUNTERS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

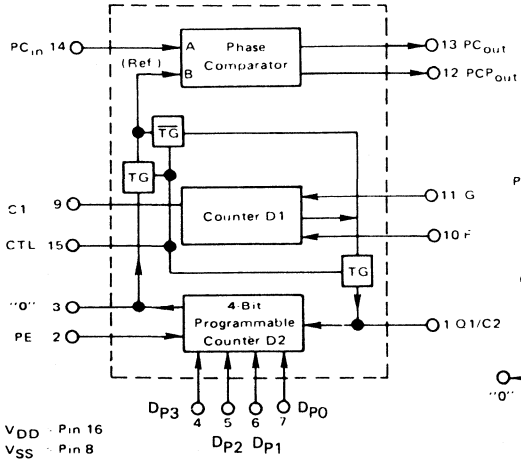
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

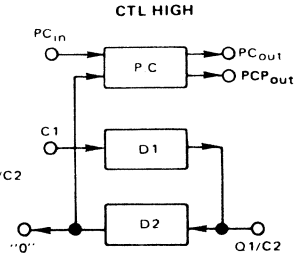
F Pin 10	G Pin 11	Division Ratio of Counter D1
0	0	4
0	1	16
1	0	64
1	1	100

The divide-by-zero state on the programmable divide-by-N 4-bit binary counter, D2, is illegal.

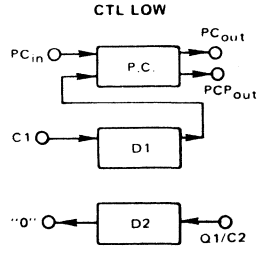
BLOCK DIAGRAM



CTL HIGH



CTL LOW



ELECTRICAL CHARACTERISTICS

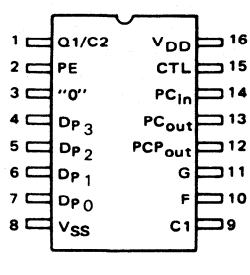
Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage #† "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	–0.8	–1.7	–	–0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	–0.16	–0.36	–	–0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	–0.4	–0.9	–	–0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	–1.2	–3.5	–	–1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10		300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.2\ \mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (0.4\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (0.9\ \mu A/kHz)\ f + I_{DD}$							
Three-State Leakage Current, Pins 1, 13 (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc
Three-State Leakage Current, Pins 1, 13 (CL/CP Devices)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	µAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

†Pin 15 is connected to V_{SS} or V_{DD} for input voltage test.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	5.0	–	180	360	ns
		10	–	90	180	
		15	–	65	130	
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Minimum Pulse Width, C1, Q1/C2, or PC_{in} Input	t_{WH}	5.0	–	125	250	ns
		10	–	60	120	
		15	–	45	90	
Maximum Clock Rise and Fall Time, C1, Q1/C2, or PC_{in} Input	t_{TLH}, t_{THL}	5.0	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
PHASE COMPARATOR						
Input Resistance	Rin	5.0 to 15	–	10^6	–	MΩ
Input Sensitivity, DC Coupled	–	5.0 to 15	See Input Voltage			
Turn-Off Delay Time, PC_{out} and PCP_{out} Outputs	t_{PHL}	5.0	–	550	1100	ns
		10	–	195	390	
		15	–	120	240	
Turn-On Delay Time, PC_{out} and PCP_{out} Outputs	t_{PHL}	5.0	–	675	1350	ns
		10	–	300	600	
		15	–	190	380	
DIVIDE-BY-4, 16, 64 OR 100 COUNTER (D1)						
Maximum Clock Pulse Frequency	f_{cl}					MHz
Division Ratio = 4, 64 or 100		5.0	3.0	6.0	–	
		10	8.0	16	–	
		15	10	22	–	
Division Ratio = 16		5.0	1.0	2.5	–	MHz
		10	3.0	6.3	–	
		15	5.0	9.7	–	
Propagation Delay Time, Q1/C2 Output	t_{PLH}, t_{PHL}					ns
Division Ratio = 4, 64 or 100		5.0	–	450	900	
		10	–	190	380	
		15	–	130	260	
Division Ratio = 16		5.0	–	720	1440	ns
		10	–	300	600	
		15	–	200	400	
PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (D2)						
Maximum Clock Pulse Frequency (Figure 3a)	f_{cl}	5.0	1.2	1.8	–	MHz
		10	3.0	8.5	–	
		15	4.0	12	–	
Turn-On Delay Time, "0" Output (Figure 3a)	t_{PLH}	5.0	–	450	900	ns
		10	–	190	380	
		15	–	130	260	
Turn-Off Delay Time, "0" Output (Figure 3a)	t_{PHL}	5.0	–	225	450	ns
		10	–	85	170	
		15	–	60	150	
Minimum Preset Enable Pulse Width	$t_{WH(PE)}$	5.0	–	75	250	ns
		10	–	40	100	
		15	–	30	75	

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g. either V_{SS} or V_{DD}).

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

FIGURE 1 – PHASE COMPARATOR

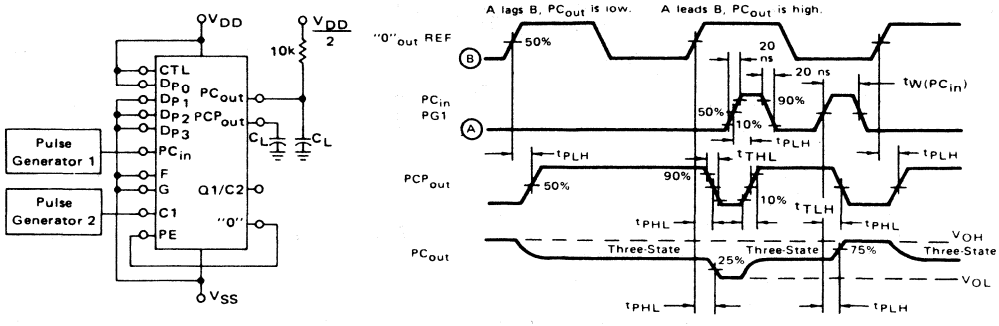


FIGURE 2 – COUNTER D1

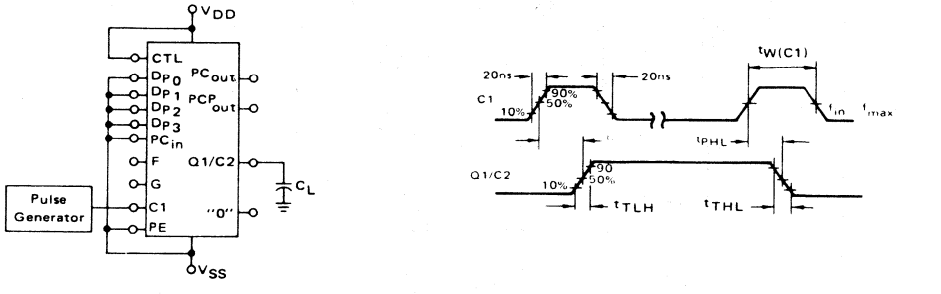
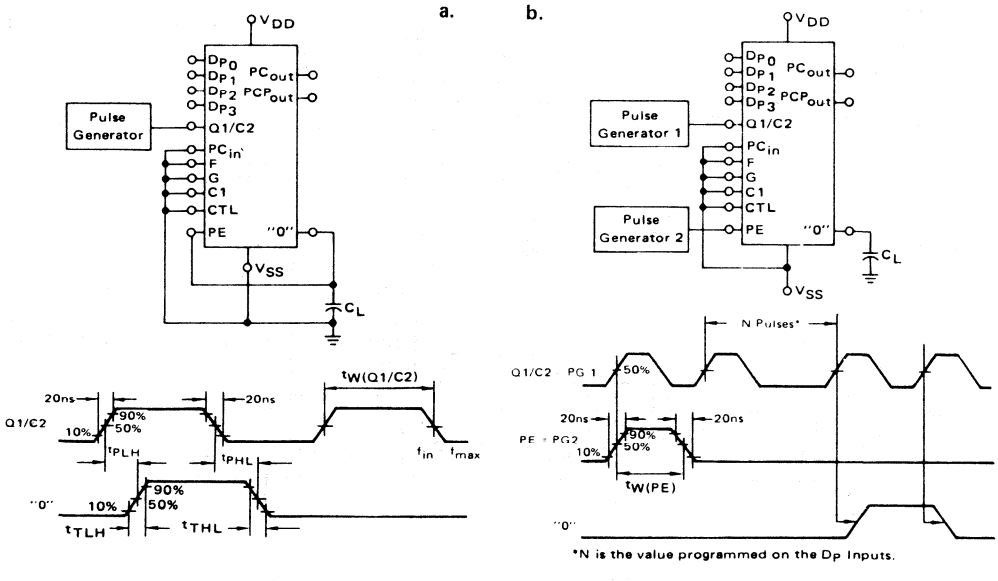
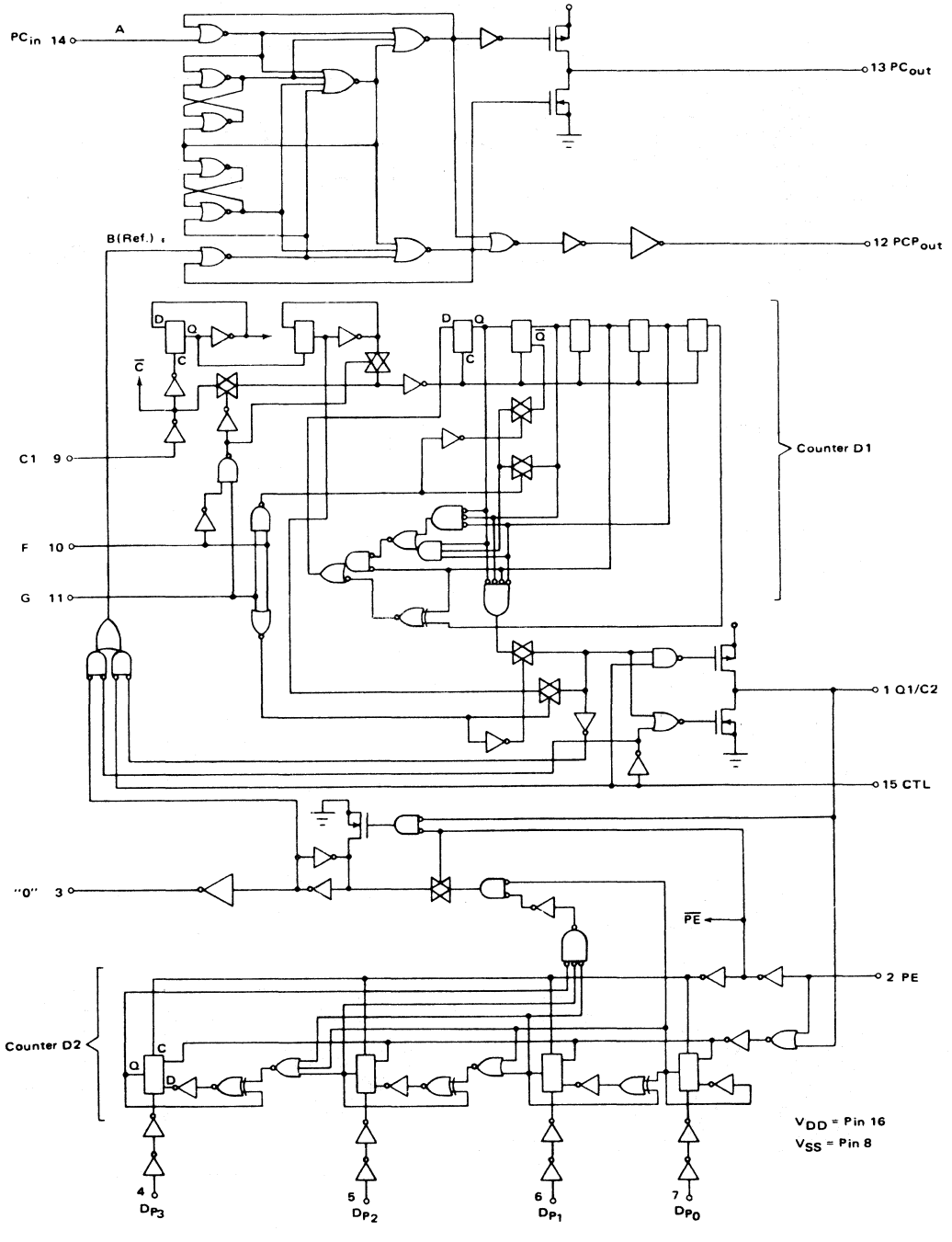


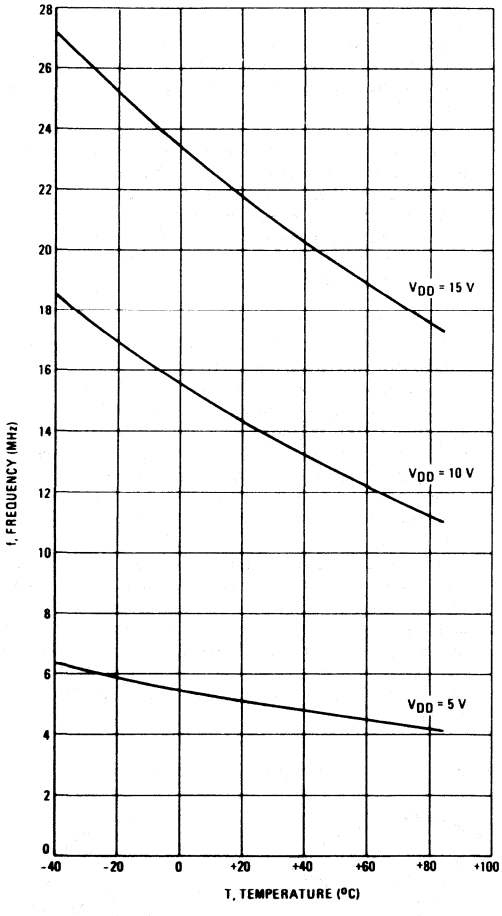
FIGURE 3 – COUNTER D2



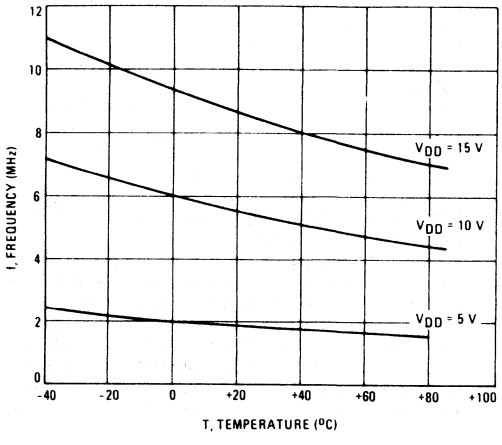
LOGIC DIAGRAM



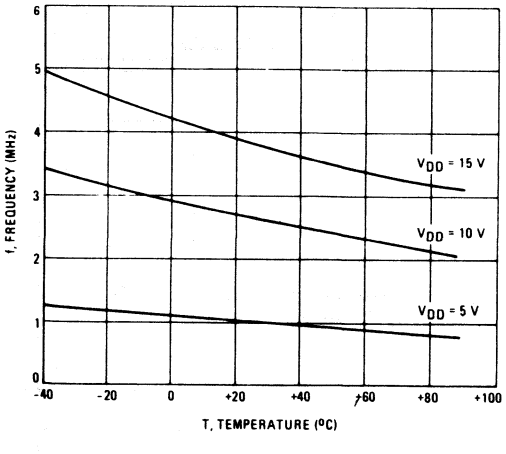
Typical Maximum Frequency Divider D1
Division ratios: 4, 64 or 100 (CL = 50 pF)



Typical Maximum Frequency Divider D1
Division ratio: 16 (CL = 50 pF)



Typical Maximum Frequency Divider D2
Division ratio: 2 (CL = 50 pF)



3

OPERATING CHARACTERISTICS

The MC14568B contains a phase comparator, a fixed divider (÷ 4, ÷ 16, ÷ 64, ÷ 100) and a programmable divide-by-N 4-bit counter.

PHASE COMPARATOR

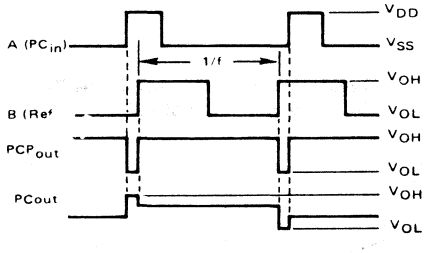
The phase comparator is a positive edge controlled logic circuit. It essentially consists of four flip-flops and an output pair of MOS transistors. Only one of its inputs (PC_{in}, pin 14) is accessible externally. The second is connected to the output of one of the two counters D1 or D2 (see block diagram).

Duty cycles of both input signals (at A and B) need not be taken into consideration since the comparator responds to leading edges only.

If both input signals have identical frequencies but different phases, with signal A (pin 14) leading signal B (Ref.), the comparator output will be high for the time equal to the phase difference.

If signal A lags signal B, the output will be low for the same time. In between, the output will be in a three-state condition and the voltage on the capacitor of an RC filter normally connected at this point will have some intermediate value (see Figure 4). When used in a phase locked loop, this value will adjust the Voltage Controlled Oscillator frequency by reducing the phase difference between the reference signal and the divided VCO frequency to zero.

FIGURE 4 – PHASE COMPARATOR WAVEFORMS



If the input signals have different frequencies, the output signal will be high when signal B has a lower frequency than signal A, and low otherwise.

Under the same conditions of frequency difference, the output will vary between V_{OH} (or V_{OL}) and some intermediate value until the frequencies of both signals are equal and their phase difference equal to zero, i.e. until locked condition is obtained.

Capture and lock range will be determined by the VCO frequency range. The comparator is provided with a lock indicator output, which will stay at logic 1 in locked conditions.

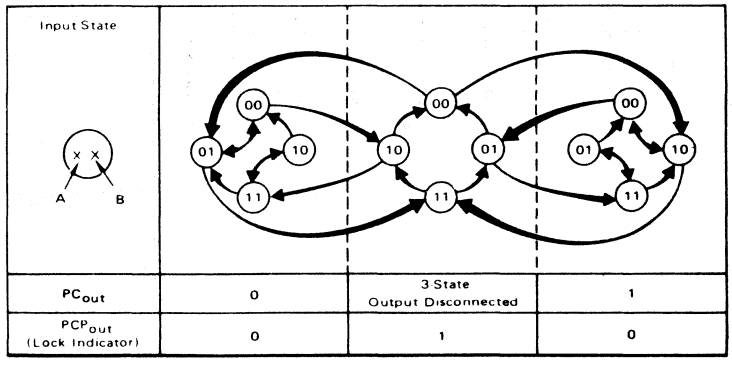
The state diagram (Figure 5) depicts the internal state transitions. It assumes that only one transition on either signal occurs at any time. It shows that a change of the output state is always associated with a positive transition of either signal. For a negative transition, the output does not change state. A positive transition may not cause the output to change; this happens when the signals have different frequencies.

DIVIDE BY 4, 16, 64 OR 100 COUNTER (D1)

This counter is able to work at an input frequency of 5 MHz for a V_{DD} value of 10 volts over the standard temperature range when dividing by 4, 64 and 100. Programming is accomplished by use of inputs F and G (pins 10 and 11) according to the truth table shown. Connecting the Control input (CTL, pin 15) to V_{DD} allows cascading this counter with the programmable divide-by-N counter provided in the same package. Independent operation is obtained when the Control input is connected to V_{SS}.

The different division ratios have been chosen to generate the reference frequences corresponding to the channel spacings normally required in frequency synthesizer applications. For example, with the division ratio 100 and a 5 MHz crystal stabilized source a reference frequency of 50 kHz is supplied to the comparator. The lower division ratios permit operation with low frequency crystals.

FIGURE 5 – PHASE COMPARATOR STATE DIAGRAM



PC_{out}	0	3-State Output Disconnected	1
PCP_{out} (Lock Indicator)	0	1	0

If used in cascade with the programmable divide-by-N counter, practically all usual reference frequencies, or channel spacings of 25, 20, 12.5, 10, 6.25 kHz, etc. are easily achievable.

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTER (D2)

This counter is programmable by using inputs D_{P0} . . . D_{P3} (pins 7 . . . 4). The Preset Enable input enables the parallel preset inputs D_{P0} . . . D_{P3}. The "0" output must be externally connected to the PE input for single stage applications. Since there is not a cascade feedback input, this counter, when cascaded, must be used as the most significant digit. Because of this, it can be cascaded with binary counters as well as with BCD counters (MC14569B, MC14522B, MC14526B).

TYPICAL APPLICATIONS

FIGURE 6 – CASCADING MC14568B AND MC14522B OR MC14526B WITH MC14569B

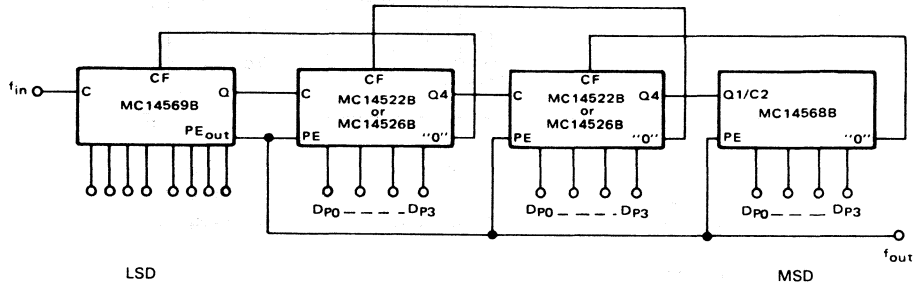
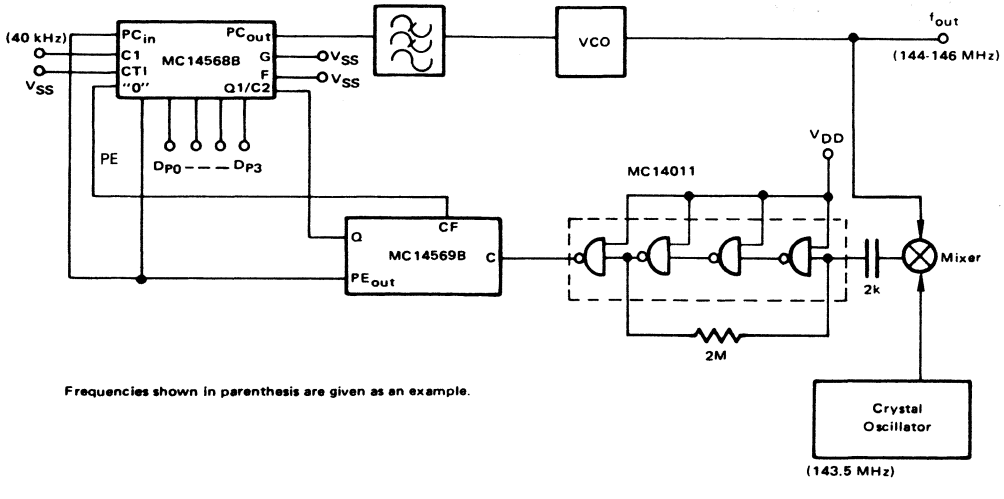
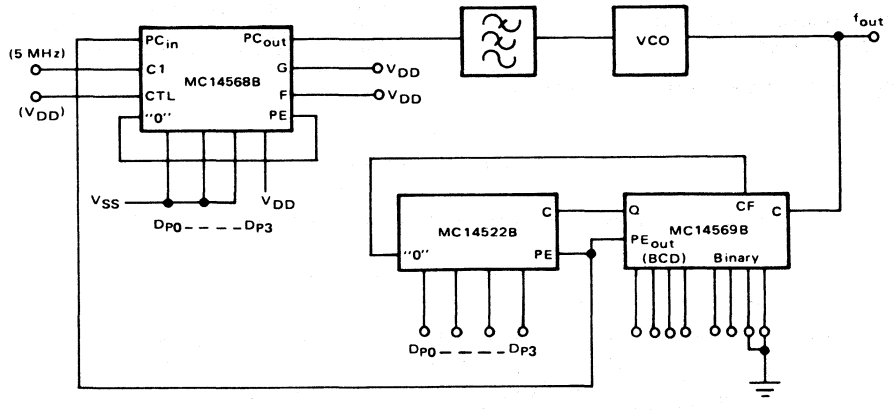


FIGURE 7 – FREQUENCY SYNTHESIZER WITH MC14568B and MC14569B USING A MIXER
(Channel Spacing 10 kHz)



Frequencies shown in parenthesis are given as an example.

FIGURE 8 – FREQUENCY SYNTHESIZER USING MC14568B, MC14569B AND MC14522B
(Without Mixer)



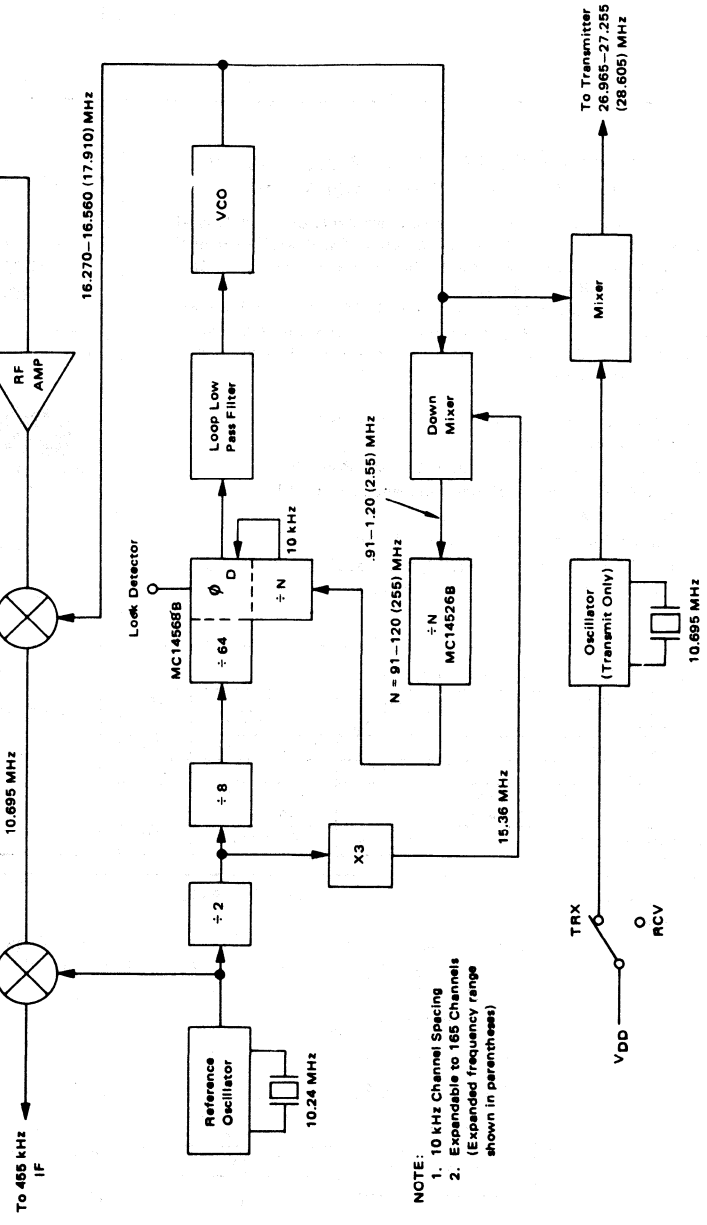
N_1	N_2	N_3
(0–5)	(0–9)	(0, 4, 8, 12)
(625 kHz steps)	(62.5 kHz steps)	(6.25 kHz steps)

Divide ratio = $160N_1 + 16N_2 + N_3$

Example:
$f_{out} = N_1$ (MHz) + N_2 (x100 kHz) + N_3 (x25 kHz)
Frequency range = 5 MHz
Channel spacing = 25 kHz
Reference frequency = 6.25 kHz

Figures shown in parenthesis refer to example.

FIGURE 9 – TYPICAL 23-CHANNEL CB FREQUENCY SYNTHESIZER FOR DOUBLE CONVERSION TRANSCEIVERS



MOTOROLA

MC14569B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

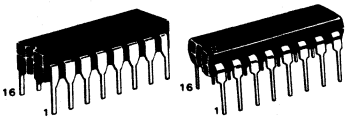
HIGH SPEED PROGRAMMABLE DIVIDE-BY-N DUAL 4-BIT BCD/BINARY COUNTER

HIGH SPEED PROGRAMMABLE DIVIDE-BY-N DUAL 4-BIT BCD/BINARY COUNTER

The MC14569B is a high speed programmable divide-by-N dual 4-bit BCD or binary down counter constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a single monolithic structure.

It has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- 9.5 MHz Typical Counting Rate at 10 V for Any Division Ratio Greater Than 1
- Speed-up Circuitry for Zero Detection and Preset Enable
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Quiescent Current = 5 nA typ/pkg @ 5 Vdc
- Can be Cascaded With MC14568B, MC14522B and MC14526B for Frequency Synthesizer Applications



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

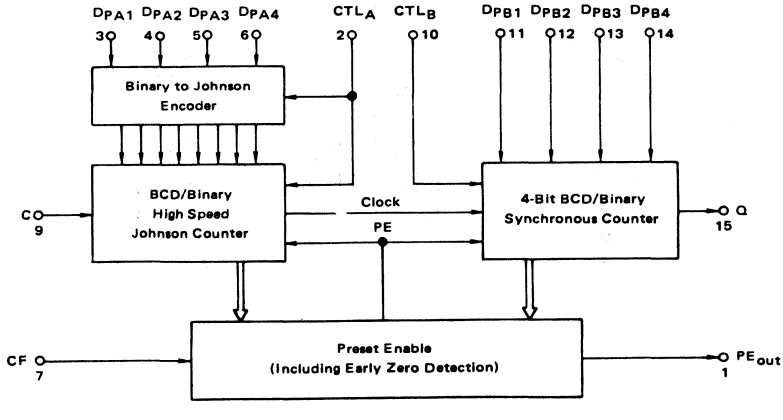
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM

CTL = "0" for Binary Count
CTL = "1" for BCD Count



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-0.88	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.005	50	–	150	μAdc
(Per Package)		10	–	100	–	0.010	100	–	300	
		15	–	200	–	0.015	200	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	(0.58 μA/kHz) f + I_{DD}							μAdc
		10	(1.20 μA/kHz) f + I_{DD}							
		15	(1.95 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Turn-On Delay Time	t_{PLH}					ns
PE_{out}		5.0	–	420	700	
		10	–	175	300	
		15	–	125	250	
Q Output		5.0	–	675	1200	ns
		10	–	285	500	
		15	–	200	400	
Turn-Off Delay Time	t_{PHL}					ns
PE_{out}		5.0	–	380	600	
		10	–	150	300	
		15	–	100	200	
Q Output		5.0	–	530	1000	ns
		10	–	225	400	
		15	–	155	300	
Clock Pulse Width	t_{WH}	5.0	300	100	–	ns
		10	150	45	–	
		15	115	30	–	
Clock Pulse Frequency #	f_{cl}	5.0	–	3.5	2.1	MHz
		10	–	9.5	5.7	
		15	–	13.0	7.8	
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	NO LIMIT			μs
		10				
		15				

#This implies that zero detection and preset enable are done while the clock is running at the specified frequency.

SWITCHING WAVEFORMS

FIGURE 1

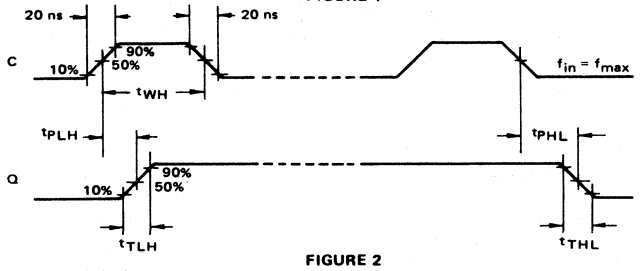
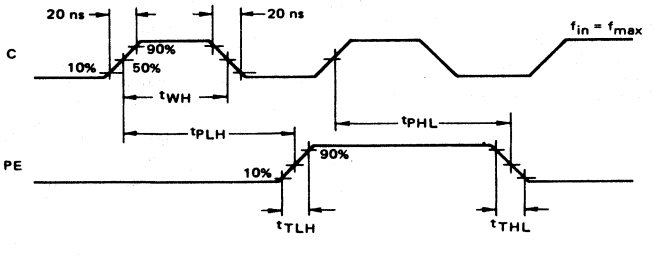


FIGURE 2



OPERATING CHARACTERISTICS

The MC14569B includes a high speed Johnson counter followed by a BCD/binary 4-bit synchronous counter (see block diagram). The use of an encoder allows the Johnson counter to be programmed (i.e. preset) in BCD or binary code through inputs D_{PA1}, D_{PA2}, D_{PA3}, and D_{PA4}.

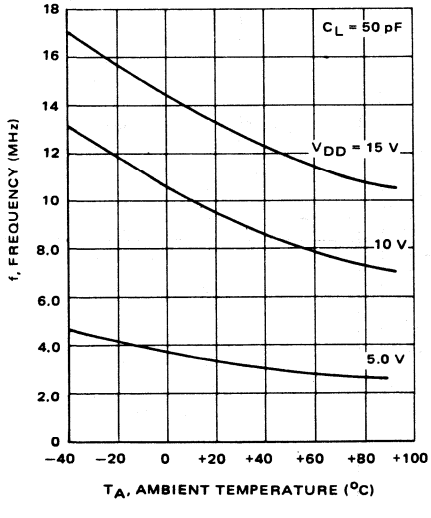
The BCD/binary counter can be programmed through inputs D_{PB1}, D_{PB2}, D_{PB3}, and D_{PB4}. For each counter a divide ratio of 10 (BCD count) or 16 (binary count) can be chosen independently by inputs CTL_A and CTL_B respectively. When one of those inputs is set high, the divide ratio of the corresponding counter is 10 (BCD); when it is set low, the division ratio is 16 (binary).

A Cascade Feedback input (pin 7), a Q output (pin 15) and a Preset Enable output (pin 1) made it possible to cascade the MC14568B, MC14522B and MC14526B with this device. CF, Q and PE_{out} of MC14569B must be respectively connected to "0", C and PE of the following counter.

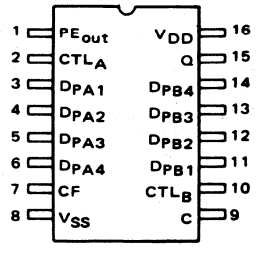
When MC14569B is used alone, CF must be connected to V_{DD}. One pulse will appear on output PE_{out} every N clock periods (N being the value programmed on the Dp inputs). Both counters included in MC14569B, and eventually all the counters which are cascaded, should normally be preset at the programmed values during the clock period where they all reach the count zero. For best speed performance, preset is started as soon as count 1 is detected. As a consequence, it is not possible to program a frequency division ratio of one. However, it is possible to program a division ratio of 11 (i.e. $D_{PA1}, \ldots D_{PA4}$ = 1,0,0,0 and $D_{PB1}, \ldots D_{PB4}$ = 1,0,0,0), or a division ratio of 101 if another counter is cascaded with the MC14569B.

This high speed configuration makes it possible to guarantee a maximum clock pulse frequency of 5.7 MHz for a 10 V V_{DD} supply for any division ratio greater than one. Due to the presence of the early zero detection, the circuit must be used in the two least significant digit positions.

Because all the circuitry is static, there is no minimum frequency specification for the Clock input, C (pin 9).



PIN ASSIGNMENT



MOTOROLA

MC14572UB

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX GATE

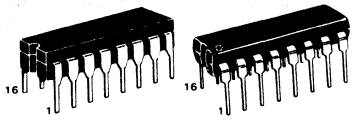
4 INVERTERS PLUS
2-INPUT NOR GATE PLUS
2-INPUT NAND GATE

3

HEX GATE

The MC14572UB hex functional gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

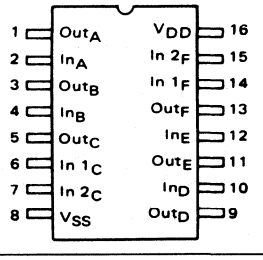
- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Single Supply Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Input Impedance = 10^{12} ohms typical
- NOR Input Pin Adjacent to V_{SS} Pin to Simplify Use As An Inverter
- NAND Input Pin Adjacent to V_{DD} Pin to Simplify Use As An Inverter
- NOR Output Pin Adjacent to Inverter Input Pin For OR Application
- NAND Output Pin Adjacent to Inverter Input Pin For AND Application
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

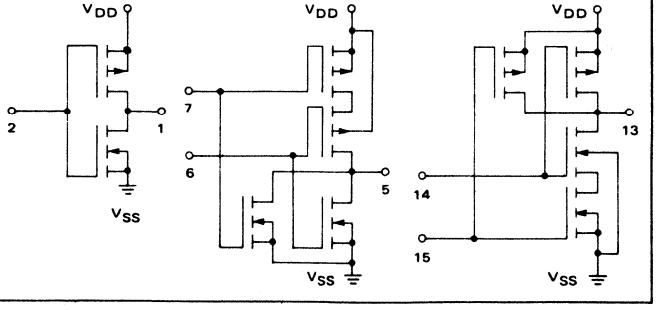
PIN ASSIGNMENT



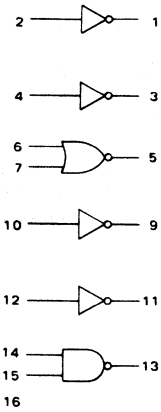
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.4	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.6	
"1" Level	V_{IH}									
(V_O = 1.4 or 3.6 Vdc)		5.0	3.6	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.1	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	–0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	-1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.89 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.80 µA/kHz) f + I_{DD}							
		15	I_T = (5.68 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

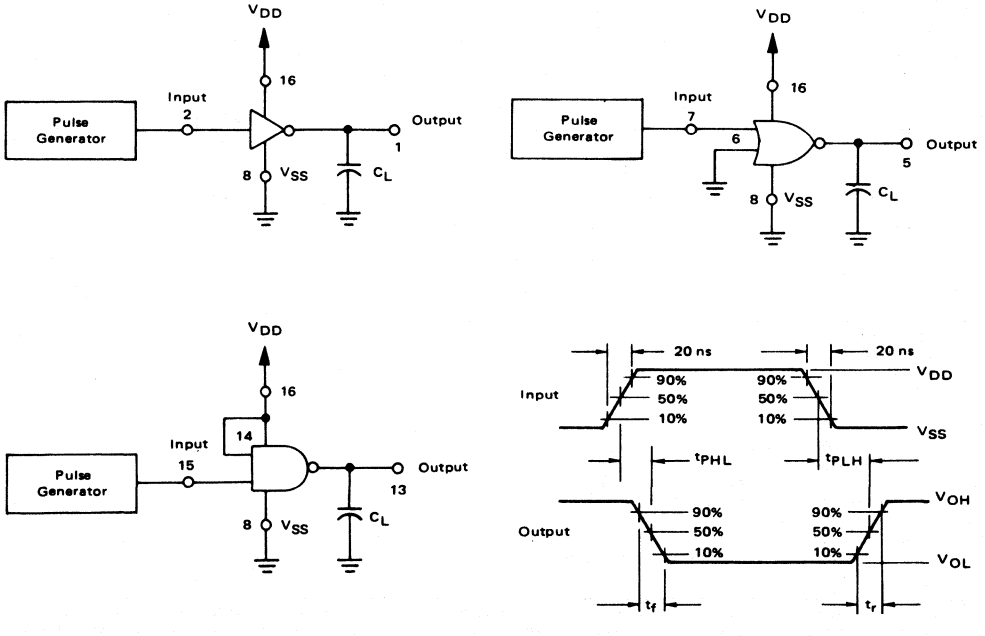
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 30 ns	t_{PHL}	5.0	–	115	200	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 22 ns		10	–	55	110	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 15 ns		15	–	40	85	

* The formulae given are for the typical characteristics only.

3

FIGURE 1 – SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



MOTOROLA

MC14580B

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

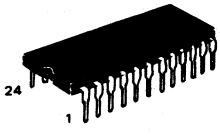
4 x 4 MULTIPORT REGISTER

4 x 4 MULTIPORT REGISTER

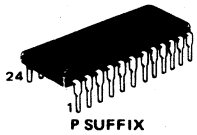
The MC14580B is a 4 by 4 multiport register useful in small scratch pad memories, arithmetic operations when coupled with an adder, and other data storage applications. It allows independent reading of any two words (or the same word at both outputs) while writing into any one of four words.

Address changing and data entry occur on the rising edge of the clock. When the write enable input is low, the contents of any word may be accessed but not altered.

- Logic Swing Independent of Fanout
- No Restrictions on Clock Input Rise or Fall Times
- 3-State Outputs
- Single Phase Clocking
- Quiescent Current = 10 nA/package typical @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range.
- Pin Compatible with CD40108



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709

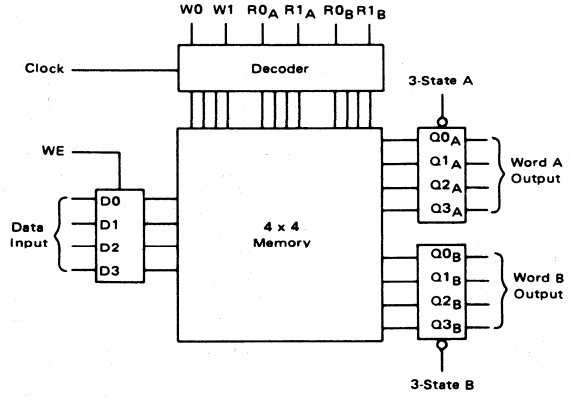
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

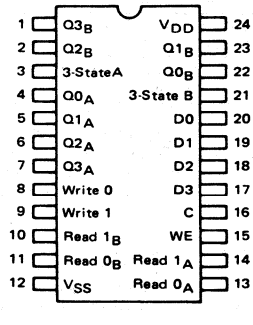
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



PIN ASSIGNMENT



V_{DD} = Pin 24
V_{SS} = Pin 12

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.020	10	–	300	
		15	–	20	–	0.030	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	50	–	0.010	50	–	375	μAdc
(Per Package)		10	–	100	–	0.020	100	–	750	
		15	–	200	–	0.030	200	–	1500	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.18 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.91 μA/kHz) f + I_{DD}							
		15	I_T = (2.67 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 4 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

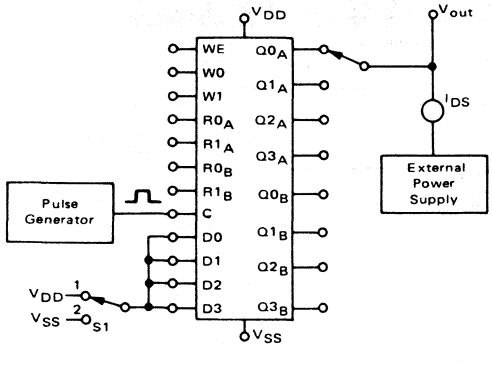
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time, Clock to Output	t_{PLH},					ns
t_{PHL}, t_{PLH} = (1.7 ns/pF) C_L + 1415 ns	t_{PHL}	5.0	–	1500	4500	
t_{PHL}, t_{PLH} = (0.66 ns/pF) C_L + 467 ns		10	–	500	1500	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 325 ns		15	–	350	1125	
Write Enable Setup Time	$t_{su(WE)}$	5.0	–	800	2000	ns
		10	–	300	750	
		15	–	180	550	
Write Enable Setup Time	$t_{su(WE)}$	5.0	–	-300	+150	ns
		10	–	-100	+75	
		15	–	-60	+55	
Write Enable Hold Time	$t_{h(WE)}$	5.0	–	-800	-200	ns
		10	–	-300	-75	
		15	–	-180	-45	
Address and Data Setup Time	$t_{su(D)}$,	5.0	–	150	450	ns
	$t_{su(W)}$	10	–	70	210	
		15	–	50	160	
Address and Data Hold Time	$t_{h(D)}$,	5.0	–	160	480	ns
	$t_{h(W)}$	10	–	65	195	
		15	–	50	150	
3-State Enable/Disable Delay Time**	t_{PHZ}, t_{PLZ},	5.0	–	355	900	ns
	t_{PZH}, t_{PZL}	10	–	140	350	
		15	–	85	250	
Positive Clock Pulse Width	t_{WH}	5.0	–	1000	3000	ns
(minimum)		10	–	350	1050	
		15	–	200	800	
Negative Clock Pulse Width	t_{WL}	5.0	–	400	1200	ns
(minimum)		10	–	85	255	
		15	–	60	200	

* The formulae given are for the typical characteristics only.

** Measured at the point of 10% change at output when the output load in 1.0 Ω and 50 pF.

FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



	Sink Current	Source Current
Position of S1	2	1
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS (3-State Inputs are High)

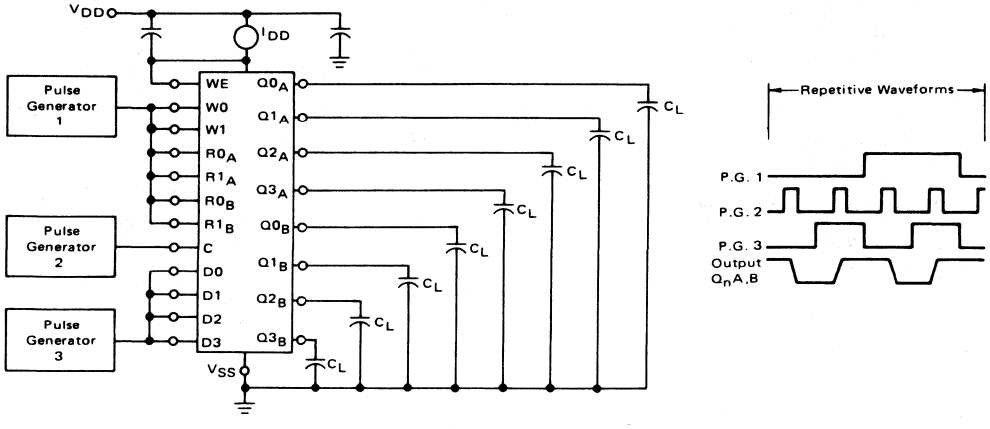


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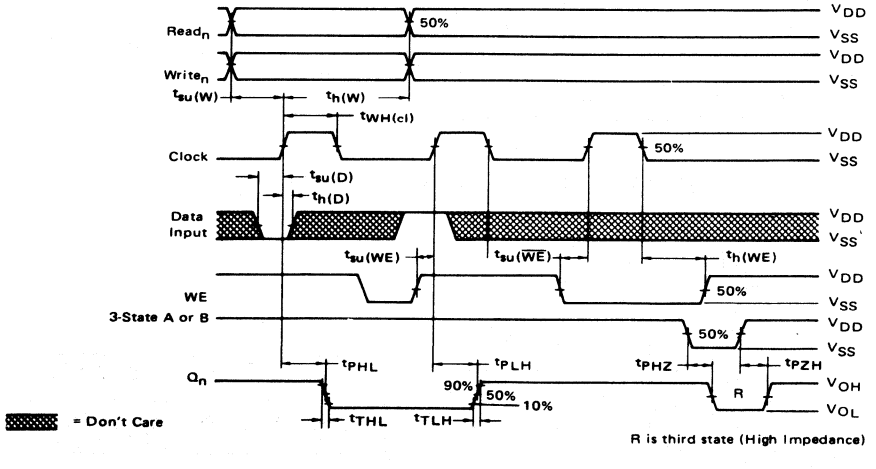
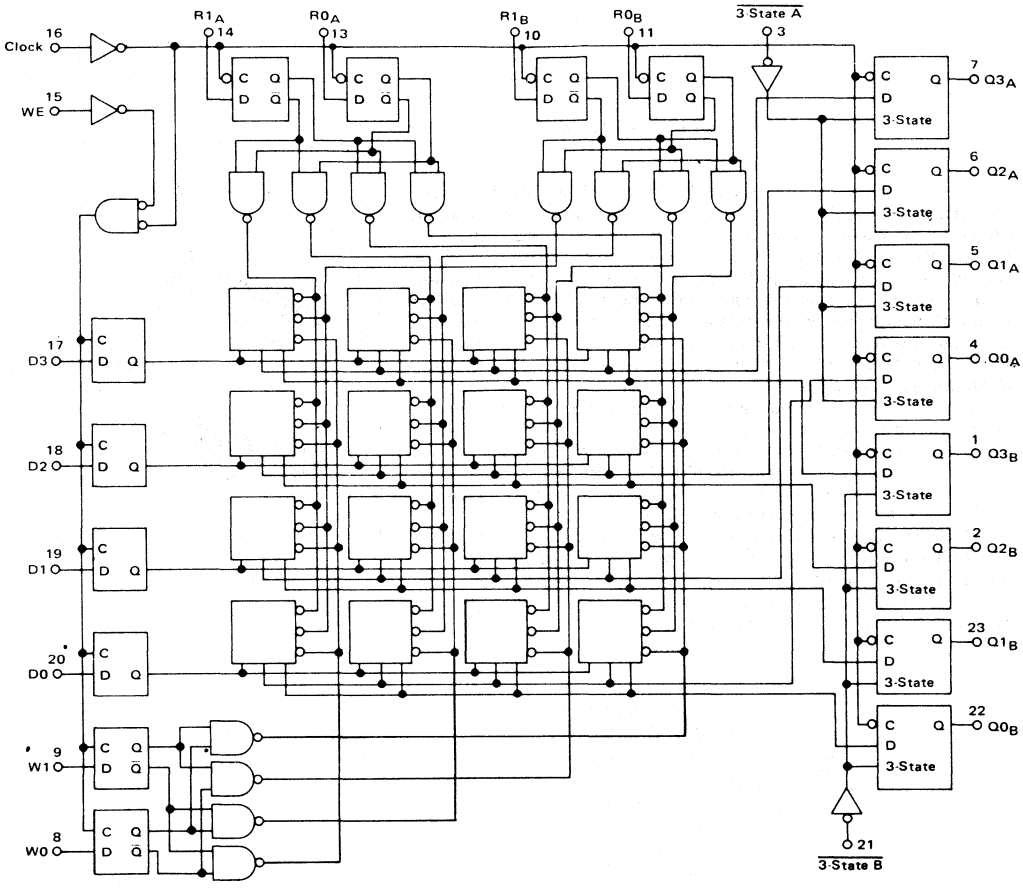
FIGURE 3 – AC WAVEFORMS AND DEFINITIONS



LOGIC DIAGRAM



TRUTH TABLE

Clock	WE	Write 1	Write 0	Read 1_A	Read 0_A	Read 1_B	Read 0_B	3-State A	3-State B	D_n	Q_nA	Q_nB
⎍	1	0	1	0	1	0	1	1	1	1	1	1
⎍	1	0	1	0	1	0	1	1	1	0	0	0
⎎	X	X	X	X	X	X	X	1	1	X	No Change	No Change
X	X	X	X	X	X	X	X	0	0	X	R	R
0	X	X	X	X	X	X	X	1	1	X	No Change	No Change
1	X	X	X	X	X	X	X	1	1	X	No Change	No Change
⎍	1	0	0	0	1	1	0	1	1	D_n to word 0	Contents of word 1 displayed	Contents of word 2 displayed
⎍	0	0	0	0	1	1	0	1	1	Word 0 not altered	Contents of word 1 displayed	Contents of word 2 displayed

R implies high resistance ~ 10^9 ohms .
X = Don't care

MOTOROLA

MC14581B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

4-BIT ARITHMETIC LOGIC UNIT

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The MC14581B is a CMOS 4-bit ALU logic unit capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 4-bit words. The level of the mode control input determines whether the output funciton is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the select inputs (S0 thru S3) with the mode control input high, while the desired arithmetic operation is selected by applying a low voltage to the mode control input, the required level to carry in, and the appropriate word to the select inputs. The word inputs and function outputs can be operated with either active high or active low data.

Carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the MC14582B as a second order look ahead block. An inverted ripple carry input (C_n) and a ripple carry output (C_{n+4}) are included for ripple through operation.

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the $\overline{A}$ and $\overline{B}$ inputs is provided using the A = B output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the C_{n+4} output can be used to indicate relative magnitude as shown in this table:

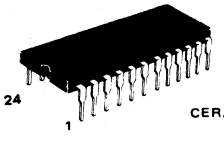
Data Level	C_n	C_{n+4}	Magnitude
Active High	H	H	A ≤ B
	L	H	A < B
	H	L	A > B
	L	L	A ≥ B
Active Low	L	L	A ≤ B
	H	L	A < B
	L	H	A > B
	H	H	A ≥ B

FEATURES:

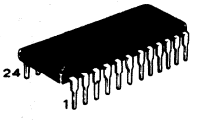
- Functional and Pinout Equivalent to 74181.
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- High Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Low Input Capacitance — 5.0 pF typical
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Load, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



L SUFFIX
CERAMIC PACKAGE
CASE 623

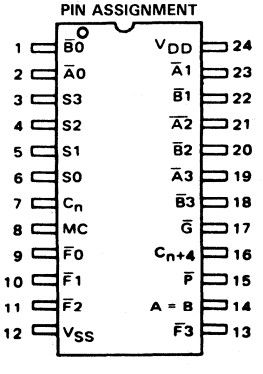


P SUFFIX
PLASTIC PACKAGE
CASE 709

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	-0.8	−1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	**0.005**	5.0	–	150	μAdc
(Per Package)		10	–	10	–	**0.010**	10	–	300	
		15	–	20	–	**0.015**	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	**0.005**	20	–	150	μAdc
(Per Package)		10	–	40	–	**0.010**	40	–	300	
		15	–	80	–	**0.015**	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.8 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.7 μA/kHz) f + I_{DD}							
		15	I_T = (5.5 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 8 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Sum in to Sum Out	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 620 ns		5.0	–	705	1410	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns		10	–	250	500	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	180	360	
Sum in to Sum Out (Logic Mode)	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 520 ns	t_{PHL}	5.0	–	605	1210	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 182 ns		10	–	215	430	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns		15	–	180	360	
Sum in to A = B	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 870 ns	t_{PHL}	5.0	–	955	1910	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 297 ns		10	–	330	660	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 220 ns		15	–	245	490	
Sum In to P or G	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 400 ns	t_{PHL}	5.0	–	485	970	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	–	130	260	
Sum In to C_{n+4}	t_{PLH}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 530 ns		5.0	–	615	1230	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 187 ns		10	–	220	440	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	–	160	360	
Carry In to Sum Out	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 295 ns	t_{PHL}	5.0	–	380	760	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 112 ns		10	–	145	290	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 80 ns		15	–	105	210	
Carry in to C_{n+4}	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 220 ns	t_{PHL}	5.0	–	305	610	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns		10	–	120	240	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 60 ns		15	–	85	170	

* The formulae given are for the typical characteristics only.

AC TEST SETUP REFERENCE TABLE

TEST	AC PATHS		DC DATA INPUTS		MODE	FIG. 3 WAVEFORM
	INPUTS	OUTPUTS	TO V_{SS}	TO V_{DD}		
Sum_{in} to Sum_{out} Delay Time	$\overline{A}0$	Any $\overline{F}$	Remaining $\overline{A}$'s C_n	All $\overline{B}$'s	Add	#1
Sum_{in} to $\overline{P}$ Delay Time	$\overline{A}0$	$\overline{P}$	Remaining $\overline{A}$'s C_n	All $\overline{B}$'s	Add	#1
Sum_{in} to $\overline{G}$ Delay Time	$\overline{B}0$	$\overline{G}$	All $\overline{A}$'s C_n	Remaining $\overline{B}$'s	Add	#1
Sum_{in} to C_{n+4} Delay Time	$\overline{B}0$	C_{n+y}	All $\overline{A}$'s C_n	Remaining $\overline{B}$'s	Add	#2
C_n to Sum_{out} Delay Time	C_n	Any $\overline{F}$	All $\overline{A}$'s	All $\overline{B}$'s	Add	#1
C_n to C_{n+4} Delay Time	C_n	C_{n+4}	All $\overline{A}$'s	All $\overline{B}$'s	Add	#1
Sum_{in} to A = B Delay Time	$\overline{A}0$	A = B	All $\overline{B}$'s Remaining $\overline{A}$'s	C_n	Sub	#2
Sum_{in} to Sum_{out} Delay Time (Logic Mode)	$\overline{B}_0$	Any $\overline{F}$	All A's	M	Exclusive OR	#2

FIGURE 1 – TYPICAL SOURCE CURRENT TEST CIRCUIT

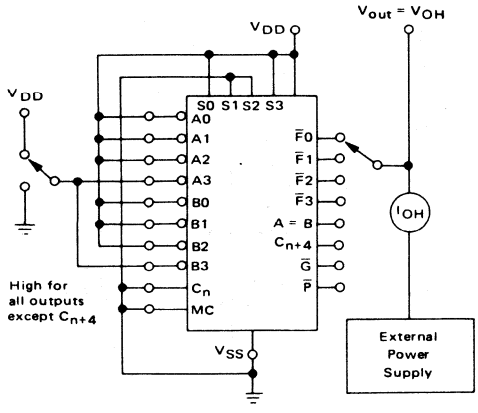


FIGURE 2 – TYPICAL SINK CURRENT TEST CIRCUIT

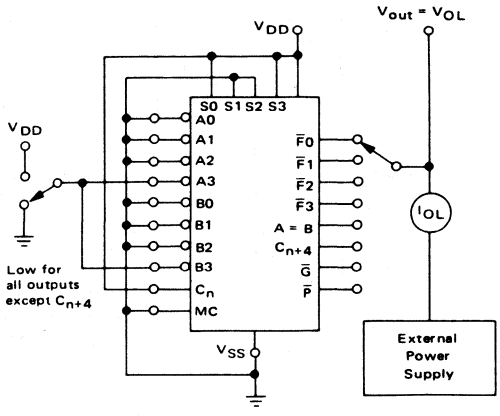


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

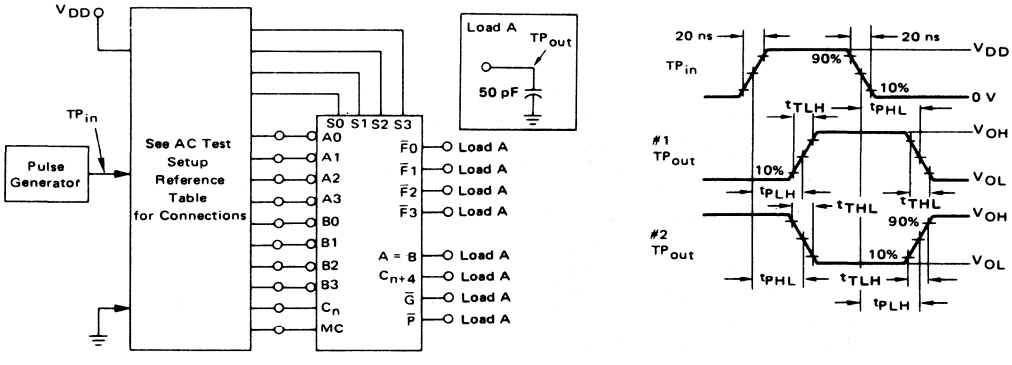
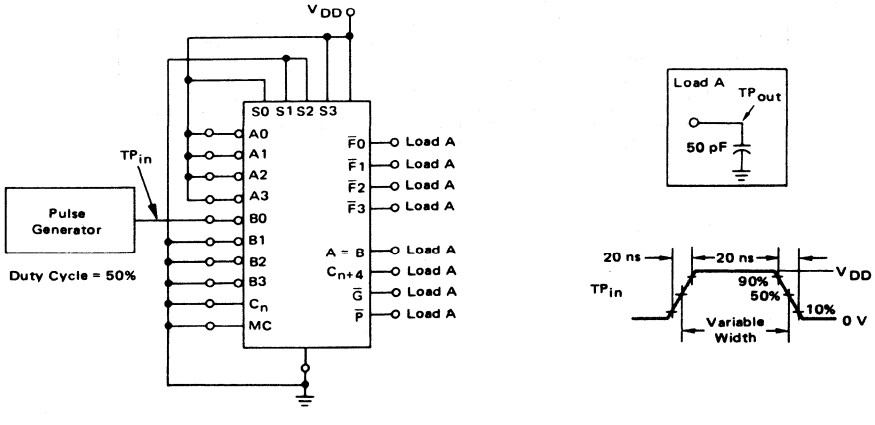
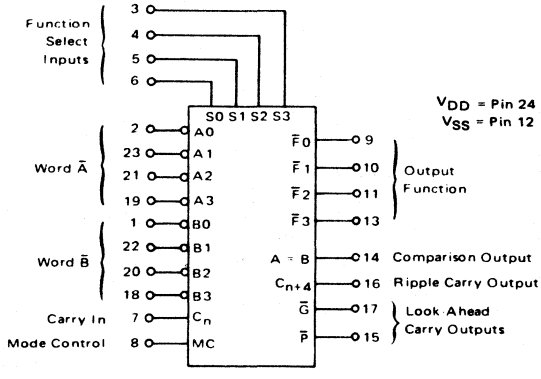


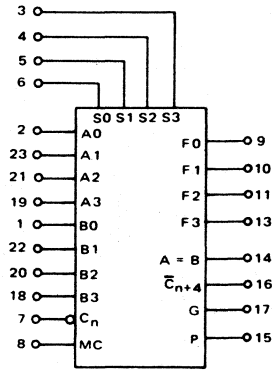
FIGURE 4 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



BLOCK DIAGRAM (ACTIVE LOW)



BLOCK DIAGRAM (ACTIVE HIGH)



TRUTH TABLE

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW		INPUTS/OUTPUTS ACTIVE HIGH	
				LOGIC FUNCTION	ARITHMETIC* FUNCTION	LOGIC FUNCTION	ARITHMETIC* FUNCTION
S3	S2	S1	S0	(MC = H)	(MC = L, C_n = L)	(MC = H)	(MC = L, $\bar{C}_n$ = H)
L	L	L	L	$\bar{A}$	A minus 1	$\bar{A}$	A
L	L	L	H	$\overline{A\bar{B}}$	AB minus 1	$\overline{A+\bar{B}}$	A+B
L	L	H	L	$\bar{A}+B$	A$\bar{B}$ minus 1	$\bar{A}B$	A+$\bar{B}$
L	L	H	H	Logic "1"	minus 1	Logic "0"	minus 1
L	H	L	L	$\overline{A+\bar{B}}$	A plus (A+$\bar{B}$)	$A\bar{B}$	A plus A$\bar{B}$
L	H	L	H	$\bar{B}$	AB plus (A+$\bar{B}$)	B	(A+B) plus A$\bar{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	A+$\bar{B}$	A+$\bar{B}$	A$\bar{B}$	A$\bar{B}$ minus 1
H	L	L	L	$\bar{A}B$	A plus (A+B)	$\overline{A+B}$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	A$\bar{B}$ plus (A+B)	B	(A+$\bar{B}$) plus AB
H	L	H	H	A+B	A+B	AB	AB minus 1
H	H	L	L	Logic "0"	A plus A	Logic "1"	A plus A
H	H	L	H	A$\bar{B}$	AB plus A	A+$\bar{B}$	(A+B) plus A
H	H	H	L	AB	A$\bar{B}$ plus A	A+B	(A+$\bar{B}$) plus A
H	H	H	H	A	A	A	A minus 1

* Expressed as two's complements. For arithmetic function with C_n in the opposite state, the resulting function is as shown plus 1.

MOTOROLA

MC14582B

LOOK-AHEAD CARRY BLOCK

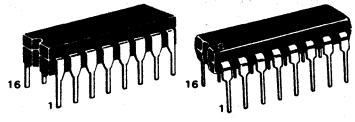
The MC14582B is a CMOS look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The device is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table shown below.

- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- High Speed Operation – 140 ns typical @ V_{DD} = 10 Vdc (from Data-in to Carry-out)
- Expandable to any Number of Bits
- Noise Immunity = 45% of V_{DD} typical
- All Buffered Outputs
- Low Power Dissipation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

LOOK-AHEAD CARRY BLOCK



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC EQUATIONS

$C_{n+x} = \overline{G0} + (\overline{P0} \bullet C_n)$

$C_{n+y} = \overline{G1} + (\overline{P1} \bullet \overline{G0}) + (\overline{P1} \bullet \overline{P0} \bullet C_n)$

$C_{n+z} = \overline{G2} + (\overline{P2} \bullet \overline{G1}) + (\overline{P2} \bullet \overline{P1} \bullet \overline{G0}) + (\overline{P2} \bullet \overline{P1} \bullet \overline{P0} \bullet C_n)$

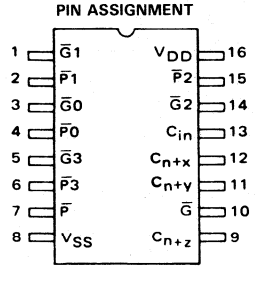
$\overline{G} = \overline{G3} + (\overline{P3} \bullet \overline{G2}) + (\overline{P3} \bullet \overline{P2} \bullet \overline{G1}) + (\overline{P1} \bullet \overline{P2} \bullet \overline{P3} \bullet \overline{G0})$

$\overline{P} = \overline{P3} \bullet \overline{P2} \bullet \overline{P1} \bullet \overline{P0}$

PIN DESIGNATIONS

DESIGNATION	PIN NO's	FUNCTION
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	3,1,14,5	Active-Low Carry-Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	4,2,15,6	Active-Low Carry-Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y} C_{n+z}	12,11,9	Carry Outputs
$\overline{G}$	10	Active-Low Group Carry-Generate Output
$\overline{P}$	7	Active-Low Group Carry-Propagate Output

PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	–	-0.8	−1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.4 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.8 µA/kHz) f + I_{DD}							
		15	I_T = (4.3 µA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

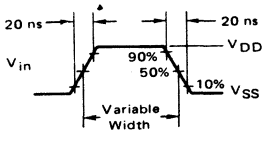
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 260 ns		Clock to Q	–	345	690	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 107 ns		10	–	140	280	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns		15	–	110	220	

* The formulae given are for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



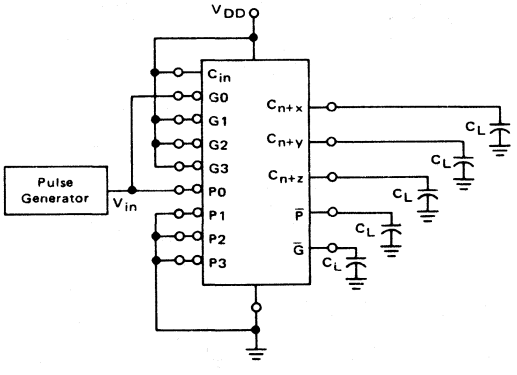


FIGURE 2 – SOURCE CURRENT TEST CIRCUIT

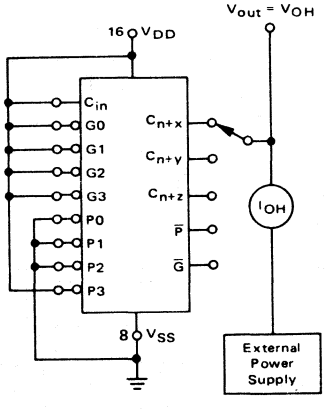


FIGURE 3 – SINK CURRENT TEST CIRCUIT

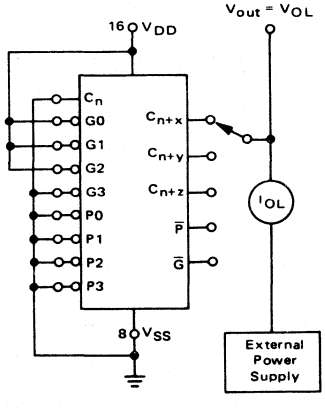
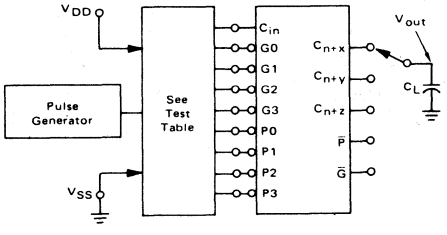
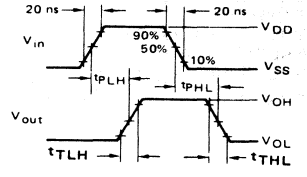


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

TEST TABLE

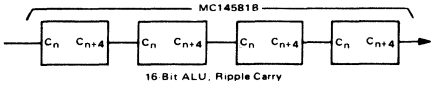
AC PATHS		DC DATA	
INPUT	OUTPUT	To V_{SS}	To V_{DD}
$\overline{P}0$	$\overline{P}$	Remaining $\overline{P}$'s, C_n	$\overline{G}$'s
$\overline{G}0$	$\overline{G}$	$\overline{P}$'s, C_n	Remaining $\overline{G}$'s
C_n	C_{n+x}, C_{n+y} C_{n+z}	$\overline{P}$'s	$\overline{G}$'s

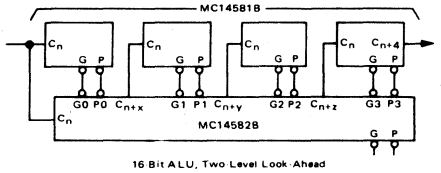


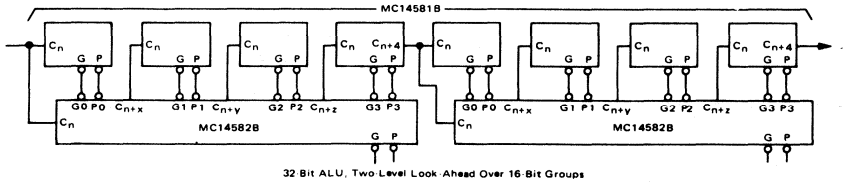


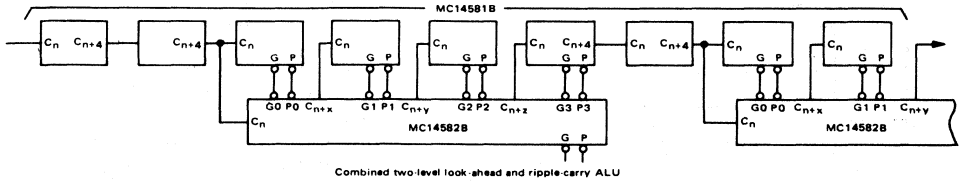
3

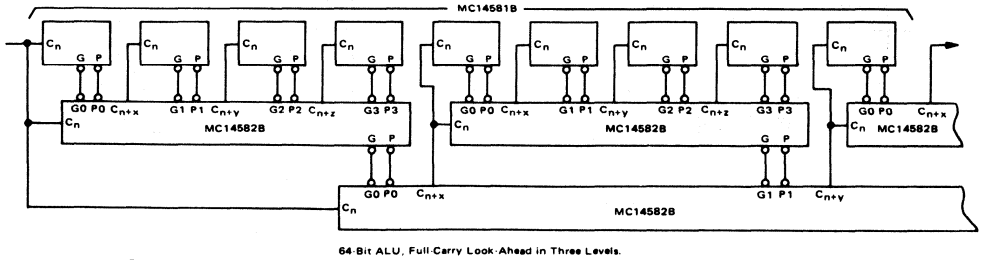
TYPICAL APPLICATIONS











A and B inputs and F outputs are not shown (MC14581B).

MOTOROLA

MC14583B

CMOS SSI

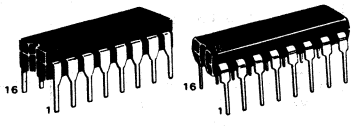
(LOW-POWER COMPLEMENTARY MOS)

DUAL SCHMITT TRIGGER

DUAL SCHMITT TRIGGER

The MC14583B is a dual Schmitt trigger constructed with complementary P-channel and N-channel MOS devices on a monolithic silicon substrate. Each Schmitt trigger is functionally independent except for a common 3-state input and an internally-connected Exclusive OR output for use in line receiver applications. Trigger levels are adjustable through the positive, negative, and common terminals with the use of external resistors. Applications include the speed-up of a slow waveform edge in interface receivers, level detectors, etc.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Schmitt Trigger Input Noise Immunity = 60% of V_{DD} Typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Resistor Adjustable Trigger Levels



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

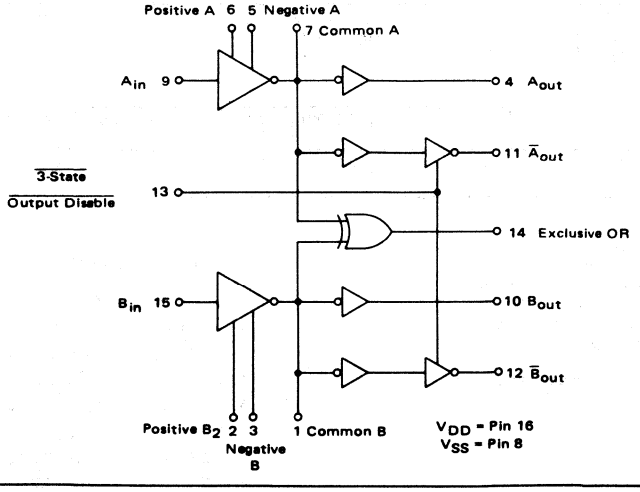
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

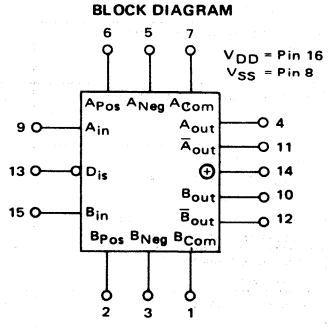
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



BLOCK DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS				
A	B	$\overline{Dis}$	A_{out}	$\bar{A}_{out}$	B_{out}	$\bar{B}_{out}$	⊕
0	0	0	0	R	0	R	0
0	0	1	0	1	0	1	0
0	1	0	0	R	1	R	1
0	1	1	0	1	1	0	1
1	0	0	1	R	0	R	1
1	0	1	1	0	0	1	1
1	1	0	1	R	1	R	0
1	1	1	1	0	1	0	0

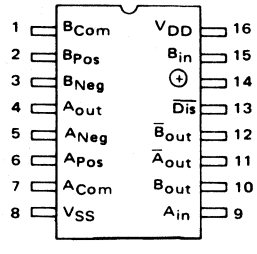
R = High resistance at output

ELECTRICAL CHARACTERISTICS (R1 = R2 = ∞)

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# A and B "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.2	–	–1.0	–1.7	–	-0.7	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.25	–	-0.2	-0.36	–	-0.14	–	
(V_{OH} = 9.5 Vdc)		10	–0.62	–	-0.5	-0.9	–	-0.35	–	
(V_{OH} = 13.5 Vdc)		15	–1.8	–	-1.5	-3.5	–	-1.1	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–1.0	–	-0.8	–1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)		5.0	–0.2	–	-0.16	–0.36	–	-0.12	–	
(V_{OH} = 9.5 Vdc)		10	–0.5	–	-0.4	–0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)		15	–1.4	–	-1.2	–3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
(Per Package)		10	–	0.50	–	0.0010	0.50	–	15.0	
		15	–	1.00	–	0.0015	1.00	–	30.0	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
(Per Package)		10	–	2.0	–	0.0010	2.0	–	15.0	
		15	–	4.0	–	0.0015	4.0	–	30.0	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.33 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (2.65 μA/kHz) f + I_{DD}							
		15	I_T = (3.98 μA/kHz) f + I_{DD}							
Three-State Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	μAdc
Three-State Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.00001	±1.0	–	±7.5	μAdc

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 5 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

PIN ASSIGNMENT



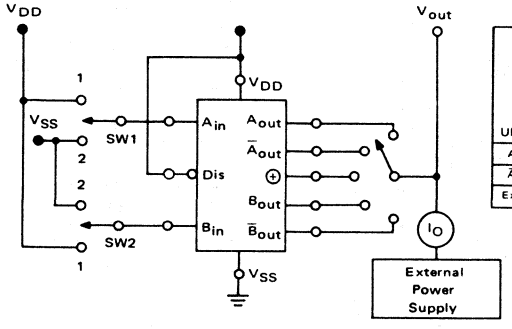
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
A_{in}, B_{in} to A_{out}, B_{out}	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	–	650	1300	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	–	230	460	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns		15	–	150	300	
A_{in}, B_{in} to A_{out}, B_{out}	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 1015 ns	t_{PHL}	5.0	–	1100	2200	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 347 ns		10	–	380	760	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 235 ns		15	–	260	520	
A_{in}, B_{in} to Exclusive OR	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns	t_{PHL}	5.0	–	750	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns		10	–	280	560	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	–	170	340	
3-State Enable, Disable Delay Time (see figure 5)	t_{on},					ns
t_{on}, t_{off} = (1.7 ns/pF) C_L + 140 ns	t_{off}	5.0	–	225	450	
t_{on}, t_{off} = (0.66 ns/pF) C_L + 57 ns		10	–	90	180	
t_{on}, t_{off} = (0.5 ns/pF) C_L + 30 ns		15	–	55	110	
Positive Threshold Voltage	V_{T+}	5.0	–	3.30	–	Vdc
(R1, R2 = 5.0 kΩ)		10	–	5.70	–	
		15	–	8.20	–	
Negative Threshold Voltage	V_{T-}	5.0	–	1.70	–	Vdc
(R1, R2 = 5.0 kΩ)		10	–	4.30	–	
		15	–	6.80	–	
Hysteresis Voltage	V_H	5.0	0.85	1.70	3.40	Vdc
(R1, R2 = 5.0 kΩ)		10	0.70	1.40	2.80	
		15	0.70	1.40	2.80	
Threshold Voltage Variation, A to B	ΔV_T	5.0	–	0.1	–	Vdc
(R1, R2 = 5.0 kΩ)		10	–	0.15	–	
		15	–	0.20	–	

* The formulae given are for the typical characteristics only.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

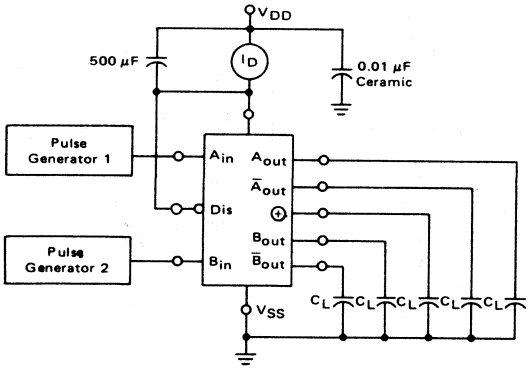
FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CHARACTERISTICS TEST CIRCUIT



OUTPUT UNDER TEST	OUTPUT SOURCE CHARACTERISTICS		OUTPUT SINK CHARACTERISTICS	
	TEST VALUE: $V_{GS} = -V_{DD}$, $V_{DS} = V_{out} - V_{DD}$		TEST VALUE: $V_{GS} = V_{DD}$, $V_{DS} = V_{out}$	
	SWITCH POSITION		SWITCH POSITION	
	SW1	SW2	SW1	SW2
A_{out}, B_{out}	1	1	2	2
$\bar{A}_{out}$, $\bar{B}_{out}$	2	2	1	1
Exclusive OR	1	2	1	1

3

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



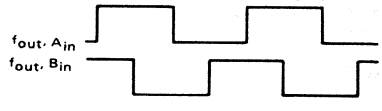
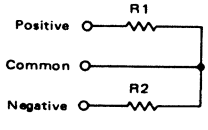
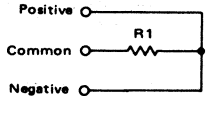


FIGURE 3 – TYPICAL THRESHOLD POINTS

A – Feedback scheme for independent threshold adjustment:



B – Feedback scheme for hysteresis adjustment:



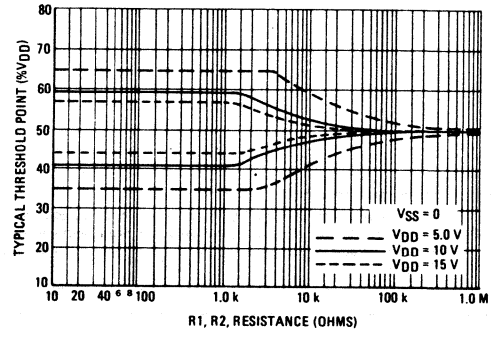
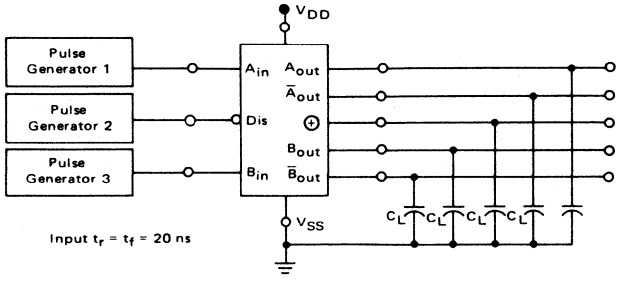
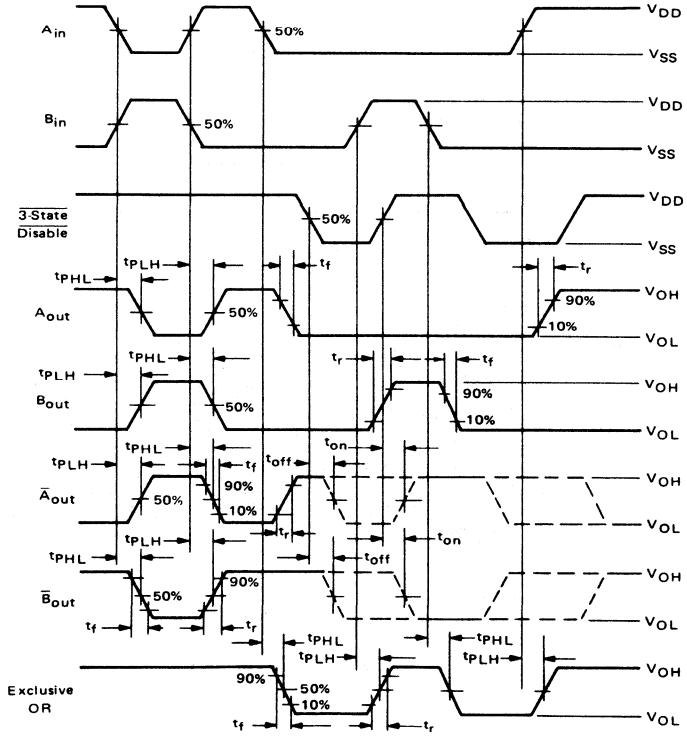


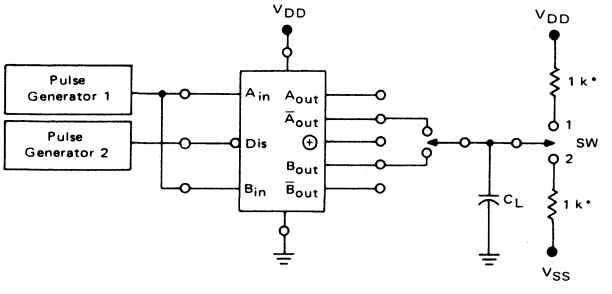
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





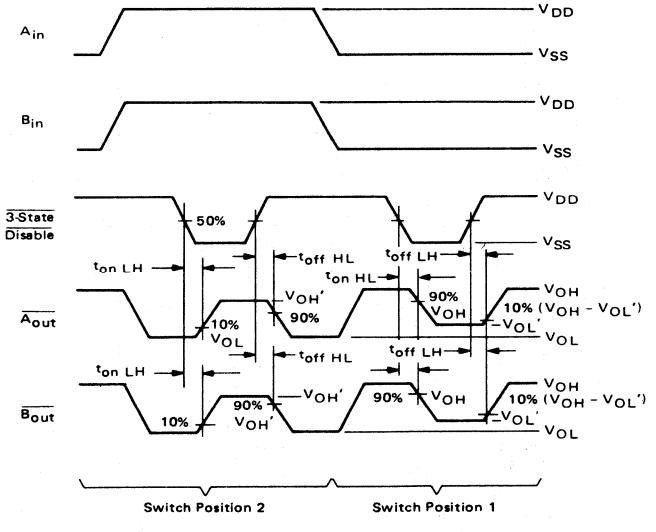
Note: Dashed lines indicate high output resistance.

FIGURE 5 – 3-STATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	SWITCH POSITION
$t_{on\ HL}$	1
$t_{on\ LH}$	2
$t_{off\ HL}$	2
$t_{off\ LH}$	1

*Metal film, ± 1%, 1/4 W or greater
C_L = 15 pF, which includes test circuit capacitance.



V_{OL}' and V_{OH}' refer to the levels present as a result of the 1 k ohm load resistors.

MOTOROLA

MC14584B

CMOS SSI

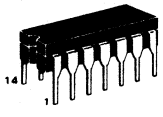
(LOW-POWER COMPLEMENTARY MOS)

HEX SCHMITT TRIGGER

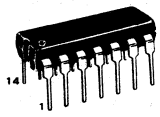
HEX SCHMITT TRIGGER

The MC14584B hex Schmitt Trigger is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These devices find primary use where low power dissipation and/or high noise immunity is desired. The MC14584B may be used in place of the MC14069UB hex inverter for enhanced noise immunity or to "square up" slowly changing waveforms.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Can Be Used to Replace MC14069UB
- For Greater Hysterisis, Use MC14106B which is Pin-for-Pin Replacement for CD40106B and MM74C14



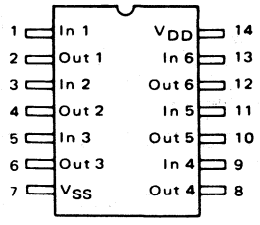
L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

3

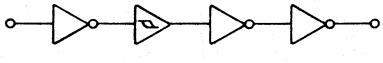
PIN ASSIGNMENT



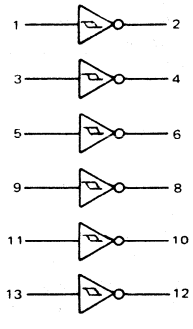
MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

EQUIVALENT CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	μAdc
		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	34	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.8 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.6 μA/kHz) f + I_{DD}							
		15	I_T = (5.4 μA/kHz) f + I_{DD}							
Hysteresis Voltage	V_H‡	5.0	0.27	1.0	0.25	0.55	1.0	0.21	1.0	Vdc
		10	0.36	1.3	0.30	0.70	1.2	0.25	1.2	
		15	0.77	1.7	0.60	1.1	1.5	0.50	1.4	
Threshold Voltage Positive-Going	V_{T+}	5.0	1.9	3.5	1.8	2.7	3.4	1.7	3.4	Vdc
		10	3.4	7.0	3.3	5.3	6.9	3.2	6.9	
		15	5.2	10.6	5.2	8.0	10.5	5.2	10.5	
Negative-Going	V_{T-}	5.0	1.6	3.3	1.6	2.1	3.2	1.5	3.2	Vdc
		10	3.0	6.7	3.0	4.6	6.7	3.0	6.7	
		15	4.5	9.7	4.6	6.9	9.8	4.7	9.9	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

†To calculate total supply current at loads other than 50 pF:
I_T (C_L) = I_T (50 pF) + 1 x 10^{-3} (C_L −50) V_{DD}f
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

**The formulas given are for the typical characteristics only at 25°C.

‡V_H = V_{T+} - V_{T-} (But maximum variation of V_H is specified as less than $V_{T+\,max}$ - $V_{T-\,min}$).

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Output Fall Time	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}	5.0	–	125	250	ns
		10	–	50	100	
		15	–	40	80	

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

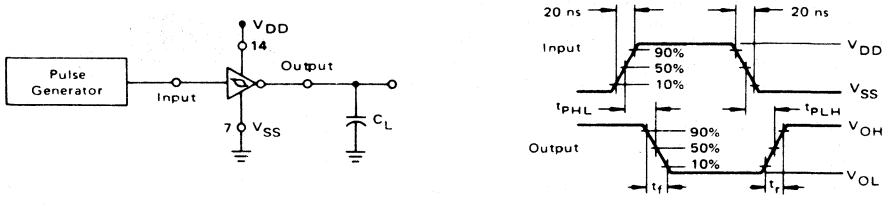


FIGURE 2 – TYPICAL SCHMITT TRIGGER APPLICATIONS

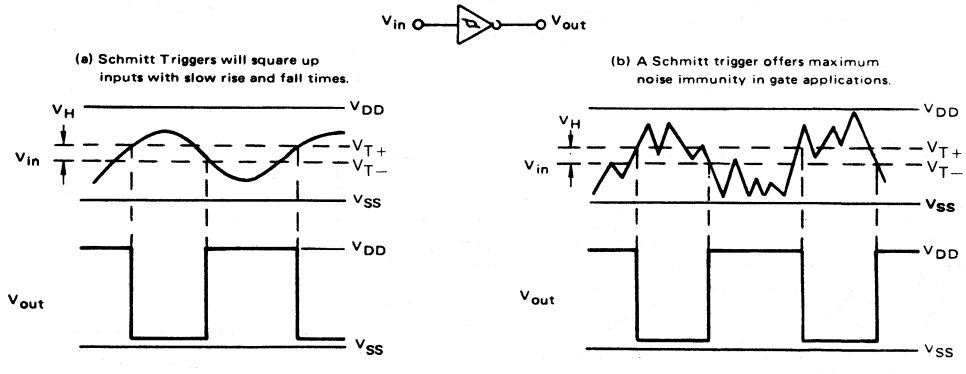
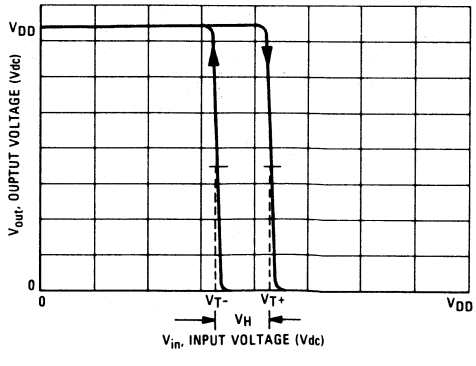


FIGURE 3 – TYPICAL TRANSFER CHARACTERISTICS



MOTOROLA

MC14585B

4-BIT MAGNITUDE COMPARATOR

The MC14585B 4-Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs ($A<A$, $A=B$, and $A>B$), and three outputs ($A<B$, $A=B$, and $A>B$). This device compares two 4-bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output. For words greater than 4-bits, units can be cascaded by connecting outputs ($A>B$), ($A<B$), and ($A=B$) to the corresponding inputs of the next significant comparator. Inputs ($A<B$), ($A=B$), and ($A>B$) on the least significant (first) comparator are connected to a low, a high, and a low, respectively.

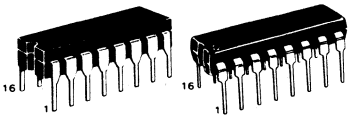
Application include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- High Fanout > 50
- Quiescent Current = 5.0 nA/package typical at 5 Vdc
- Expandable
- Applicable to Binary or 8421-BCD Code
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Can be Cascaded - See Fig. 3

CMOS MSI

(LOW POWER COMPLEMENTARY MOS)

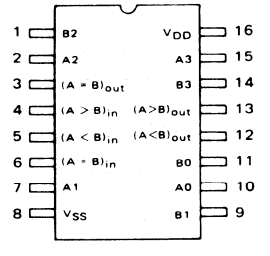
4-BIT MAGNITUDE COMPARATOR



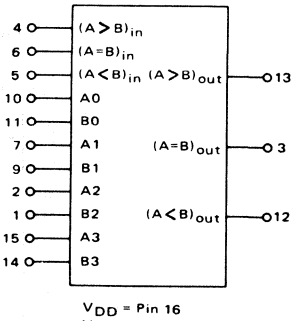
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



BLOCK DIAGRAM



VDD = Pin 16
VSS = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	×	×	×	×	×	×	0	0	1
A3=B3	A2>B2	×	×	×	×	×	0	0	1
A3=B3	A2=B2	A1>B1	×	×	×	×	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	×	×	×	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	×	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	×	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	×	1	0	0
A3=B3	A2=B2	A1=B1	A0=B0	1	1	×	1	1	0
A3=B3	A2=B2	A1=B1	A0<B0	×	×	×	1	0	0
A3=B3	A2=B2	A1<B1	×	×	×	×	1	0	0
A3=B3	A2<B2	×	×	×	×	×	1	0	0
A3<B3	×	×	×	×	×	×	1	0	0

× = Don't Care

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 Vdc)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 Vdc)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.6 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.8 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

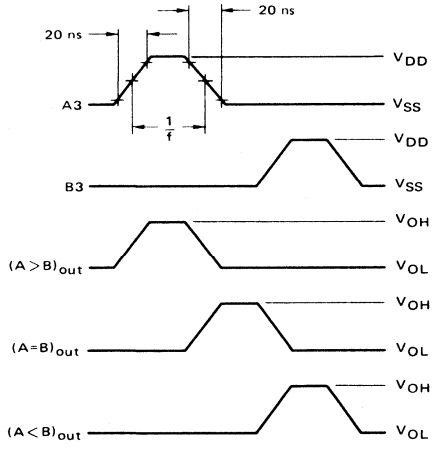
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	100	200	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	50	100	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	40	80	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Turn-Off Delay Time	t_{PLH},					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 345 ns	t_{PHL}	5.0	–	430	860	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 147 ns		10	–	180	360	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 105 ns		15	–	130	260	

* The formulae given are for the typical characteristics only.

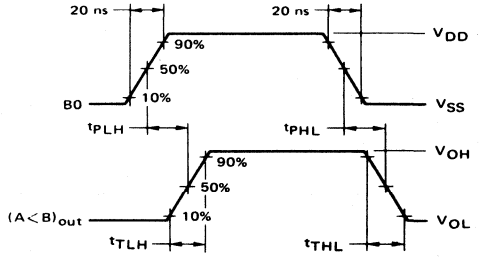
3

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS



Inputs (A > B) and (A=B) high, and inputs B2, A2, B1, A1, B0, A0 and (A < B) low
f in respect to a system clock.

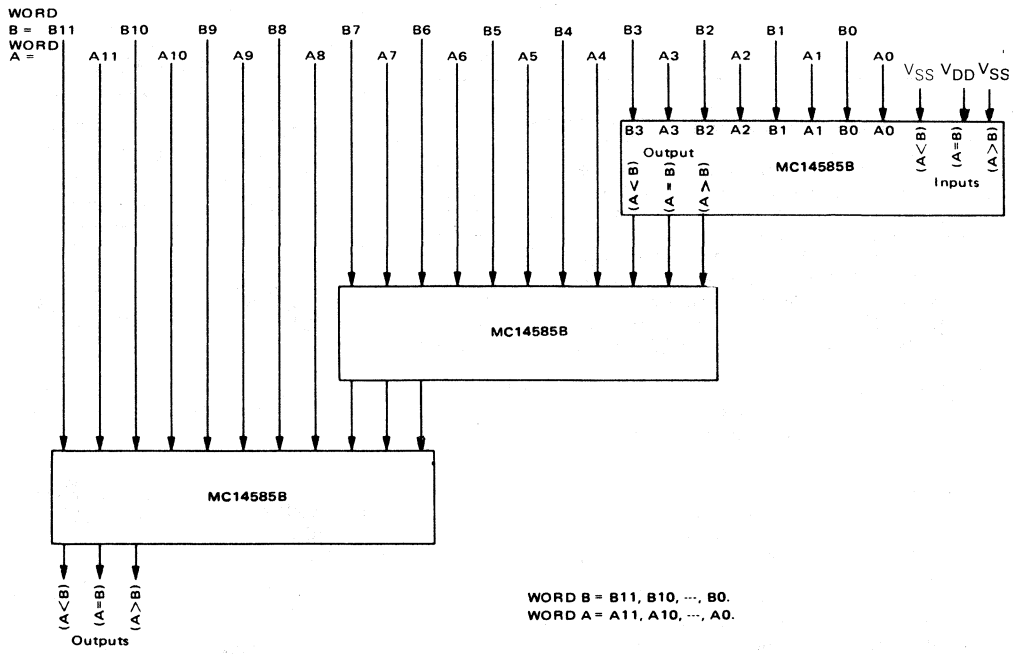
FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



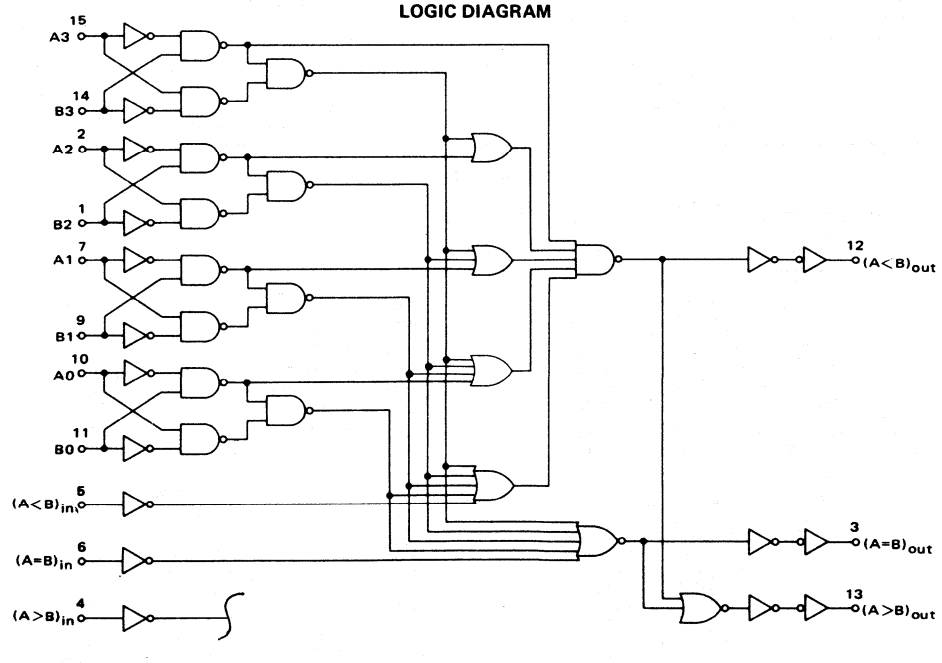
Inputs (A > B) and (A=B) high, and inputs B3, A3, B2, A2, B1, A1, A0, and (A < B) low.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 3 – CASCADING COMPARATORS



LOGIC DIAGRAM



MOTOROLA

MC14597B
MC14598B

CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

8-BIT, BUS-COMPATIBLE THREE-STATE LATCHES
Internal Counter — MC14597B
Binary Address — MC14598B

8-BIT BUS-COMPATIBLE LATCHES

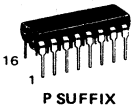
The MC14597B and MC14598B are 8-bit latches, one addressed with an internal counter and the other addressed with an external binary address. The 8 latch-outputs are high drive, three-state and bus line compatible. The drive capability allows direct applications with MPU systems such as the Motorola 6800 family.

With MC14597B, a 3-bit address counter (clocked on the falling edge of Increment) selects the appropriate latch. The latches of the MC14598B are accessed via the Address pins, A0, A1, and A2. A $\overline{\text{Full}}$ Flag is provided on the MC14597B to indicate the position of the Address counter.

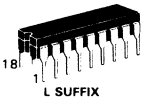
All 8 outputs from the latches are available in parallel when $\overline{\text{Enable}}$ is in the low state. Data is entered into a selected latch from the Data pin when the Strobe is high. Master reset is available on both parts.

- Serial Data Input
- Three-State Bus Compatible Parallel Outputs
- Three-State Control Pin ($\overline{\text{Enable}}$) TTL Compatible Input
- Open Drain $\overline{\text{Full}}$ Flag (Multiple Latch Wire-O Ring)
- Master Reset
- Level Shifting Inputs on All Except $\overline{\text{Enable}}$
- Noise Immunity — 45% of V_{DD} Typical
- Diode Protection — All Inputs
- Supply Voltage Range — 3.0 Vdc to 18 Vdc
- Capable of Driving TTL Over Rated Temperature Range
  With Fanout as Follows:
  1 TTL Load
  4 LSTTL Loads
  9 LPTTL Loads

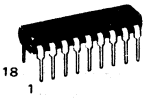
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 726

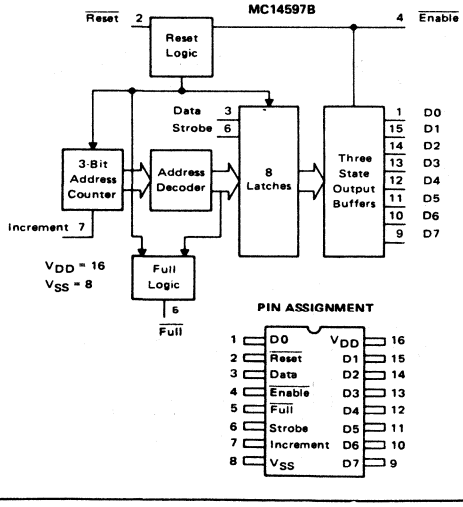


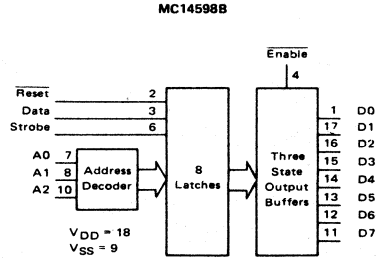
P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAMS





PIN ASSIGNMENT

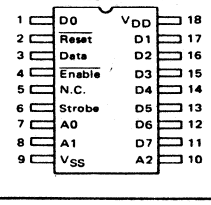
OUTPUT TRUTH TABLE

Enable	Outputs
1	High Impedence
0	D_n

D_n = State of nth latch

NC = No Connection

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltage referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, $\overline{\text{Enable}}$	V_{in}	-0.5 to V_{DD} +0.5	Vdc
Input Voltage, All Other Inputs	V_{in}	-0.5 to V_{DD} +12	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{out} be constrained to the range $V_{SS} \leq (V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# — $\overline{\text{Enable}}$ "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	0.8	–	1.1	0.8	–	0.8	
(V_O = 9.0 or 1.0 Vdc)		10	–	1.6	–	2.2	1.6	–	1.6	
(V_O = 13.5 or 1.5 Vdc)		15	–	2.4	–	3.4	2.4	–	2.4	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	2.0	–	2.0	1.9	–	2.0	–	
(V_O = 1.0 or 9.0 Vdc)		10	6.0	–	6.0	3.1	–	6.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	10	–	10	4.3	–	10	–	
Input Voltage# — "0" Level	V_{IL}									Vdc
Other Inputs										
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11	–	11	8.25	–	11	–	
Output Drive Current Source	I_{OH}									mAdc
($\overline{\text{Full}}$—Sink Only)										
(V_{OH} = 4.6 Vdc)		5.0	-1.0	–	-1.0	-2.0	–	-1.0	–	
(V_{OH} = 9.5 Vdc)		10	–	–	–	-6.0	–	–	–	
(V_{OH} = 13.5 Vdc)		15	–	–	–	-12	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	1.6	–	1.6	3.2	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)		10	–	–	–	6.0	–	–	–	
(V_{OL} = 1.5 Vdc)		15	–	–	–	12	–	–	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Three-State Leakage Current	I_{TL}									μAdc
(AL Device)		15	–	±0.1	–	±0.00001	±0.1	–	±3.0	
(CL/CP Device)		15	–	±1.0	–	±0.00001	±1.0	–	±7.5	
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	μAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
†Total Supply Current at an External Load Capacitance (C_L) of 130 pF	I_T	5.0	I_T = (2.0 μA/kHz)f + I_{DD}							
		10	I_T = (4.0 μA/kHz)f + I_{DD}							
		15	I_T = (6.0 μA/kHz)f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

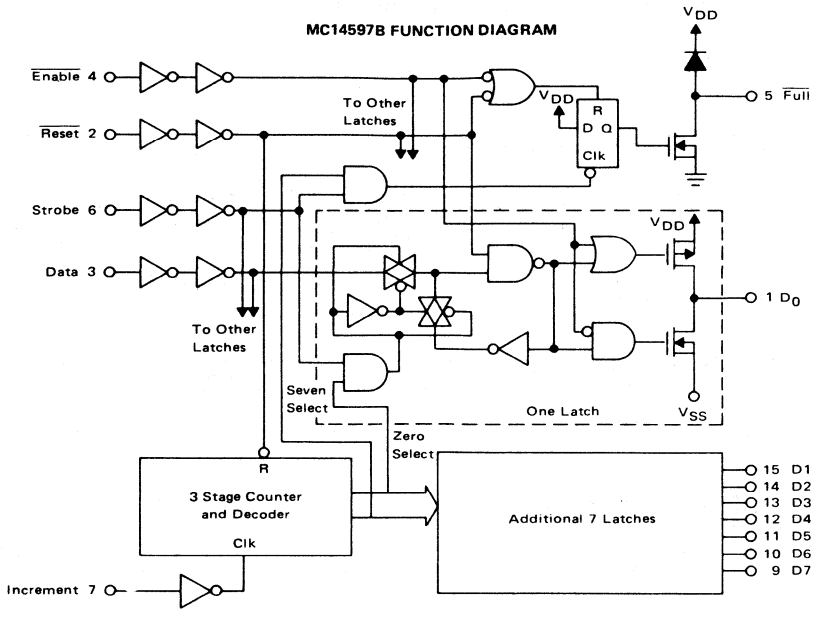
#Noise immunity specified for worst-case input combination. Noise Margin both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

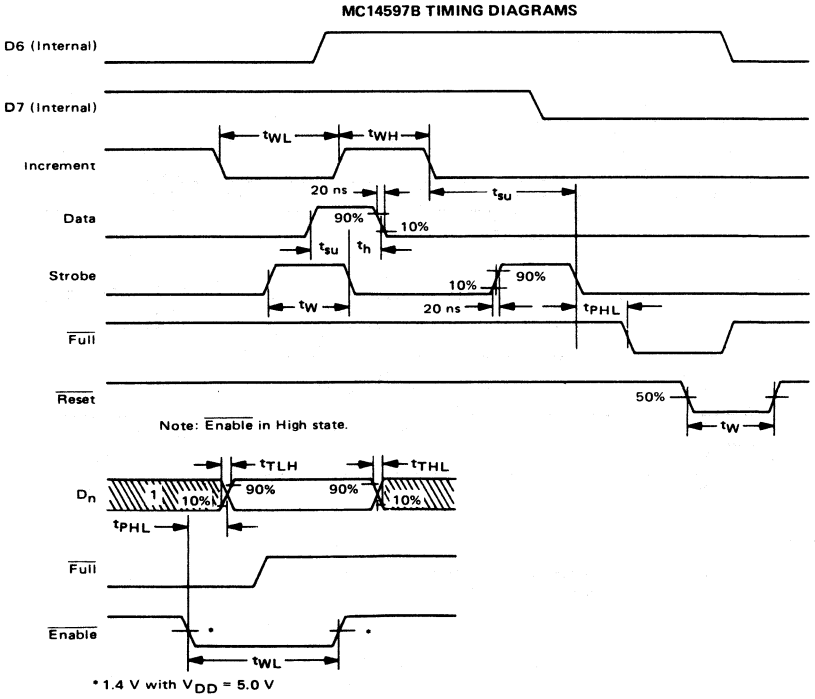
†The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS* (T_A = 25°C, C_L = 130 pF + 1 TTL Load)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (0.5 ns/pF) C_L +35 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.2 ns/pF) C_L +25 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.16 ns/pF) C_L +20 ns		15	–	40	80	
Propagation Delay Time						ns
$\overline{\text{Enable}}$ to Output	t_{PLH},	5.0	–	160	320	
	t_{PHL}	10	–	125	250	
		15	–	100	200	
Strobe to Output		5.0	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
Strobe to $\overline{\text{Full}}$ (MC14597B only)		5.0	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
Reset to Output		5.0	–	175	350	ns
		10	–	90	180	
		15	–	70	140	
Pulse Width						
$\overline{\text{Enable}}$	t_{WH},	5.0	320	160	–	ns
	t_{WL}	10	240	120	–	
		15	160	80	–	
Strobe		5.0	200	100	–	ns
		10	100	50	–	
		15	80	40	–	
Increment (MC14597B only)		5.0	200	100	–	ns
		10	100	50	–	
		15	80	40	–	
Reset		5.0	300	150	–	ns
		10	160	80	–	
		15	100	50	–	
Setup Time						
Data	t_{su}	5.0	100	50	–	ns
		10	50	25	–	
		15	35	20	–	
Address (MC14598B only)		5.0	200	100	–	ns
		10	100	50	–	
		15	70	35	–	
Increment (MC14597B only)		5.0	400	200	–	ns
		10	200	100	–	
		15	170	85	–	
Hold Time						
Data	t_h	5.0	100	50	–	ns
		10	50	25	–	
		15	35	20	–	
Address (MC14598B only)		5.0	100	50	–	ns
		10	50	25	–	
		15	35	20	–	

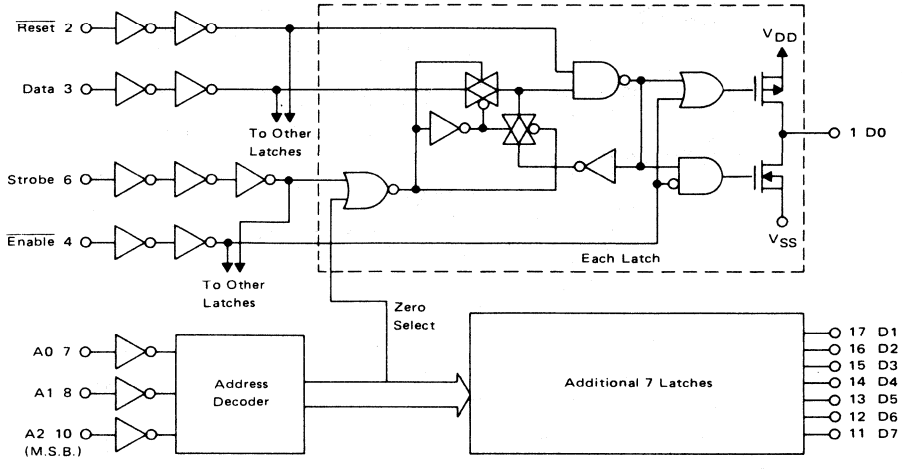
* The formulae given are for the typical characteristics only.



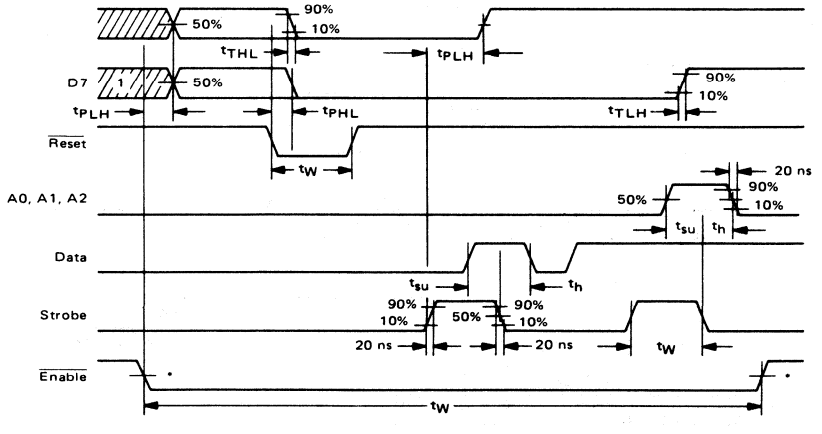


NOTES: 1. High-impedance output state (another device controls bus).
2. $\overline{\text{Reset}}$ in High state.

MC14598B FUNCTION DIAGRAM



MC14598B TIMING DIAGRAM



* 1.4 V with V_{DD} = 5.0 V.

NOTES 1. High-impedance output state (another device controls bus).

2. Output Load as for MC14597B.

LATCH TRUTH TABLE

Strobe	$\overline{\text{Reset}}$	Addressed Latch	Other Latches
0	1	*	*
1	1	Data	*
X	0	0	0

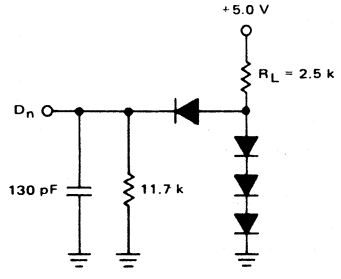
* = No change in state of latch
X = Don't care

TRUTH TABLE FOR MC14597B

Increment	$\overline{\text{Enable}}$	$\overline{\text{Reset}}$	Address Counter	$\overline{\text{Full}}$
⎍	X	1	Count Up	–
⎍	X	1	No Change	–
X	1	0	Reset to Zero	Set to One
X	0	1	No Change	Set to One
X	1	1	If at ADDRESS 7	To Zero on Falling Edge of STROBE

X = Don't care

Test Load
All Outputs



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MOTOROLA

MC14599B

FOR COMPLETE DATA
SEE MC14099B

8-BIT ADDRESSABLE LATCHES

The MC14099B and MC14599B are 8-bit addressable latches. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. Chip enable must be high for writing into MC14599B. For the MC14599B the data pin is a bidirectional data port and for the MC14099B the input is a unidirectional write only port. The Write/$\overline{\text{Read}}$ line controls this port in the MC14599B.

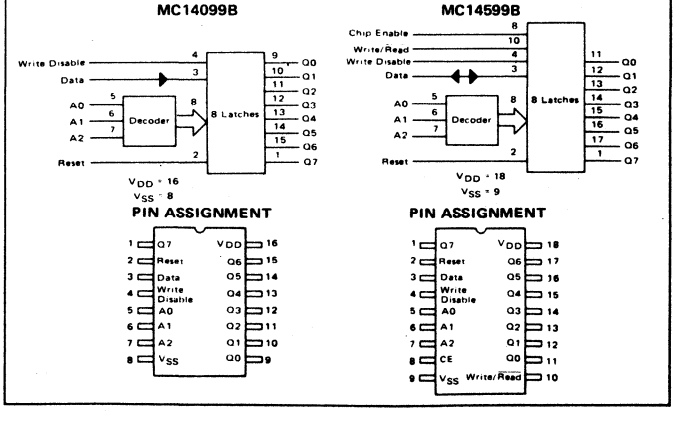
The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/$\overline{\text{Read}}$ or Chip Enable.

A Master Reset capability is available on both parts.

- Serial Data Input
- Parallel Output
- Low Input Capacitance — 5.0 pF typical
- Master Reset
- Noise Immunity — 45% of V_{DD} typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B
- Pin for pin compatible with Fairchild 4724.

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range - AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

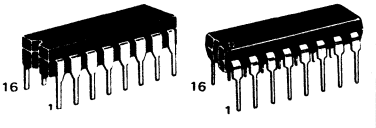


CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

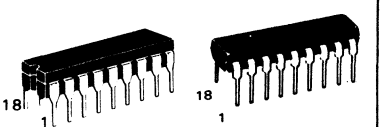
8-BIT ADDRESSABLE LATCH

MC14599B WITH BIDIRECTIONAL PORT



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 726

P SUFFIX
PLASTIC PACKAGE
CASE 707

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Mechanical Data

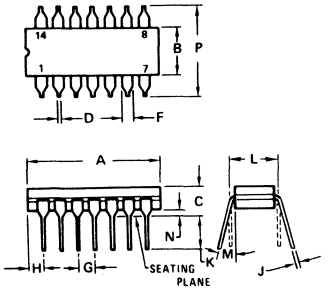
4

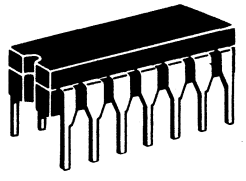
Mechanical Data

The package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter.

14-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 632

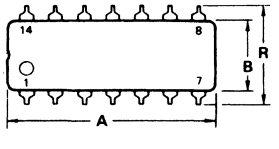


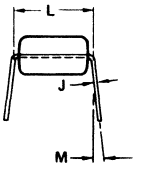


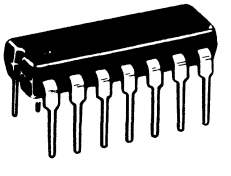
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.

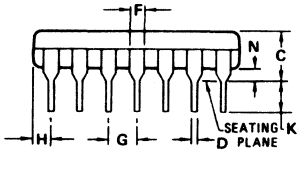
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	1.9	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

P SUFFIX
PLASTIC PACKAGE
CASE 646







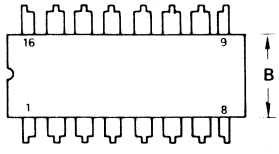


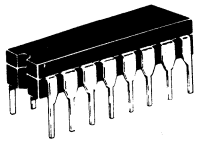
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

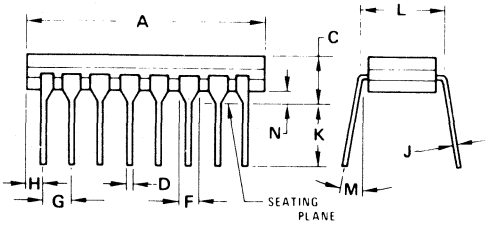
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

16-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 620





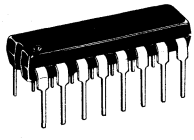


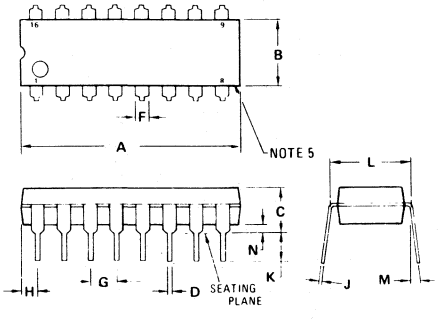
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM. "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIM. "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
5. DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

4

P SUFFIX
PLASTIC PACKAGE
CASE 648



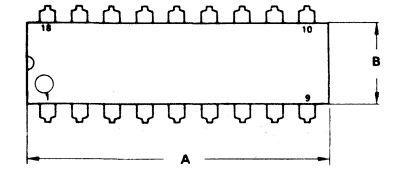


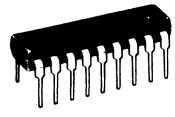
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

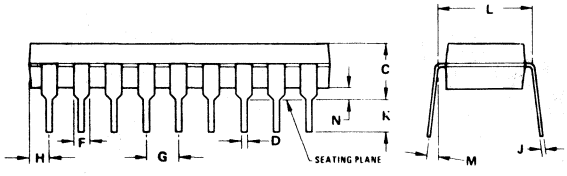
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

18-PIN PACKAGES

P SUFFIX
PLASTIC PACKAGE
CASE 707





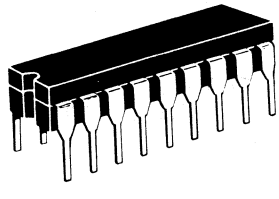


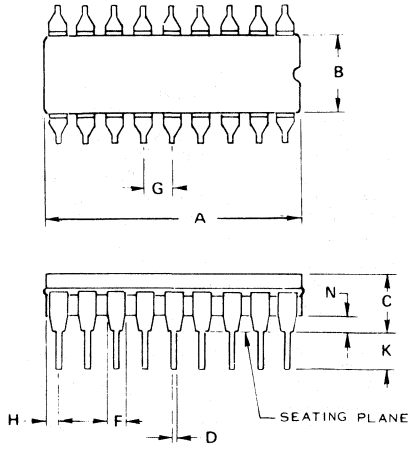
NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

L SUFFIX
CERAMIC PACKAGE
CASE 726



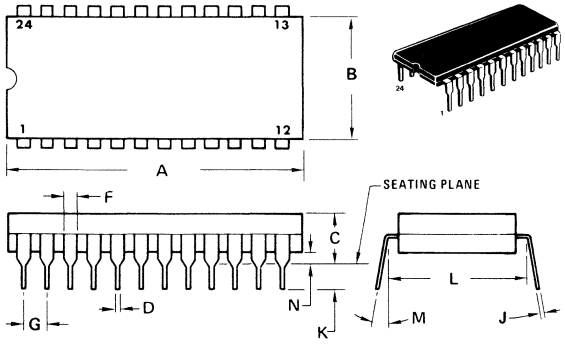


NOTES:
1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIM. "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM. "A" & "B" INCLUDES MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

24-PIN PACKAGES

L SUFFIX
CERAMIC PACKAGE
CASE 623

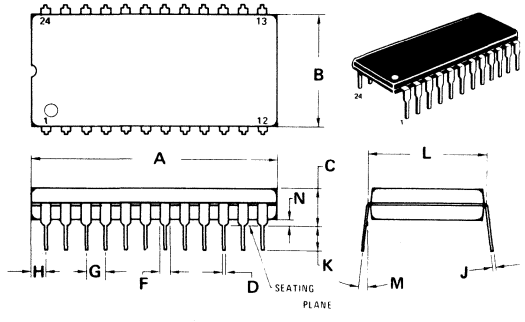


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

4

P SUFFIX
PLASTIC PACKAGE
CASE 709



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

4

Handling Precautions

5

Handling Procedures for CMOS Devices

Motorola CMOS devices have diode input protection against adverse electrical environments such as electrostatic discharge. In regards to this, the following statement is included on each data sheet:

> This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Unfortunately, severe electrical transient voltages can be generated during handling. For example, static voltages generated by a person walking across a common waxed floor have been measured in the 4 to 15 kV range (depending on humidity, surface conditions, etc.). These static voltages are potentially dangerous when discharged into a CMOS input, considering the energy stored in the capacity ($\approx$ 300 pF) of the human body at these voltage levels.

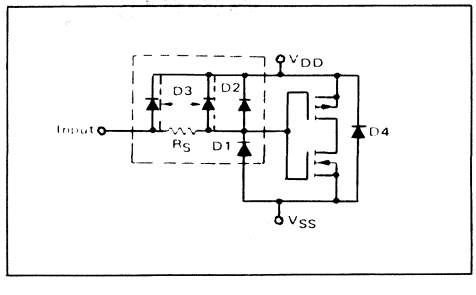
Present CMOS gate protection structures can generally protect against overvoltages. This is usually sufficient except in the severe cases.

The input protection circuit, while adding some delay time, provides protection by clamping positive and negative potentials to V_{DD} and V_{SS} respectively. Figure 1 shows the internal circuitry for the diode-resistor protection.

The input protection circuit consists of a series isolation resistor R_S, whose typical value is 1.5 kΩ, and diodes D1 and D2, which clamp the input voltages between the power supply pins V_{DD} and V_{SS}. Diode D3 is a distributed structure resulting from the diffusion fabrication of R_S.

5

FIGURE 1 — SCHEMATIC DIAGRAM, DIODE-RESISTOR INPUT PROTECTION



In addition to the internal protection network, the following steps are recommended to further reduce damage to CMOS integrated circuits due to improper handling.

1. All CMOS devices should be stored or transported in materials that are antistatic. CMOS devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.

2. The shipping rails are antistatically treated inside and outside. They provide adequate protection during storage and test/assembly handling operations, but should not be re-cycled as continuous use will cause deterioration of the antistatic coating.

3. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 2.

4. Nylon or other static generating materials should not come in contact with CMOS circuits.

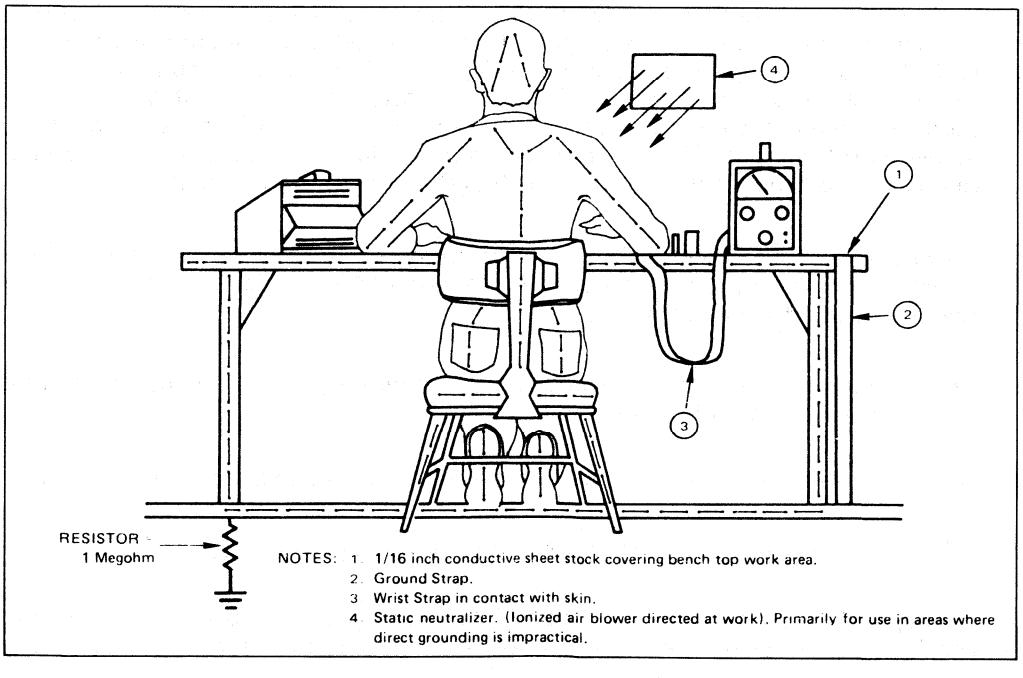
5. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices or boards. Avoid this by grounding suspect areas and/or by the use of ionized air blowers, and/or air humidifiers.

6. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.

7. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.

8. The following steps should be observed during wave solder operations.
   a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.

FIGURE 2 — TYPICAL MANUFACTURING WORK STATION



b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
c. Operators must comply with precautions previously explained.
d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.

9. The following steps should be observed during board cleaning operation.
   a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
   b. Brush or spray cleaning should not be used.
   c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
   d. Cleaned assemblies should be placed in antistatic container immediately after removal from the cleaning basket.
   e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.

10. The use of static detection meters for line surveillance is highly recommended.

11. All low impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the CMOS is powered up. Similarly, this type of equipment should be disconnected before power is turned off.

12. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.

13. A circuit board containing CMOS devices is merely an extension of the device and the same handling precautions apply. Contacting edge connectors wired directly to CMOS device inputs can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address only an input of a CMOS integrated circuit, it is recommended that a resistance or 10 kΩ or greater be used in series with the input. This resistor will limit accidental damage if the PC board is removed and brought into contact with static generating materials.

14. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing CMOS devices to be certain there are no voltage transients present.

15. Double check test equipment setup for proper polarity of voltage before conducting parametric or functional testing.

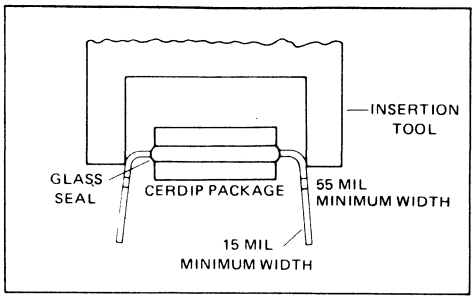
16. Do not exceed the maximum electrical voltage ratings specified by the data sheet.

17. All unused device inputs should be connected to V_{DD} or V_{SS}.

Another type of precaution involves the CERDIP package. Since this device employs a glass seal, a high stress on the leads can cause hermeticity failure which will eventually

result in aluminum corrosion on the die. To avoid this, the leads should never be flexed above the seating plane. All insertion tools or automated equipment should contact the lead at its narrowest dimension allowing it to bend without affecting the wide portion above the seating plane.

FIGURE 3 — CERDIP INSERTION PRECAUTIONS



5

Reliability and Quality Assurance

6

Reliability and Quality Assurance

Motorola has an active Quality Improvement Program with the objective of improving failure rates and permitting tighter AQLs. At the time of writing — 84Q2 — the following data was applicable. For current data, please contact your Motorola Sales Office or franchised Motorola distributor.

OUTGOING QUALITY

Functional/Parametric Combined 0.065 % AQL Level II

Visual/Mechanical Combined 0.10 % AQL Level II

FAILURE RATES

TABLE 1 — FAILURE RATES FOR PLASTIC AND CERAMIC PACKAGES

Package	Failure Rate in %/1000 hours at Ambient Temperature:		
	50°C	70°C	85°C
Plastic	0.0003	0.0027	0.0109
Ceramic	0.0001	0.0007	0.0030

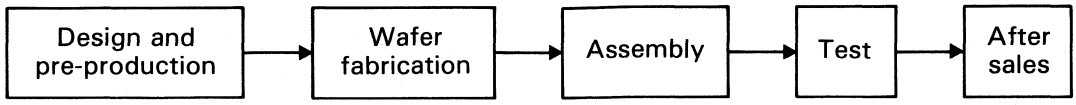
The Motorola Philosophy

Our objective is to further improve our position as the quality leader in the supply of semiconductor products.
Our strategies are:

1. Actively promote a quality conscious attitude and quality environment in all process, manufacturing and support operations.
2. Actively promote quality improvement plans.
3. Maintain and improve programmes for the continuous improvement of outgoing quality and reliability.
4. Constantly measure and provide product reliability data.
5. Support and develop the Motorola world-wide P.P.M. culture.
6. Provide a fast responsive service for investigating customer related problems.
7. Further improve good working relationships with customers' quality/engineering operations.

Reliability and Quality Assurance Activities

In order to assure conformance to specifications, and to assure high levels of quality and reliability, there are R & QA activities in all parts of the production cycle.



Supporting all these activities is our product analysis group and providing supplementary support is our Hi-Rel operations group.

1. PRE-PRODUCTION

Quality Assurance starts before production commences. Within Motorola, all new production related activities and modifications thereto must be specified, qualified and approved prior to implementation. The form of control is defined by the change, and different controls are used for suppliers, raw materials, processes, equipments, designs and packages. Tables 2 and 3 list the qualification tests. Figure 1 shows two typical qualification and approval flows, one for a new circuit and one for a process change. Before approval is given, three consecutive lots must pass the tests. Once approved, the specification is signed off and production can commence.

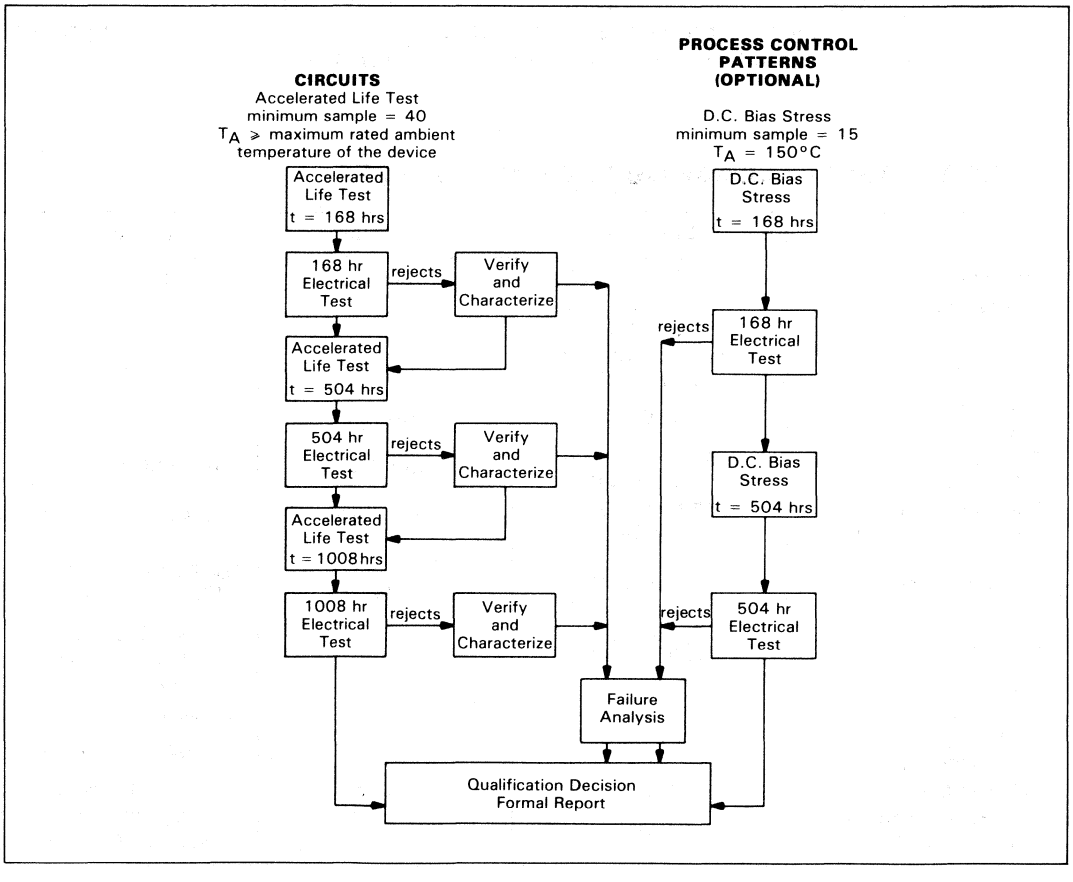
TABLE 2 — NEW PACKAGE QUALIFICATION TESTS

Test	Condition	Duration	Reference
Electrical Endurance	125°C, 5V or 15V	1000 Hours	BS9400
Temperature, Humidity Bias	85°C, 85% R.H. 5V or 15V	1000 Hours	—
Autoclave	121°C, 100% R.H. 15 P.S.I.G.	240 Hours	—
High Temperature Storage	150°C	1000 Hours	BS9400 1.2.6.3
Thermal Cycle (Air to Air)	−65°C to 150°C 5 Min Dwell	1000 Cycles	BS9400 1.2.6.13
Thermal Shock (Liquid to Liquid)	−65°C to 150°C 5 Min Dwell	1000 Cycles	BS9400 1.2.6.19
Shock & Vibration	1500G, 3 per axis 20G, 150-2000Hz per axis	0.5 mS 2 Hours	BS9400 1.2.6.6/11 BS9400 1.2.6.8.1
Hermeticity	1.85, 10^{-8} STD CC/SEC	—	MIL STD 883 Method 014.1
Visual Inspection	—	—	BS9400 1.2.2.1
Dimensions	—	—	BS9400 1.2.3
Marking Permanency	—	—	BS9400 1.2.6.18
Solderability	230°C	3 Sec	BS9400 1.2.6.15.1
Wire Bond Strength (Post Seal)	1.5 Gram	—	MIL STD 883, Method 2011.1.C

TABLE 3 — NEW PROCESS QUALIFICATION TESTS

Test	Condition	Duration	Reference
Electrical Endurance	125°C, 5V or 15V	1000 Hours	BS9400
Temperature, Humidity Bias	85°C, 85% R.H. 5V or 15V	1000 Hours	—
Autoclave	121°C, 100% R.H. 15 P.S.I.G.	240 Hours	—
High Temperature Storage	150°C	1000 Hours	BS9400 1.2.6.3
Thermal Cycle (Air to Air)	−65°C to 150°C 5 Min Dwell	1000 Cycles	BS9400 1.2.6.13
Thermal Shock (Liquid to Liquid)	−65°C to 150°C 5 Min Dwell	1000 Cycles	BS9400 1.2.6.19
Shock & Vibration	1500G, 3 per axis 150-2000Hz, 20G, per axis	0.5 mS 2 Hours	BS9400 1.2.6.6/11 BS9400 1.2.6.8.1
Data Retention Bake (Non Volatile Memories)	200/250°C	1000 Hours	—

FIGURE 1 — QUALIFICATION AND APPROVAL FLOW FOR A NEW CIRCUIT AND A WAFER FABRICATION MODIFICATION



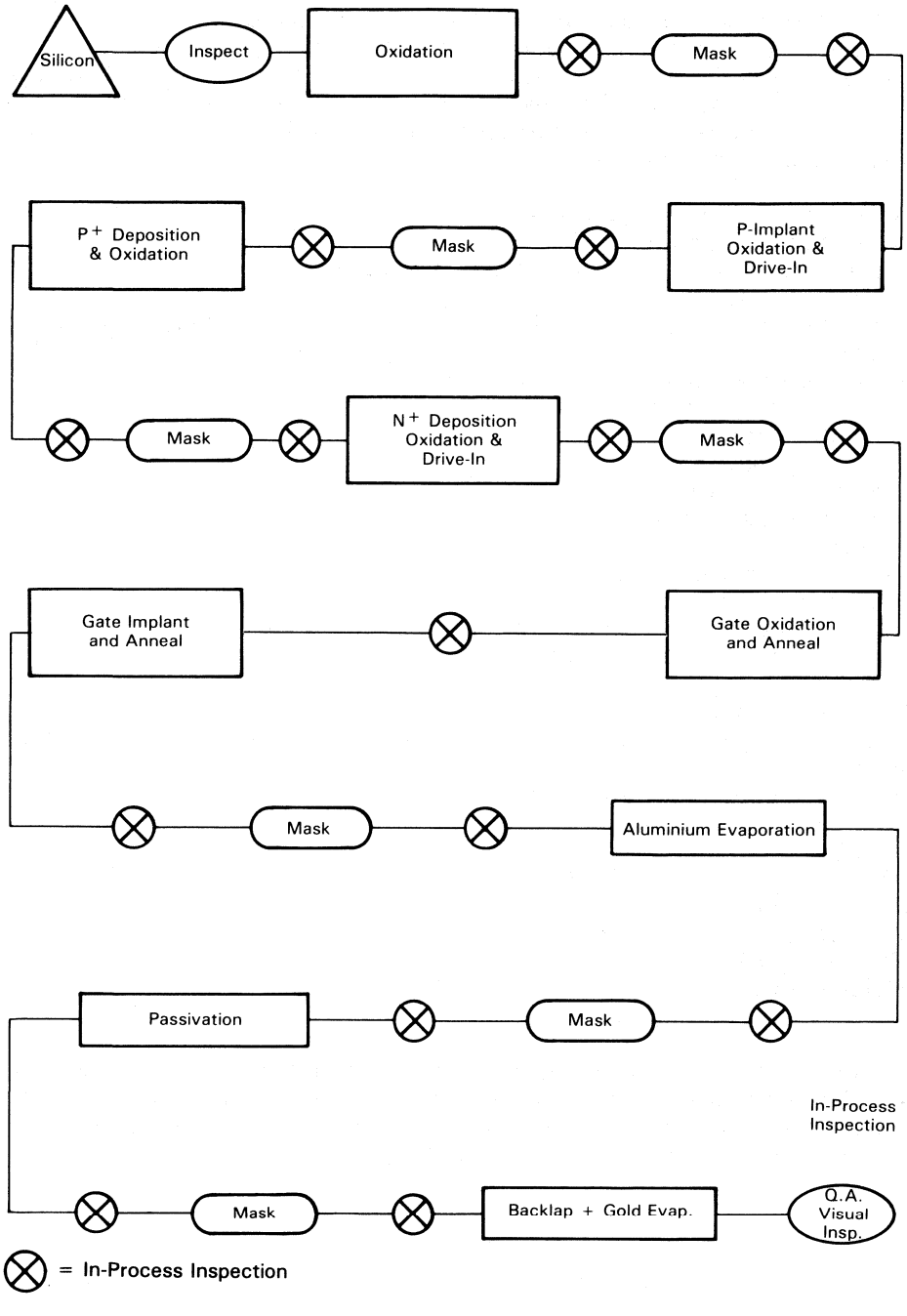
2. WAFER FABRICATION

The Wafer fabrication process is a complex one, involving small geometries, physics, chemistry and ultra high levels of purity and cleanliness. Figure 2 depicts the process flow and highlights the major process steps. The quality assurance activities are designed to give process control at each major process step, and to perform real time evaluation of the process at intermediate points within the process.
The process control activities are:

1. Incoming inspection of raw materials.
2. Incoming inspection of masks.
3. Capacitance Voltage Drifts on Tubes/Product/Evaporator.
4. Oxide thickness/sheet resistance.
5. Vapox Chemical Vapour Deposition (Doped/Undoped), thickness, % Phosphorous and Integrity.
6. Gate oxide breakdown (Furnaces/Lomac).
7. Source bubbler monitor.
8. Gas bottle pressures.
9. Implant evaluation.
10. Furnace temp. profiles.
11. 4 Pt. Probe calibration check.
12. Spin Drier.
13. De-ionized water/bacteria monitor.
14. Mask clean inspection.
15. Photoresist equipment check, Resist thickness monitor, Pinhole check.
16. Scanning Electron Microscope — Surface profiles, Junction depth.
17. Final visual inspection.
18. Shutter leakage, Metal thickness, Reflectivity, Sheet resistance and Monitors on evaporators.
19. Fab environmental monitor — clean room and work stations.
20. Perkin Elmer aligner checks.
21. Junction depth monitor.
22. Oxidation induced stacking faults.
23. Quartzware check.
24. Monitor incoming acid quality.
25. Mylar burn and gas spectrum check on implanter.
26. Wafer analysis.
27. Electrical probe monitor.

These activities not only measure the characteristics of each lot, but also measure trends within the process from which extrapolations are made to give forewarning of potential problems. This feedback avoids reliability and quality problems and maintains optimum operation of the Wafer fabrication facility.

FIGURE 2 — CMOS WAFER FABRICATION (SIMPLIFIED)



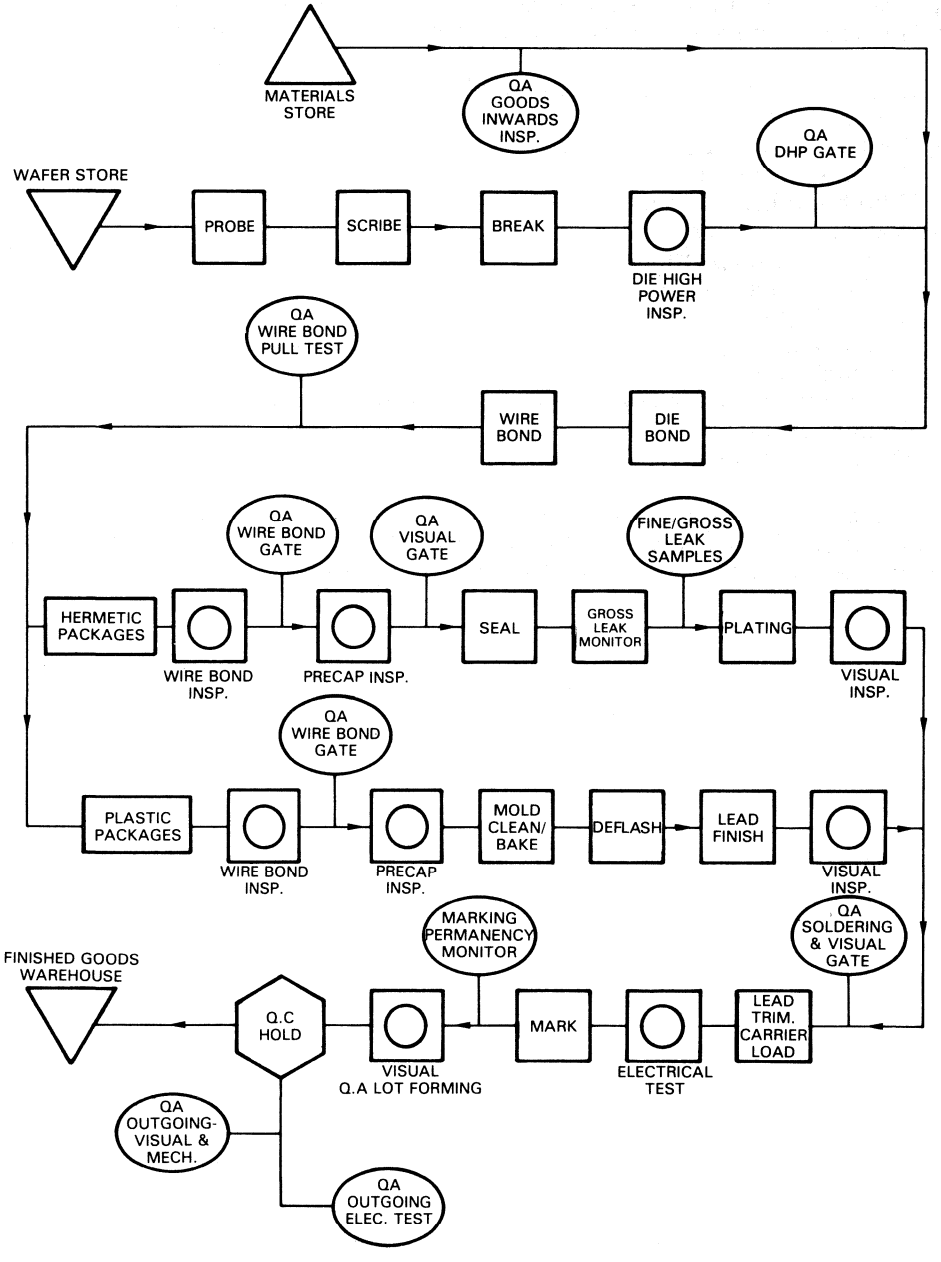
3. ASSEMBLY

Assembly is highly automated — which benefits reliability and quality. In addition to the 100% screens, there are the following assembly quality activities:

1. Incoming inspection of raw materials.
2. Scribe audit.
3. Die high power visual inspection.
4. Die bond inspection.
5. Wire bond inspection.
6. Pre-cap inspection.
7. Hermeticity inspection.
8. Plating inspection.
9. Solderability.
10. Terminal strength.
11. Dimensions monitor.
12. Visual/mechanical inspection for flaws to body/leads.
13. Calibration monitor.
14. Moisture monitor.

An integral part of the assembly operation is to give every device a coded marking which defines the assembly location, the Wafer fabrication lot and the assembly lot. Thus it is possible to trace the history of every device.

FIGURE 3 — TYPICAL INTEGRATED CIRCUITS ASSEMBLY & FINAL TEST FLOW CHART



6

4. TEST

After 100% electrical test, there is a final inspection before the product is shipped to the warehouse. The inspection is

Functional/Parametric Combined 0.065 % AQL Level II *
Visual/Mechanical Combined 0.10 % AQL Level II *

Electrical parameters include all parameters on the data sheet. Visual/mechanical includes marking legibility, plating, dimensions, etc. We even include the orientation of the devices within the tube!

We believe these are the best AQLs for standard CMOS product in the Semiconductor Industry, and our objective is to maintain this position.

In addition, Motorola has a series of weekly audits as follows:

1. Finished goods.
2. Marking/marking permanency.
3. Hermeticity.
4. Dimensions.
5. Outgoing shipments.
6. Specifications/procedures.
7. Static protection.
8. General housekeeping.
9. Calibration.

The combination of audits and lot inspection is designed to give maximum protection to our customers. Feedback from our customers shows that they find a reject rate of typically less than 200 PPM, i.e. 1 failure in every 5,000 parts supplied. At this low level, incoming inspection is not cost efficient and it is possible to reduce or eliminate incoming inspection.

Of equal importance to incoming quality is product reliability. Motorola has a comprehensive reliability program which assesses all aspects of product reliability. The program comprises the following periodic tests which are designed to provide mechanical, environmental and electrical stresses which will accelerate the life cycle into a short period:

- Visual inspection.
- Dimensions.
- Marking permanency.
- Resistance to cleaning fluids.
- Solderability and plating.
- Acceleration.
- Wire bond.
- Hermeticity.
- Thermal shock.
- Temperature cycling.
- Mechanical shock and vibration.
- Flammability.
- High temperature storage.
- High temperature electrical endurance.
- Temperature/humidity/bias.
- Pressure/temperature/humidity.

** Correct as of 84Q2.*

The most significant test is high temperature electrical endurance which is performed at 125°C with the application of a 15V static bias in accordance with the truth table of the individual device. This test accelerates any inherent die related failure mechanisms.

Electrical tests to Motorola Data Sheet specifications are used to measure the performance of the devices. The number of failures at the 1,008 hour readout (including both parametric downgrades and catastrophics) are extrapolated to a lower temperature to provide a failure rate at 85°C. The mathematical models employed to predict this are detailed in the appendix to this chapter.

TABLE 4 — HIGH TEMPERATURE ELECTRICAL ENDURANCE RESULTS FOR PLASTIC PACKAGES (1982)

No. of Batches	No. of Devices	No. of Device Hours at 125°C	Equivalent Device Hours at 85°C	No. of Failures	Failure Rate % / 1,000 hours ———Temperature——— 50°C	70°C	85°C
35	3,302	3.33M (380 years)	86.31M (9,850 years)	8	0.0003	0.0027	0.0109

The failure rate at 85°C of 0.0109% / 1,000 hours (or a mean time between failures of 1,047 years) is graphed in Figure 4 and compares favourably with our 1981 standard of 0.030% / 1,000 hours.

TABLE 5 — HIGH TEMPERATURE ELECTRICAL ENDURANCE RESULTS FOR CERAMIC PACKAGES (1982)

No. of Batches	No. of Devices	No. of Device Hours at 150°C	Equivalent Device Hours at 85°C	No. of Failures	Failure Rate % / 1,000 hours ———Temperature——— 50°C	70°C	85°C
25	2,394	2.41M (275 years)	350.15M (39,971 years)	9	0.0001	0.0007	0.003

The failure rate at 85°C of 0.003% / 1,000 hours (or a mean time between failures of 3,805 years) is graphed in Figure 4 and is impressingly low when compared with our 1981 standard of 0.014% / 1,000 hours.

The steady reduction of plastic and ceramic failure rates reflects Motorola's commitment to reliability and quality improvement. The improvements are such that many customers who previously purchased burnt-in components now achieve the same or better reliability using Motorola CMOS without burn-in.

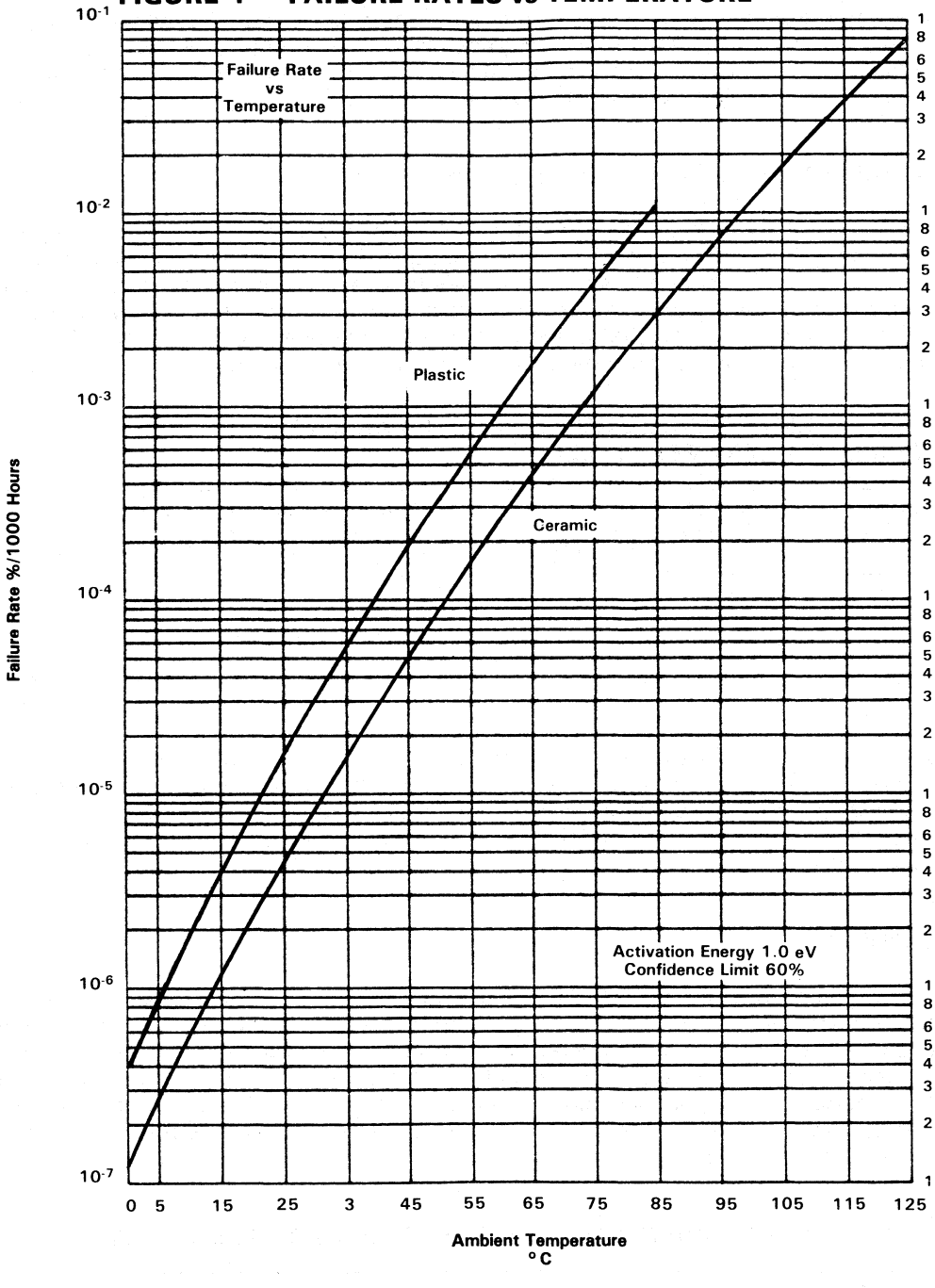
6

CERAMIC vs PLASTIC

It is recommended that hermetic ceramic product be used in extreme high temperature or humidity environments. Plastic product will provide similarly excellent reliability for lower cost in more normal operating conditions.

All plastic packaged devices are intrinsically non-hermetic as moisture can penetrate the lead frame/package seal interface or diffuse through the bulk of the plastic. If water reaches the surface of the chip and a bias is applied, an electrolytic cell is set up. Corrosion of the aluminium tracks/bond pads can occur which can downgrade the device

FIGURE 4 — FAILURE RATES vs TEMPERATURE



parameters and lead to catastrophic (open metal) failures. This phenomenon is accelerated by the presence of contaminants and Motorola is careful to minimize this effect by the use of quality grade materials/packaging and meticulous housekeeping. The tests which best monitor the environmental related performance of the plastic package are Temperature Humidity Bias, Autoclave, and Thermal Shock.

TEMPERATURE HUMIDITY BIAS (T.H.B.)

This environmental test is the most reliable method of highlighting any die/package incompatibility. It is performed at 85°C, 85% Relative Humidity with the application of a static bias of 15V. The conditions of this test are far in excess of those ever expected to be experienced by the device in a normal operating environment. The results below are for 1982. It should be noted that there are a number of die and package modifications pending which are expected to provide further significant improvements in the results.

TABLE 6 — TEMPERATURE HUMIDITY BIAS RESULTS FOR PLASTIC PACKAGES (1982)

No. of Batches	No. of Devices	% Total Cumulative failure (test hours)				
		168	336	504	774	1,008
3	378	0.31	0.31	0.63	0.63	0.94
		% Cumulative Corrosion failures				
3	378	0.31	0.31	0.31	0.31	0.63

The small number of failures due to corrosion of the metallization is a result of the closely matched package components. The remaining rejects show the same failure modes as noted for electrical endurance. These results are an improvement on those recorded previously and verify that no new failure patterns have emerged in house or should be expected in the field.

AUTOCLAVE

The conditions of this test are 121°C, 15 p.s.i.g. and 100% Relative Humidity. It is a moisture resistance test without bias and is used to evaluate the durability of the plastic package under extremely high temperature and humidity conditions. This test is used as an ongoing assembly process monitor and supplements the T.H.B. corrosion failure results. In view of the highly accelerated test environment and the fact that very small changes in these test conditions can have a dramatic effect on the end results, the data is included for information only.

TABLE 7 — AUTOCLAVE RESULTS FOR PLASTIC PACKAGES (1982)

No. of Batches	No. of Devices	% Cumulative failure (test hours)				
		24	48	96	148	168
4	347	0.00	0.00	0.00	0.00	0.58

The Autoclave results augment those recorded for T.H.B. performance and demonstrate the moisture resistant nature of the Motorola plastic encapsulated devices under extreme conditions.

THERMAL SHOCK

Thermal shock provides a quick and severe method of stress and is a liquid to liquid cycle between −65°C to +150°C with a dwell of five minutes at each temperature.

TABLE 8 — THERMAL SHOCK RESULTS FOR PLASTIC PACKAGES (1982)

No. of Batches	No. of Devices	% Cumulative failure (test cycles)	
		200	1,000
2	250	0.00	0.00

The results verify the plastic mould compound, bond wires and lead frames have closely matched coefficients of expansion. This benefit reduces the potential of moisture ingress (e.g. during the T.H.B. test) within the package ensuring a stable encapsulant for the die.

There is one further important source of quality and reliability data—feedback from our customers!

5. AFTER SALES

CUSTOMER FEEDBACK ENSURES QUALITY IMPROVEMENT

Customer feedback is obtained from incoming inspection and qualification results and from returned defective product.

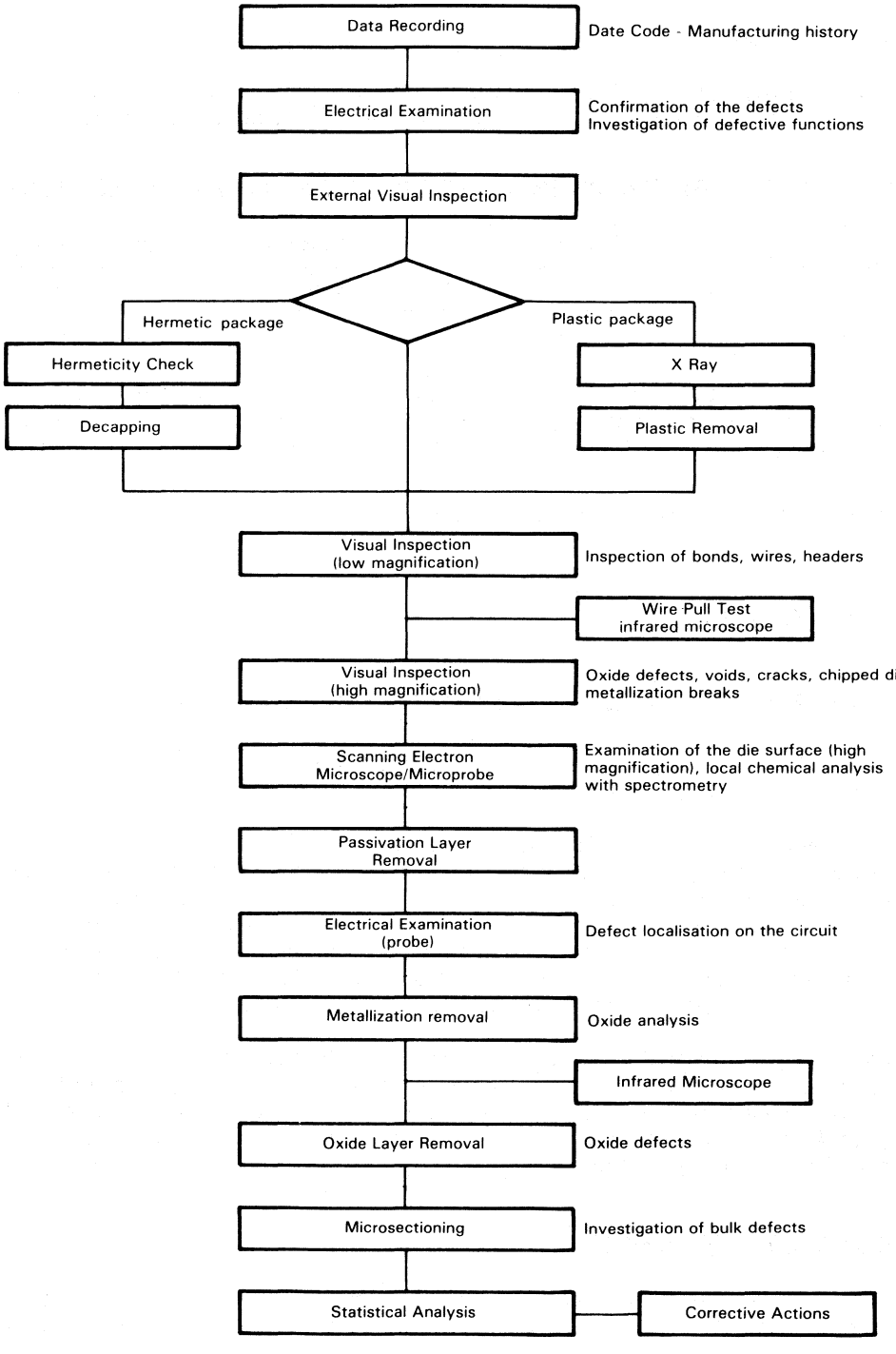
a) With certain customers who use large quantities of CMOS, Motorola has reached agreement on joint quality improvement programs. These programs are basically an exchange of information. Our customers provide feedback by device type on the quality and reliability of our product. Analysis of this feedback highlights problems not previously apparent, and corrective action is implemented. Both Motorola and all our customers have benefitted from these programs. The incoming quality level as reported by these customers is typically less than 200 PPM.

b) Due to the high quality of our product, it is possible to analyse every return of defective product. Approximately 40% of these are in fact non-defective and are the result of correlation problems. Some of the returns have been mishandled (see Chapter 4), the remainder are analysed to determine where action can be taken to improve the outgoing quality.

6. PRODUCT ANALYSIS

Product analysis is used at all stages of manufacturing—from pre-production to after sales—to determine failure mechanisms and how to avoid them. Various techniques are

FIGURE 5 — ANALYSIS FLOW FOR FINISHED PRODUCT



used and our failure analysis laboratory is well equipped with a variety of equipment including scanning electron microscopes, X-ray analysers and micromanipulative probers. Figure 5 shows the flow used for finished product.

7. HI-REL

Motorola's Hi-Rel programs—for avionic, space and military applications—has indirectly provided a considerable contribution to our commercial products. The Hi-Rel programs set the standards for the control of quality and the assessment of reliability, and at Motorola we use these standards for our commercial product as well as our Hi-Rel product. At the time of writing, Motorola has the following approvals for CMOS product:

DEF STAN 05/31	— MOD Registration 1G9MO1
DEF STAN 05/21	— MOD Registration 1G9MO1
BSI	App. No. 1085 M
CECC	App. No. M0070/CECC/UK 1085 M

CONCLUSION

With design and manufacturing facilities in the U.S.A., Japan and Europe, Motorola's experience in CMOS is unsurpassed. In Europe alone, Motorola has shipped over 500,000,000 CMOS devices. The levels of quality and reliability which we have achieved are extremely high. Through our quality improvement program, we will achieve even higher levels for the benefit of you, our customer.

APPENDIX

FAILURE RATE CALCULATIONS:

Two mathematical models are employed to predict the failure rate. Firstly it is assumed that the failure rate distribution follows an exponential probability density function.

$$F(X) = \lambda \text{ EXP } /-\lambda\ t)$$

where $F(X)$ = probability density function

λ = failure rate

t = time

Since reliability evaluations usually involve random samples of a population, a point estimation for the failure rate is calculated using the Chi-squared distribution.

$$\lambda = \frac{\chi^2\ (\alpha,\ 2r + 2),}{2nt} \qquad \alpha = \frac{(100 - CL)}{100}$$

where χ^2 = tabulated value

CL = confidence limit in percent

r = number of rejects

n = number of devices

t = duration of the test

A confidence limit of 60% is employed in the formula.

The second model uses the Arrhenius Equation to relate the failure rate at test temperature to that expected at normal operating conditions.

$$R(T) = Ro \text{ EXP } (E_a / kT)$$

where $R(T)$ = reaction rate at normal temperatures

Ro = a constant

E_a = activation energy (1eV)

k = Boltzmann's constant

T = junction temperature

6

The use of junction temperatures rather than ambient (lifetest) temperature provides a more accurate failure rate. The junction temperature is computed using the equation below:

$$T(J) = T(A) + (P \times \theta_{JA})$$

where $T(J)$ = junction temperature (°C)

$T(A)$ = ambient temperature (°C)

P = power (Watts)

θ_{JA} = average junction to ambient thermal resistance (°C/W)

Publications and Applications

7

Data Books, Brochures and Selection Guides

Additional information on CMOS products can be found in the following publications available at your nearest Motorola Sales Office or Distributor.

DATA BOOKS

B001 A/D and D/A Conversion Manual

B002B CMOS Data Manual, Volume 2, Special Functions

B002C CMOS Data Manual, Volume 3, High Speed CMOS

B003A Home Electronics / Integrated Circuits

B011 Memory Data Manual

B025 The European Master Selection

B039 Telecommunications Data Manual

BROCHURES AND SELECTION GUIDES

F045 Telecommunications, A System Approach

F055 High Speed CMOS Function Selector Guide

F060 Catalog of Technical Literature

F062 CMOS Standard Logic Reliability Report

F072 Macrocell Arrays and CAD

F075 CMOS Function Selector Guide

F077 High Speed CMOS Life Test

APPLICATION NOTES

A complete list of Application Notes can be found in the Catalog of Technical Literature (Reference F060).

AN-538A Motorola Complementary MOS I/C's.

This note discusses some of the properties of N-channel and P-channel MOSFET's and describes how they are used to construct complementary MOS integrated circuits. Some basic CMOS logic functions are then discussed.

AN-707 Noise Immunity Comparison of CMOS versus Bipolar Logic Families.

This application note compares the noise immunity of CMOS and bipolar families and includes general notes on common noise sources, precautions against noise, noise specification and standard noise tests.

AN-712A Interface Techniques between Industrial Logic and Power Devices.

This application note presents worst case design approaches to illustrate the methods of interfacing MCMOS and MHTL logic to various power load levels, both a.c. and d.c. Interface devices vary from small-signal transistors to power transistors and thyristors, using direct coupling/level translation and optoelectronic coupling techniques.

AN-715 Introduction to CMOS Integrated Circuits with Three-State Outputs.

This note describes a wide variety of standard CMOS integrated circuits incorporating transmission gates with standard logic. Design rules and applications of these devices include the areas of analog switching and multiplexing, digital multiplexing and data bussing.

AN-768 CMOS Schmitt Triggers.

The Motorola Schmitt triggers—MC14093B, MC14583B and MC14584B—are described. Operating characteristic, theory of operation, and applications of Schmitt triggers are covered.

AN-772 CMOS Monostable Multivibrators.

This note describes the theory and operation of the MC14538B precision monostable multivibrator, which incorporates both digital and linear CMOS technology. Applications are described.

AN-843 A Review of Transients and their means of Suppression.

Transient sources within and outwith electronic equipment are described and characterised, and methods of suppression, and their applications, are covered.

AN-874 Macrocell Arrays: Concept-Features-CAD Interface.

High technology array based products offer the advantages of custom circuits, yet overcome the problems of high costs and long design cycles. Recent developments in array technology make use of Macrocell building blocks rather than primitive gates for easier design and higher performance. Additional developments in computer-aided-design customer interface systems simplify the job of developing array circuit options. This note examines Motorola's Macrocell array concept with special emphasis on the CAD user interface.

1 Selection Guides

2 B-Series Family Data

3 Data Sheets

4 Mechanical Data

5 Handling Precautions

6 Reliability and Quality Assurance

7 Publications and Applications